JPE 19-5-5

https://doi.org/10.6113/JPE.2019.19.5.1108
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Design Methodology for Optimal Phase-Shift Modulation of Non-Inverting Buck-Boost Converters

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Abstract

The non-inverting buck-boost converter (NIBB) is a step-up and step-down DC-DC converter suitable for wide-input-voltage-range applications. However, when the input voltage is close to the output voltage, the NIBB needs to operate in the buck-boost mode, causing a significant efficiency reduction since all four switches operates in the PWM mode. Considering both the current stress limitation and the efficiency optimization, a novel design methodology for the optimal phase-shift modulation of a NIBB in the buck-boost mode is proposed in this paper. Since the four switches in the NIBB form two bridges, the shifted phase between the two bridges can serve as an extra degree of freedom for performance optimization. With general phase-shift modulation, the analytic current expressions for every duty ratio, shifted phase and input voltage are derived. Then with the two key factors in the NIBB, the converter efficiency and the switch current stress, taken into account, an objective function with constraints is derived. By optimizing the derived objective function over the full input voltage range, an offline design methodology for the optimal modulation scheme is proposed for efficiency optimization on the premise of current stress limitation. Finally, the designed optimal modulation scheme is implemented on a DSPs and the design methodology is verified with experimental results on a 300V-1.5kW NIBB prototype.

Key words: Buck-boost mode, Current stress limitation, Efficiency optimization, Non-inverting buck-boost, Phase-shift modulation

I. INTRODUCTION

A wide input voltage range is common among various power electronic applications, such as solar generation which produces large voltage fluctuations. Under such circumstances, where input voltage has the chance to be higher or lower than the output voltage, a step-up/step-down converter is required to meet the demands of varying the ratio between the input and output voltage.

There are various types of step-up/step-down converters, including isolated DC/DC, Sepic, Zeta, Cuk, inverting Buck-Boost and non-inverting Buck-Boost converters (IBB and NIBB). The isolated DC/DC converters like DAB are not suitable for a wide input voltage range, which results in a large inductor current [3], [5]. For Sepic and Zeta converters, there are too many passive components, resulting in a low power density. The Cuk converter is a better choice as a current-source converter, but is not suitable for voltage source applications [4]. Although the IBB has less switches than the NIBB, it introduces much higher voltage and current stresses on the switches, and has higher values for the current RMS and the current ripple on the inductor [1], [2]. This results in higher requirements for the current capacity of the inductors and switches, which in turn results in higher costs. Therefore, the NIBB is a reasonable choice and is the main focus of this paper.

For the NIBB in Fig. 1(a), Q_{1SR} is complementary to Q_1, and Q_{2SR} is complementary to Q_2. Under a unidirectional power-flow situation such as PV power generation, Q_{1SR} and Q_{2SR} are usually kept off or replaced by two diodes as shown in Fig. 1(b) [4]. Both synchronous control and asynchronous control can be used for the NIBB. In synchronous control [2], Q_1 and Q_2 are switched on or off simultaneously, transforming the NIBB into the IBB and consequently causing higher

Manuscript received Jan. 2, 2019; accepted May 14, 2019
Recommended for publication by Associate Editor Wu Chen.
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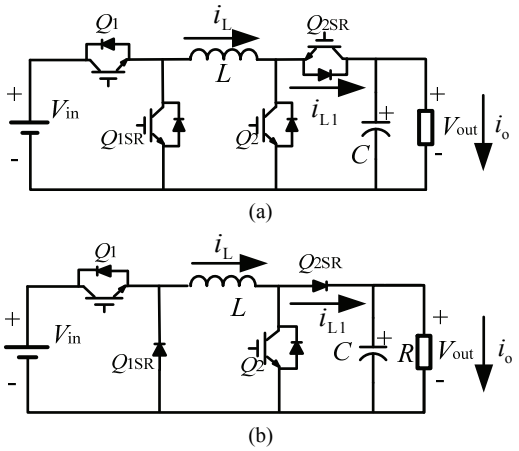


Fig. 1. Non-inverting buck-boost converter. (a) Four active switches. (b) Two active switches.

voltage and current stresses. To solve this problem, asynchronous control was proposed for voltage and current stress reduction.

In asynchronous control, the control signal of Q_1 is independent from that of Q_2. Two-mode control (buck mode and boost mode) has attracted the attention of some researchers thanks to its high efficiency [6]-[9]. When the input voltage is lower than the output voltage, Q_2 is switched on and off while Q_1 is kept on. This is called the boost mode. When the input voltage is higher than the output voltage, Q_1 is on and off while Q_2 is kept off. This is called the buck mode. However, neither of the modes can operate well when the input voltage is close to the output voltage due to switching delay and driver delay [10], [11]. Therefore, a buffer mode, when the input voltage gets close to the output voltage, is inserted between the buck and boost modes, which is called three-mode control [12]-[14].

Three-mode control includes buck, boost and buck-boost modes. In the buck-boost mode, four switches (including two active power semiconductors and two diodes) operate at high frequencies, resulting in a significant increase of the switching loss. Many papers tend to improve efficiency by soft-switching [15]-[17]. However, this inevitably increases the voltage and current stresses on the switches. Some papers have proposed strategies to increase the efficiency of NIBB in the buck-boost mode. One such strategy involves decreasing the equivalent switching frequency [6], [12]. Wide band gap semiconductors (e.g. silicon carbide) have also been used for switching loss reduction. Some other papers solve the efficiency problem from the perspective of the modulation scheme. A novel modulation scheme to achieve a higher efficiency was proposed in [19]. However, the current stress, which is equal to the peak current value of the switches, is too high, which may result in overcurrent damage on the switches. Reference [7] attempts to decrease the current RMS value with leading edge modulation and a decrease in the switching frequency, which reduces the conduction and switching loss of the switches. However, only two types of modulation schemes (leading edge and trailing edge) were compared in [7]. The impact of a shifted phase is considered in [18]. However, it only focuses on efficiency maximization through ZVS, which, as previously discussed, inevitably increases current stress on the switches. In addition, without analytic inductor current expressions in all of the modulation schemes, the analysis of the efficiency in [18] is qualitative rather than quantitative. In this paper, a novel general phase-shift modulation scheme is proposed, with every input voltage, duty ratio and shifted phase taken into account. Then analytical expressions of the inductor current are derived accurately for different types of modulation schemes, presenting the switch current stress and converter efficiency. Both the current stress limitation and the efficiency optimization in the buck-boost mode are discussed from the perspective of modulation schemes. All of the other factors, such as the power stage and switching frequency, are fixed.

This paper focuses on designing an optimal modulation scheme, and achieving efficiency optimization and current stress limitation for a unidirectional two-switch NIBB in the buck-boost mode. In Section II, the basic input voltage range of the unidirectional NIBB in the buck-boost mode is introduced. Then, formulas are derived considering two degrees of freedom including the shifted phase and duty ratio. In Section III, a general phase-shift modulation is introduced. Based on this, the inductor current considering every duty ratio, shifted phase and input voltage is derived. In Section IV, the current stress of the switches, and the converter efficiency are analyzed in detail. Accordingly, by optimizing an objective function with inequality constraints, an offline design methodology of the modulation scheme for both converter efficiency optimization and current stress limitation is proposed. Efficiency can be optimized based on the premise of current stress limitation, which can be determined by the designers according to system requirements. In Section V, a novel optimal modulation scheme is presented, based on the design methodology, which provides the selection method for the NIBB converter parameters. The current stress limitation and efficiency optimization of the modulation scheme are experimentally validated on a 300V, 1.5kW NIBB prototype. Finally, some conclusions are presented in Section VI.

II. Operation Principle of the NIBB

A. Operation Range of the Buck-Boost Mode

A two-switch NIBB is shown in Fig. 1(b). In the asynchronous control, Q_1 and Q_2 can be controlled independently. The relationship between the input voltage and the output voltage is:

$$V_{\text{out}} = V_{\text{in}} \times \frac{d_1}{1-d_2} \tag{1}$$

where d_1 is the duty ratio of Q_1, and d_2 is the duty ratio of Q_2.

There are three operation modes for the NIBB. When the

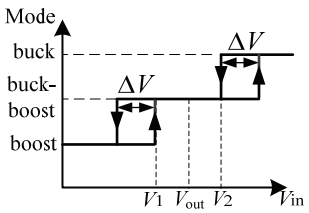


Fig. 2. Three operation modes in a NIBB.

input voltage V_{in} is much lower than V_{out}, the converter operates in the boost mode with Q_1 kept on and Q_2 operating in the PWM mode. When the input voltage is much higher than V_{out}, the converter operates in the buck mode with Q_2 kept off and Q_1 operating in the PWM mode. When V_{in} is close to V_{out}, the NIBB operates in the buck-boost mode where both Q_1 and Q_2 operate in the PWM mode. The relationships among the operation modes and the input voltage are shown in Fig. 2. As shown in [7], two hysteresis zones are needed between the two adjacent operation modes (i.e. the boost and buck-boost modes, and the buck-boost and buck modes) to avoid converter swing.

When the NIBB operates in the boost mode, the relationship between V_{in} and V_{out} is:

$$V_{out} = \frac{V_{in}}{1-d_2} \tag{2}$$

When the NIBB operates in the buck mode, the relationship between V_{in} and V_{out} is:

$$V_{out} = d_1 V_{in} \tag{3}$$

Because of the switching delay and the driver delay, there is a minimum pulse width for the power semiconductor, which is notated as d_{min}. The ranges of the duty ratios can be represented as:

$$\begin{cases} d_{min} \le d_1 \le 1-d_{min} \\ d_{min} \le d_2 \le 1-d_{min} \end{cases} \tag{4}$$

By substituting Eqns. (4) into (2) and (3), the maximum input voltage V_1 in the boost mode and the minimum input voltage V_2 in the buck mode are:

$$\begin{aligned} V_1 &= (1-d_{min})V_{out} \\ V_2 &= \frac{V_{out}}{1-d_{min}} \end{aligned} \tag{5}$$

Set ΔV as the hysteresis width. Then the input voltage range for the buck-boost mode can be presented by:

$$V_1 - \Delta V \le V_{in} \le V_2 + \Delta V \tag{6}$$

Define c as the ratio of the input voltage to the output voltage. Then c can be represented as:

$$\frac{V_1 - \Delta V}{V_{out}} \le c \le \frac{V_2 + \Delta V}{V_{out}} \tag{7}$$

B. Degrees of Freedom for the Modulation Scheme in the Buck-Boost Mode

Since only the buck-boost mode is considered in this paper, its control and modulation diagram are presented in Fig. 3. The PWM signals of Q_1 and Q_2 are generated by comparing the duty ratios d_1 and d_2 with two sawtooth carriers. Here, d_1 is set as a constant value while d_2 is determined by two PI controllers. The inductor current i_L and the output voltage V_{out} are sampled once per switching period. The outer-loop controller calculates the inductor current reference i_L^*, while the inner-loop controller regulates i_L to i_L^*. The controller design is not the focus of this paper. With a certain input and output voltage, the degrees of freedom for a modulation scheme are the shifted phase ratio Δp between the carriers of Q_1 and Q_2 and d_1. Various modulation schemes are represented by these two factors. Δp can arbitrarily vary between 0 and 1, where 1 means 2π for the shifted phase. The limitation on d_1 is derived as follows.

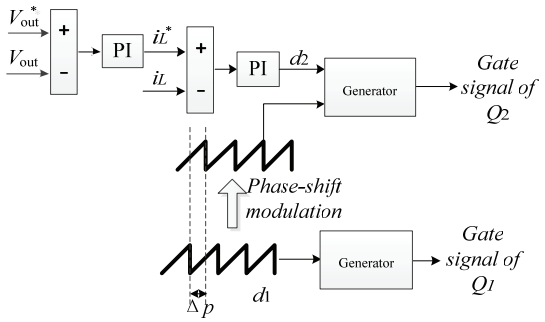


Fig. 3. Control and modulation diagram in the buck-boost mode.

Substituting Eqns. (1) and (5) into (6) yields:

$$1 - \frac{d_1}{1-d_{min}} - \frac{d_1 \Delta V}{V_{out}} \le d_2 \le 1 - (1-d_{min})d_1 + \frac{d_1 \Delta V}{V_{out}} \tag{8}$$

In order to guarantee operation over the full input voltage range mentioned in (6) in the buck-boost mode, the range of d_2 should meet the requirements in (8). Considering Eqns. (4) and (8), d_1 should satisfy:

$$\begin{cases} 1 - \frac{d_1}{1-d_{min}} - \frac{d_1 \Delta V}{V_{out}} \ge d_{min} \\ d_{min} \le d_1 \le 1-d_{min} \\ 1 - d_1(1-d_{min}) + \frac{d_1 \Delta V}{V_{out}} \le 1-d_{min} \end{cases} \tag{9}$$

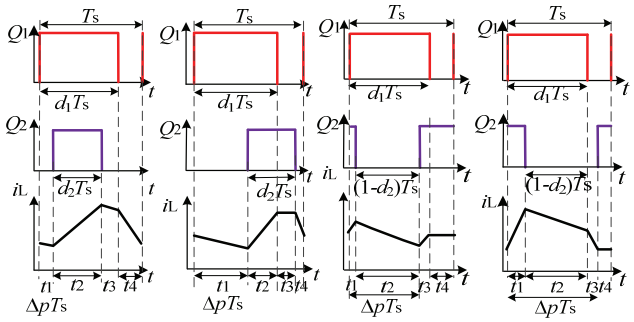
Therefore, the range of d_1 is derived as:

$$\max\left\{\frac{d_{min}V_{out}}{(1-d_{min})V_{out} - \Delta V}, d_{min}\right\} \le d_1 \le \min\left\{\frac{V_{out}(1-d_{min})^2}{V_{out} + \Delta V(1-d_{min})}, 1-d_{min}\right\} \tag{10}$$

As discussed above, with given values of d_{min}, V_{out} and ΔV, the range of d_1 should satisfy the requirements in Eq. (10), which are used as boundaries for optimization design in the following sections.

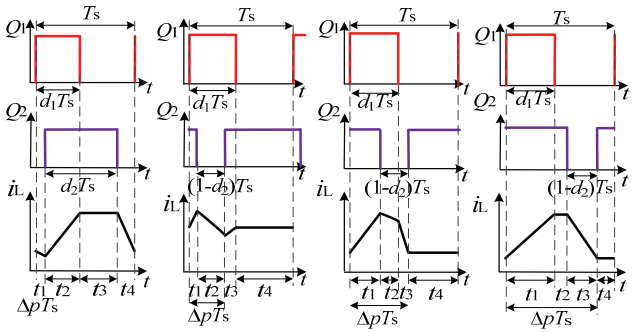
III. Analysis of a NIBB with Phase-Shift Modulation

The two control degrees of freedom d_1 and Δp can change to form different types of modulation schemes. With consideration



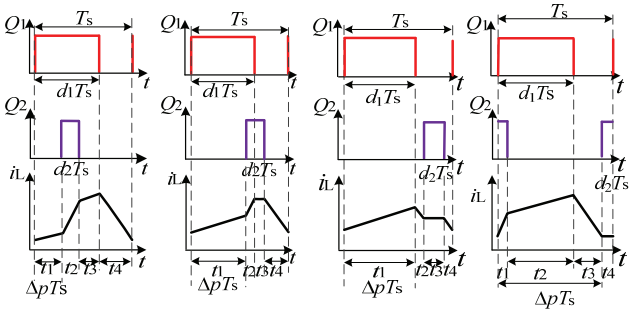
(a) $0\le\Delta p<d_1-d_2$. (b) $d_1-d_2\le\Delta p<1-d_2$. (c) $1-d_2\le\Delta p<d_1$. (d) $d_1\le\Delta p<1$.

Fig. 4. Gate signals and inductor current waveforms when $V_{in}<V_{out}$ and $d_1>d_2$.



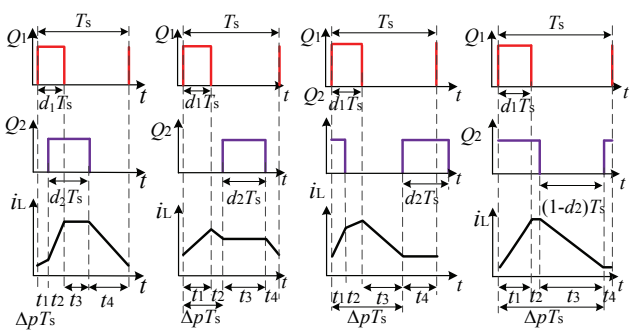
(a) $0\le\Delta p<1-d_2$. (b) $1-d_2\le\Delta p<d_1$. (c) $d_1\le\Delta p<1+d_1-d_2$. (d) $1+d_1-d_2\le\Delta p<1$.

Fig. 5. Gate signals and inductor current waveforms when $V_{in}<V_{out}$ and $d_1<d_2$.



(a) $0\le\Delta p<d_1-d_2$. (b) $d_1-d_2\le\Delta p<d_1$. (c) $d_1\le\Delta p<1-d_2$. (d) $1-d_2\le\Delta p<1$.

Fig. 6. Gate signals and inductor current waveforms when $V_{in}>V_{out}$ and $d_1>d_2$.



(a) $0\le\Delta p<d_1$. (b) $d_1\le\Delta p<1-d_2$. (c) $1-d_2\le\Delta p<1+d_1-d_2$. (d) $1+d_1-d_2\le\Delta p<1$.

Fig. 7. Gate signals and inductor current waveforms when $V_{in}>V_{out}$ and $d_1<d_2$.

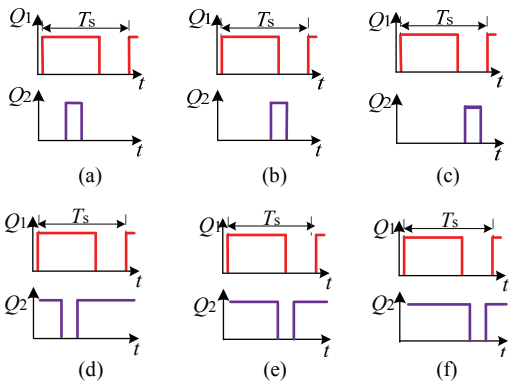


Fig. 8. Relative position between the two control signals in six PSTs.

TABLE I
RELATIONS AMONG THE 16 SITUATIONS AND SIX PSTS

	$V_{in}<V_{out}$, $d_1>d_2$ Fig. 4	$V_{in}<V_{out}$, $d_1<d_2$ Fig. 5	$V_{in}>V_{out}$, $d_1>d_2$ Fig. 6	$V_{in}>V_{out}$, $d_1<d_2$ Fig. 7
PST (1): Fig. 8(a)	Fig. 4(a)		Fig. 6(a)	
PST (2): Fig. 8(b)	Fig. 4(b)	Fig. 5(a)	Fig. 6(b)	Fig. 7(a)
PST (3): Fig. 8(d)	Fig. 4(c)	Fig. 5(b)		
PST (4): Fig. 8(c)			Fig. 6(c)	Fig. 7(b)
PST (5): Fig. 8(e)	Fig. 4(d)	Fig. 5(c)	Fig. 6(d)	Fig. 7(c)
PST (6): Fig. 8(f)		Fig. 5(d)		Fig. 7(d)

The characteristics for these six PSTs are as follows.
PST (1): $0\le\Delta p<d_1-d_2$, which appears only when $d_1>d_2$.
PST (2): $\min(d_1-d_2,0)\le\Delta p<\min(d_1,1-d_2)$.
PST (3): $1-d_2\le\Delta p<d_1$, which appears only when $V_{in}<V_{out}$.
PST (4): $d_1\le\Delta p<1-d_2$, which appears only when $V_{in}>V_{out}$.
PST (5): $\max(d_1,1-d_2)\le\Delta p<\min(1+d_1-d_2,1)$.
PST (6): $1+d_1-d_2\le\Delta p<1$, which appears only when $d_1<d_2$.

of the different types of modulation schemes, a general phase-shift modulation, which can be used for NIBB converter improvement, is introduced in this paper. In this section, different situations involving various input voltages, duty ratios and phase shift ratios are analyzed with this general phase-shift modulation.

A. Waveforms in Different Situations with Phase-shift Modulation

For the NIBB shown in Fig. 1(b), there are four states. The four states are: Q_1 and Q_2 are both on; Q_1 and Q_2 are both off; Q_1 is off and Q_2 is on; and Q_1 is on and Q_2 is off. The inductor current slopes for the four switching states can be calculated as:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t}=\frac{V_{in}}{L},\frac{\mathrm{d}i_L}{\mathrm{d}t}=-\frac{V_{out}}{L},\frac{\mathrm{d}i_L}{\mathrm{d}t}=0,\frac{\mathrm{d}i_L}{\mathrm{d}t}=\frac{V_{in}-V_{out}}{L} \tag{11}$$

Based on the above four inductor current slopes, inductor current waveforms in different situations in a switching period T_s are shown in Fig. 4 through Fig. 7, considering different input voltages and d_1. In each figure, inductor current waveforms with various phase-shift ratios are diagramed during four periods (i.e. t_1, t_2, t_3 and t_4).

In fact, the relative positions between the two control signals of Q_1 and Q_2 can be sorted into six phase-shift types (PST) as shown in Fig. 8. The above 16 situations can be grouped into these six PSTs, as shown in Table I.

B. Ampere-second Equivalent Principle

When Q_2 is off, the current flow of the inductor, as shown in Fig. 1(b), is expressed by:

$$i_{L1} = i_L \tag{12}$$

When Q_2 is on, the current flow of the inductor satisfies:

$$i_{L1} = 0 \tag{13}$$

In addtion, there is:

$$i_{L1} - i_o = C\frac{dV_{out}}{dt} \tag{14}$$

Assuming the time duration when Q_2 is kept off is t_{off} and the time duration when Q_2 is kept on is T_s - t_{off}. Equation (14) is integrated in a switching period, and the item in the right side is zero. Combining (12) and (13) yields:

$$\int_0^{T_s}(i_{L1} - i_o)dt = \int_0^{t_{off}} i_L dt - i_o T_s = \int_0^{T_s} C\frac{dV_{out}}{dt}dt = 0 \tag{15}$$

Therefore:

$$\int_0^{t_{off}} i_L dt = i_o T_s \tag{16}$$

When V_{out} is stable, the integral of i_L during t_{off} remains constant.

C. Derivation of the Inductor Current

i_1 is the inductor current at the rising edge of Q_1, i_3 is the inductor current at the falling edge of Q_1, i_2 is the inductor current at the rising edge of Q_2, and i_4 is the inductor current at the falling edge of Q_2. From Fig. 4 through Fig. 7, i_1 and i_2 are never higher than i_3 and i_4. The maximum inductor current is the higher among i_3 and i_4, while the minimum value is the lower among i_1 and i_2. The current stress, defined as the peak current of the switches, is equal to the maximum inductor current.

Fig. 9 shows an inductor current waveform in PST (1), which is only suitable when $d_1 > d_2$. The inductor currents in PST (1) are given by:

$$\begin{cases} i_2 - i_1 = \dfrac{(V_{in} - V_{out})\Delta p T_s}{L} \\ i_4 - i_2 = \dfrac{V_{in} d_2 T_s}{L} \\ i_1 - i_3 = -\dfrac{V_{out}(1-d_1)T_s}{L} \end{cases} \tag{17}$$

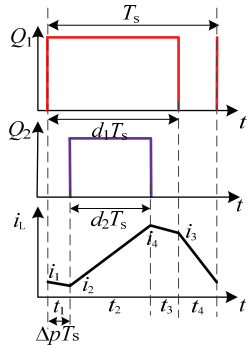


Fig. 9. Inductor current in PST (1).

According to the above ampere-second equivalent principle, the currents i_1, i_2, i_3 and i_4 can be derived by combining Eqns. (17) and (16):

$$\begin{cases} i_1 = \dfrac{V_{out}}{Rcd_1} + \dfrac{V_{out}T_s}{2Ld_1} + \dfrac{V_{out}T_s}{2L}(c^2+c+1)d_1 - \dfrac{V_{out}T_s}{L}(1+c) \\ \quad + \dfrac{V_{out}T_s}{L}(\dfrac{1}{d_1} - c)\Delta p \\ i_2 = \dfrac{V_{out}}{Rcd_1} + \dfrac{V_{out}T_s}{2Ld_1} + \dfrac{V_{out}T_s}{2L}(c^2+c+1)d_1 - \dfrac{V_{out}T_s}{L}(1+c) \\ \quad + \dfrac{V_{out}T_s}{L}\dfrac{1-d_1}{d_1}\Delta p \\ i_3 = \dfrac{V_{out}}{Rcd_1} + \dfrac{V_{out}T_s}{2Ld_1} + \dfrac{V_{out}T_s}{2L}(c^2+c-1)d_1 - \dfrac{V_{out}T_s}{L}c \\ \quad + \dfrac{V_{out}T_s}{L}(\dfrac{1}{d_1} - c)\Delta p \\ i_4 = \dfrac{V_{out}}{Rcd_1} + \dfrac{V_{out}T_s}{2Ld_1} + \dfrac{V_{out}T_s}{2L}(-c^2+c+1)d_1 - \dfrac{V_{out}T_s}{L} \\ \quad + \dfrac{V_{out}T_s}{L}\dfrac{1-d_1}{d_1}\Delta p \end{cases} \tag{18}$$

i_1, i_2, i_3 and i_4 from PST (2) to PST (6) are derived and given as follows.

PST (2): d_1-$d_2 \le \Delta p < \min(d_1, 1\text{-}d_2)$

$$\begin{cases} i_1 = \dfrac{V_{out}}{Rcd_1} - \dfrac{V_{out}T_s c d_1}{2L} + \dfrac{V_{out}T_s}{2L}(-\dfrac{\Delta p^2}{d_1} + 2\Delta p) \\ i_2 = \dfrac{V_{out}}{Rcd_1} - \dfrac{V_{out}T_s c d_1}{2L} + \dfrac{V_{out}T_s}{2L}(-\dfrac{\Delta p^2}{d_1} + 2c\Delta p) \\ i_3 = i_4 = \dfrac{V_{out}}{Rcd_1} + \dfrac{V_{out}T_s c d_1}{2L} - \dfrac{V_{out}T_s}{2L}\dfrac{\Delta p^2}{d_1} \end{cases} \tag{19}$$

PST (3): $1\text{-}d_2 \le \Delta p < d_1$ and $V_{in} < V_{out}$

$$\begin{cases} i_1 = i_3 = \dfrac{V_{out}}{Rcd_1} + \dfrac{(c^2+c)d_1 V_{out}T_s}{2L} - \dfrac{cV_{out}\Delta pT_s}{L} \\ i_2 = \dfrac{V_{out}}{Rcd_1} + \dfrac{(c-1)cd_1 V_{out}T_s}{2L} \\ i_4 = \dfrac{V_{out}}{Rcd_1} + \dfrac{(-c+1)cd_1 V_{out}T_s}{2L} \end{cases} \tag{20}$$

PST (4): $d_1 \le \Delta p < 1\text{-}d_2$ and $V_{in} > V_{out}$

$$\begin{cases} i_1 = \dfrac{V_{\text{out}}}{Rcd_1} - \dfrac{V_{\text{out}}T_{\text{s}}(c-1)d_1}{2L} \\ i_2 = i_4 = \dfrac{V_{\text{out}}}{Rcd_1} + \dfrac{V_{\text{out}}T_{\text{s}}(c+1)d_1}{2L} - \dfrac{V_{\text{out}}T_{\text{s}}\Delta p}{L} \\ i_3 = \dfrac{V_{\text{out}}}{Rcd_1} + \dfrac{V_{\text{out}}T_{\text{s}}(c-1)d_1}{2L} \end{cases} \tag{21}$$

PST (5): $\max(d_1, 1-d_2) \le \Delta p < \min(1+d_1-d_2, 1)$

$$\begin{cases} i_1 = i_2 = \dfrac{V_{\text{out}}}{Rcd_1} + \dfrac{V_{\text{out}}T_{\text{s}}d_1}{2L}(c^2+c+1) - \dfrac{V_{\text{out}}T_{\text{s}}}{2L}[2(c+1)\Delta p - \dfrac{\Delta p^2}{d_1}] \\ i_3 = \dfrac{V_{\text{out}}}{Rcd_1} + \dfrac{V_{\text{out}}T_{\text{s}}d_1}{2L}(c^2+c-1) - \dfrac{V_{\text{out}}T_{\text{s}}}{2L}[2c\Delta p - \dfrac{\Delta p^2}{d_1}] \\ i_4 = \dfrac{V_{\text{out}}}{Rcd_1} + \dfrac{V_{\text{out}}T_{\text{s}}d_1}{2L}(-c^2+c+1) - \dfrac{V_{\text{out}}T_{\text{s}}}{2L}[2\Delta p - \dfrac{\Delta p^2}{d_1}] \end{cases} \tag{22}$$

PST (6): $1+d_1-d_2 \le \Delta p < 1$ and $d_1 < d_2$

$$\begin{cases} i_1 = i_2 = \dfrac{V_{\text{out}}}{Rcd_1} - \dfrac{V_{\text{out}}cd_1T_{\text{s}}}{2L} \\ i_3 = i_4 = \dfrac{V_{\text{out}}}{Rcd_1} + \dfrac{V_{\text{out}}cd_1T_{\text{s}}}{2L} \end{cases} \tag{23}$$

In summary, the inductor current waveforms with various duty ratios, input voltages and shifted phases between the control signals of Q_1 and Q_2 are sorted into six PSTs based on the relative positions of the control signals. The analytical expressions of the inductor current are all obtained with the ampere-second equivalent principle. In the following section, the current stress and efficiency will be analyzed and calculated for current stress minimization and efficiency maximization over the entire input voltage range.

IV. Offline Design Methodology for the Optimal Modulation Scheme

Based on the inductor current derived in Section III, current stress minimization and efficiency maximization schemes for minimal current stress and maximal efficiency over the entire V_{in} range are proposed. Then, a design methodology for modulation schemes in the buck-boost mode to take both the current stress and efficiency into consideration is proposed. Current stress should be limited to protect switches to operate in the safe operating area. Efficiency is optimized in the buck-boost mode on premise of current stress limitation in this section.

A. Current Stress Minimization

With the current stress $i_{\text{stress}}(\Delta p, d_1, V_{\text{in}})$ derived above, the procedure for achieving the modulation scheme with minimal current stress $i_{\text{stress}}{}^*(V_{\text{in}})$ in the range of inequality (6) in the buck-boost mode is:

1) Configuration of d_1:

There are two control degrees of freedom including d_1 and Δp. First, d_1 can be randomly configured in the range of inequality (10).

2) Derivation of $\Delta p = f(d_1, V_{in})$ to Minimize Current Stress $i_{stress}(\Delta p, d_1, V_{in})$ for a Given d_1:

Take the situations in Fig. 4 as an example to analyze the current stress tendency with Δp increasing from 0 to 1 when d_1 and V_{in} are fixed. According to Table I, there are four PSTs (1), (2), (3) and (5) in this case.

When Δp changes from 0 to d_1-d_2, the situation belongs to PST (1), and the current stress is i_4. The relationship between i_4 and Δp is shown in the following equation. i_4 increases with an increasing Δp.

$$\frac{\partial i_4}{\partial \Delta p} = \frac{V_{out}T_s}{L}\frac{1-d_1}{d_1} > 0 \tag{24}$$

When Δp changes from d_1-d_2 to 1- d_2, the situation belongs to PST (2) and the current stress is i_3 or i_4(i_3= i_4). The relationship between the current stress and Δp is shown as follows. The current stress decreases with an increasing Δp.

$$\frac{\partial i_3}{\partial \Delta p} = \frac{\partial i_4}{\partial \Delta p} = -\frac{V_{out}T_s\Delta p}{Ld_1} < 0 \tag{25}$$

When Δp changes from 1- d_2 to d_1, the situation belongs to PST (3) and the current stress is i_4. The relationship between i_4 and Δp is given as follows. i_4 is constant with an increasing Δp.

$$\frac{\partial i_4}{\partial \Delta p} = 0 \tag{26}$$

When Δp changes from d_1 to 1, the situation belongs to PST (5) and the current stress is i_4. The relationship between i_4 and Δp is shown as the following inequality. i_4 increases with an increasing Δp.

$$\frac{\partial i_4}{\partial \Delta p} = -\frac{V_{\text{out}}T_{\text{s}}}{L}(1-\frac{\Delta p}{d_1}) \ge -\frac{V_{\text{out}}T_{\text{s}}}{L}(1-\frac{d_1}{d_1}) = 0 \tag{27}$$

Therefore, for given values of V_{in} and d_1, the current stress reaches its minimum in PST (3) when Δp changes from 0 to 1.

The current stress in other cases (as shown in Fig.5, Fig.6 and Fig.7) can be derived using the above procedure. For given value of V_{in} and d_1, the current stress reaches its minimum in PST (3) when $V_{\text{in}} < V_{\text{out}}$, and in PST (4) when $V_{\text{in}} > V_{\text{out}}$.

3) Determination of d_1 to Minimize Current Stress $i_{stress}{}^*(V_{in}) = min(i_{stress}(V_{in}, d_1))$:

As discussed above, considering the minimum current stress in PST (3) and PST (4), the minimized current stress under various values of d_1 can be obtained through an analysis of these two PSTs. For the current stress in PST (3), the derivation of the current stress with respect to d_1 is represented as:

$$\begin{aligned} \frac{\partial i_4}{\partial d_1} &= -\frac{V_{\text{out}}}{Rcd_1{}^2} + \frac{(-c+1)cV_{\text{out}}T_{\text{s}}}{2L} \\ &= -\frac{1}{d_1}(\frac{V_{\text{out}}}{Rcd_1} - \frac{(-c+1)cd_1V_{\text{out}}T_{\text{s}}}{2L}) = -\frac{i_2}{d_1} \end{aligned} \tag{28}$$

TABLE II
(D_1, ΔP) FOR CURRENT STRESS MINIMIZATION

	d_1	Δp	Current stress i_{stress}*(V_{in})
$V_{in}<V_{out}$	$\min\{\frac{V_{out}(1-d_{min})^2}{V_{out}+\Delta V(1-d_{min})}, 1-d_{min}\}$	$1\text{-}d_2 \le \Delta p < d_1$	$\frac{V_{out}}{Rcd_1}+\frac{(-c+1)cd_1V_{out}T_s}{2L}$
$V_{in}\ge V_{out}$		$d_1 \le \Delta p < 1\text{-}d_2$	$\frac{V_{out}}{Rcd_1}+\frac{V_{out}T_s(c-1)d_1}{2L}$

For the unidirectional NIBB, i_1 i_2 i_3 $i_4 \ge 0$. Therefore, $\partial i_4/\partial d_1 \le 0$. $i_{stress}(d_1)$ decreases with an increasing d_1. Similarly, the current stress in PST (4) when $V_{in} > V_{out}$ can also be analyzed.

It can be concluded that over the entire range of V_{in}, the current stress reaches its minimum value in PST (3) when $V_{in} < V_{out}$ or in PST (4) when $V_{in} > V_{out}$. Δp for the minimum current stress with a given d_1 can be obtained with consideration of these two PSTs. In terms of the freedom of d_1, based on Eq. (28), it should be configured as the maximum value in the range in Eq. (10). Eventually, the two degrees of freedom (d_1 and Δp) for current stress minimization i_{stress}*, where each V_{in} can be obtained as listed in Table II.

B. Efficiency Maximization

A model calculating the power loss is needed to obtain the efficiency. The power losses of the NIBB mainly consist of the inductor loss, and the conduction and switching losses of the power semiconductors. The impact of the other power losses (e.g. auxiliary power supply loss and PCB copper trace loss) are negligible for various modulation schemes and input voltages.

The inductor currents i_1, i_2, i_3 and i_4 shown in Fig. 9(a) are equal to the turn-on and turn-off currents of Q_1 and Q_2, which impacts the switching losses. The power semiconductors are approximated at the conduction state as resistors. The RMS value of the inductor current, which impacts the conduction loss of the power semiconductors and inductor loss, can also be obtained with i_1, i_2, i_3 and i_4. Therefore, the total power loss of the NIBB is highly affect by i_1, i_2, i_3 and i_4.

1) Efficiency Calculation:

a) Inductor Losses

As for the losses of the inductor, according to test results [20] - [22], the core loss of the inductor can be obtained by:

$$P_{core} = C_m f_s^{\alpha} B^{\beta} = f_{core}(f_s, i_{Lac}) \tag{29}$$

where B is the maximum magnet density of the AC component, and f_s is the magnet density frequency of the AC component, which is also the switching frequency. C_m, α and β can be obtained by curve fittings based on experimental results.

R_{Lac} and R_{Ldc} are the AC resistance and DC resistance of the winding, respectively. The copper loss can be represented as:

$$\begin{cases} P_{copper} = P_{copper\_ac} + P_{copper\_dc} \\ P_{copper\_ac} = i_{Lac\_rms}^{\ 2} \times R_{Lac} \\ P_{copper\_dc} = i_{Ldc}^{\ 2} \times R_{Ldc} \end{cases} \tag{30}$$

where:

$$\begin{cases} i_{Ldc} = \dfrac{i_o}{1-d_2} \\ i_{Lac\_rms} = \sqrt{\dfrac{\int_{T_s}(i_L - i_{Ldc})^2 \,\mathrm{d}t}{T_s}} \end{cases} \tag{31}$$

b) Switching Losses of Power Semiconductors

There are two kinds of power semiconductors in the NIBB, including two diodes and two active switches. Switching losses exist during the turn-on and turn-off of Q_1 and Q_2.

When Q_1 turns on, Q_1 commutates with Q_{SR1}, resulting in turn-on loss of Q_1 and turn-off loss of Q_{SR1}. These losses can be presented by a function of i_1:

$$P_{on1} = P_{on\_Q_1} + P_{off\_Q_{SR1}} = \frac{f_{on}(i_1 V_{in})}{T_s} \tag{32}$$

When Q_1 turns off, there is only the turn-off loss of Q_1 since the turn-on loss of the diode is negligible. It can be calculated by:

$$P_{off1} = P_{off\_Q_1} = \frac{f_{off}(i_3 V_{in})}{T_s} \tag{33}$$

where $f_{on}(iV)$ is the total turn-on loss and $f_{off}(iV)$ is the total turn-off loss relating to current and voltage of Q_1 (i.e. V_{in}). f_{on} and f_{off} can be obtained by the following steps.

(1) Collect the switching data of the power semiconductor through double pulse tests under different load currents and dc voltages.

(2) Calculate the turn-on and turn-off losses by integrating the product of switching current and voltage during switching transients.

(3) Obtain $f_{on}(iV)$ and $f_{off}(iV)$ through curve fitting.

When Q_2 turns on, Q_2 commutates with Q_{SR2}, resulting in the turn-on losses of Q_2 and the turn-off losses of Q_{SR2}. They can be calculated by:

$$P_{on2} = P_{on\_Q_2} + P_{off\_Q_{SR2}} = \frac{f_{on}(i_2 V_{out})}{T_s} \tag{34}$$

When Q_2 turns off, only the turn-off loss of Q_2 exists. This loss can be represented as:

$$P_{\text{off2}} = \frac{f_{\text{off}}(i_4 V_{\text{out}})}{T_s} \tag{35}$$

c) Conduction Losses of Power Semiconductors

The RMS value of the conduction current on the power semiconductors is required for the conduction loss calculation. Taking the situation in Fig. 9 as an example, the RMS current values of Q_1 and Q_{SR1} are:

$$\begin{cases} i_{\text{rms\_Q}_1}{}^2 = (\frac{(i_1+i_2)^2}{4} + \frac{(i_1-i_2)^2}{12}) \times \frac{t_1}{T_s} \\ +(\frac{(i_4+i_2)^2}{4} + \frac{(i_4-i_2)^2}{12}) \times \frac{t_2}{T_s} + (\frac{(i_4+i_3)^2}{4} + \frac{(i_4-i_3)^2}{12}) \times \frac{t_3}{T_s} \\ i_{\text{rms\_Q}_{\text{SR1}}}{}^2 = (\frac{(i_1+i_3)^2}{4} + \frac{(i_1-i_3)^2}{12}) \times \frac{t_4}{T_s} \end{cases} \tag{36}$$

Then, the conduction losses of Q_1 and Q_{SR1} are:

$$\begin{aligned} P_{\text{conduction\_Q}_1} &= U_{\text{on\_Q}_1} i_{\text{rms\_Q}_1} \\ P_{\text{conduction\_Q}_{\text{SR1}}} &= U_{\text{on\_Q}_{\text{SR1}}} i_{\text{rms\_Q}_{\text{SR1}}} \end{aligned} \tag{37}$$

Where $U_{\text{on\_}Q1}$ and $U_{\text{on\_}QSR1}$ are the conduction voltage on Q_1 and Q_{SR1}. They are related to the current on Q_1 and Q_{SR1} ($i_{\text{rms\_Q1}}$ and $i_{\text{rms\_QSR1}}$) and can be achieved by experiments and curve fittings. The conduction losses of Q_2 and Q_{SR2} are the same as those of Q_1 and Q_{SR1}.

d) Efficiency Calculation

The total loss can be derived by:

$$\begin{aligned} P_{losses} = {} & P_{core} + P_{copper} + P_{\text{on1}} + P_{\text{off1}} + P_{\text{on2}} + P_{\text{off2}} + P_{\text{conduction\_Q}_1} \\ & + P_{\text{conduction\_Q}_{\text{SR1}}} + P_{\text{conduction\_Q}_2} + P_{\text{conduction\_Q}_{\text{SR2}}} \end{aligned} \tag{38}$$

Thus, the efficiency can be represented as:

$$\eta = P_{out} \Big/ (P_{out} + P_{losses}) \tag{39}$$

In terms of the equations (18)-(23) given in Section III-C, even with the same $V_{\text{in}}(c)$, the inductor current waveforms change with the PSTs (i.e. various d_1 and Δp), resulting in different efficiencies. The efficiency $\eta(d_1,\Delta p)$ can be calculated by substituting the inductor current given in equations (18)-(23) into equations (29)-(39). Then, considering efficiency maximization, d_1 and Δp can be obtained with the given V_{in}.

2) Objective Function of Efficiency Over the Entire Range of V_{in} and Efficiency Maximization:

V_{in} in the range in Eq. (6) can be discretized into n steps as $V_{\text{in}}(1)$, $V_{\text{in}}(2)$,…, $V_{\text{in}}(\text{n})$. The efficiency in each step can be calculated as $\eta_1(x)$, $\eta_2(x)$,…, $\eta_{\text{n}}(x)$, where x refers to (d_1 and Δp).

The efficiency functions $\eta_{\text{i}}(x)(i=1,2,\ldots,n)$ with different input voltages V_{in} are different from each other and can be optimized with a particular $x_1, x_2 \ldots, x_{\text{n}}$ shown in Eq. (40), as analyzed above.

$$x_i = \arg\max \eta_i(x) \quad x=(d_1,\Delta p) \tag{40}$$

Total efficiency optimization with two control freedom degrees (d_1 and the shifted phase angle Δp) over the entire range of V_{in} is derived as a multi-objective optimization, as shown in Eq. (41).

$$\begin{cases} \max(\eta_1(x), \eta_2(x), ..., \eta_{\text{n}}(x)) \\ \text{subject to} \\ x \in E, E = \{(d_1,\Delta p) \in R^2 \mid 0 \le \Delta p \le 1, d_1 \text{ in Eq.(10)}\} \end{cases} \tag{41}$$

To turn this multi-objective optimization into a single-objective optimization, an objective function of efficiency is obtained by a linear weighted summation algorithm as follows.

Step 1: discretize V_{in} in the range in Eq. (6) into n steps as $V_{\text{in}}(i)$, where $i = 1{:}n$. The efficiency at $V_{\text{in}}(i)$ is derived as $\eta_{\text{i}}(x)$, where x refers to (d_1, Δp). For every $\eta_{\text{i}}(x)$ (i=1,…,n), calculate $\eta_{\text{i}}(x_{\text{j}})$ (j=1,…,n).

Step 2: calculate the bias $\delta_{\text{ij}} = \eta_{\text{i}}(x_{\text{i}}) - \eta_{\text{i}}(x_{\text{j}})$.

Step 3: calculate the average bias m_{i} by

$$m_{\text{i}} = \sum_{j=1}^{n} \delta_{\text{ij}} \Big/ n \tag{42}$$

Step 4: sort m_{i}:

$$m_{\text{s1}} \ge m_{\text{s2}} \ge \ldots \ge m_{\text{sn}} \tag{43}$$

The weight coefficients can be represented as:

$$\lambda_{\text{i}} = m_{\text{i}} \Big/ \sum_{i=1}^{n} m_{\text{i}}, \quad i=1,2,...,n \tag{44}$$

Correspondingly, $\lambda_{\text{s1}} \ge \lambda_{\text{s2}} \ge \ldots \ge \lambda_{\text{sn}}$. Then, define the objective function of the efficiency over the entire V_{in} range as shown in the following formula.

$$\eta_{\text{goal}}(x) = \lambda_{\text{s1}}\eta_{\text{sn}}(x) + \lambda_{\text{s2}}\eta_{\text{s(n-1)}}(x) + \cdots + \lambda_{\text{sn}}\eta_{\text{s1}}(x) \tag{45}$$

Finally, considering η_{goal} as the objective function of efficiency over the entire range of V_{in}, x_{goal} (i.e. d_1 and Δp) can be obtained through the maximization of $\eta_{\text{goal}}(x)$.

C. Proposed Design Methodology of Optimal Modulation Schemes

It is feasible to design a modulation scheme achieving the current stress minimization as analyzed in Section IV-A or the efficiency maximization as analyzed in Section IV-B over the entire input voltage range in the buck-boost mode. However, neither of them can achieve both goals (i.e. efficiency maximization and current stress minimization) at the same time.

A design methodology for the modulation schemes is proposed to take both efficiency and current stress into account. Efficiency is optimized in the buck-boost mode based on the premise of current stress limitation by maximizing the objective function with n inequality constraints shown in Eq. (46). The n inequality constraints are for the current stress limitation while the objective function is for efficiency

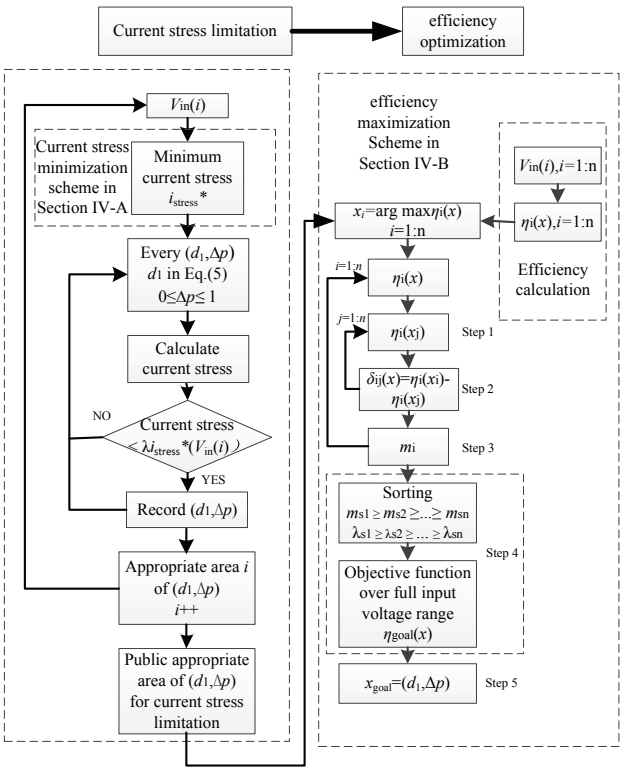


Fig. 10. Flow chart of the proposed design methodology.

optimization.

$$\begin{cases} \max \eta_{goal}(x) \\ \text{subject to} \\ x \in C, C = \{(d_1,\Delta p) \in E \mid i_{stress}(d_1,\Delta p,V_{in}) \le \lambda i_{stress}^{*}(V_{in})\} \end{cases} \quad (46)$$

where i_{stress}*(V_{in}) is the minimum current stress with V_{in} derived in Table II. In addition, i_{stress}(d_1, Δp, V_{in}) is the current stress function of d_1, Δp with V_{in} derived by Eq. (18)-(23). λ, the limitation ratio for the current stress, should be determined by the designers according to their requirements in terms of current stress limitation. λ is always greater than 1. The higher the requirements of the current stress limitation, the closer λ should be to 1.

The whole process for the proposed design methodology in Fig. 10 is divided into two steps.

(1) Limit the current stress based on the analysis in Section IV-A. The range of (d_1, Δp), meeting that the current stress is lower than a defined threshold λi_{stress}* ($V_{in}(i)$) (e.g. λ = 1.1) for every $V_{in}(i)$ can be solved.

(2) Maximize the efficiency based on the discussion in Section IV-B, while (d_1, Δp) should be in the range obtained in step (1).

V. Simulations and Experimental Verifications

In order to verify the proposed design methodology, a prototype with an output voltage of 300 V is built, as shown in Fig. 11. FF150R12MS4G IGBTs are used as the active switches and diodes. A DSP320F2812 is applied as the DSP chip of the control board, while a CPLD is used for hardware protection. A power analyzer YOKOGAWA-WT1800 is used to measure the efficiency of the prototype.

TABLE III
Parameters of the NIBB in the Buck-Boost Mode

parameters	values
Input voltage V_{in}	280 V~320 V
Output voltage V_{out}	300 V
Output power	1.5 kW
Inductance L	1 mH
Equivalent AC resistor R_{Lac}	0.2 Ω
Equivalent DC resistor R_{Ldc}	0.733 Ω
Load resistor R	60 Ω
Output capacitor C	420 μF
Switching period T_s	50 μs
d_{min}	0.05
ΔV	5 V
λ	1.1

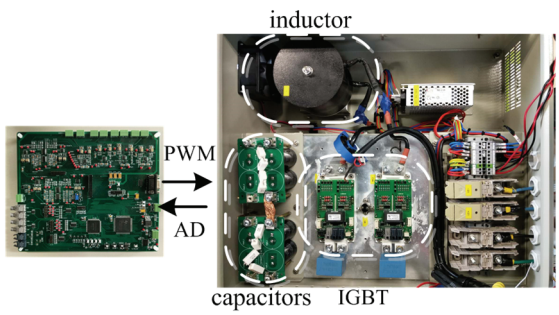


Fig. 11. Prototype of a NIBB.

The parameters of the prototype are given in Table III. The performance of the NIBB in the buck-boost mode is the focus of this paper, and the input voltage varies from 280 V to 320 V. d_1 changes from 0.054 to 0.88 as calculated by an inequality, while Δp varies from 0 to 1. The discretization step size of d_1, Δp and V_{in} are 0.01, 0.01 and 1 V, respectively. The parameters d_{min} and ΔV are introduced in Section II. λ is the ratio between the current stress threshold and the minimal current stress, as introduced in Section IV-C. It can be determined by the designers according to the requirements in terms of current stress limitation.

A. Simulations and Modulation Scheme Design

1) Simulation Verifications for Inductor Current Analyses and Formulations:

Take PST (1) and PST (3) as examples to verify the inductor current analyses and formulations in Section III with simulation results. V_{in} = 280 V, d_1 = 0.85. In Fig. 12, Δp = 0, and it belongs to PST (1). A simulation inductor current waveform shown by the blue line in Fig. 12 is almost the same as the one obtained by analyses and calculations shown

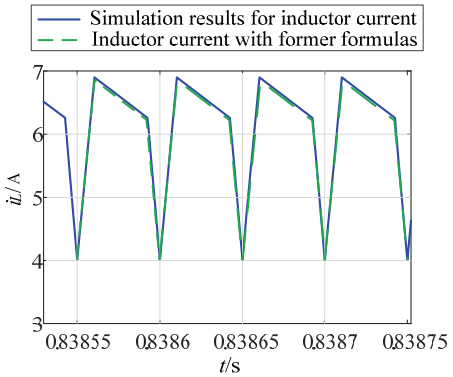


Fig. 12. Simulation verification for inductor current analyses in PST (1).

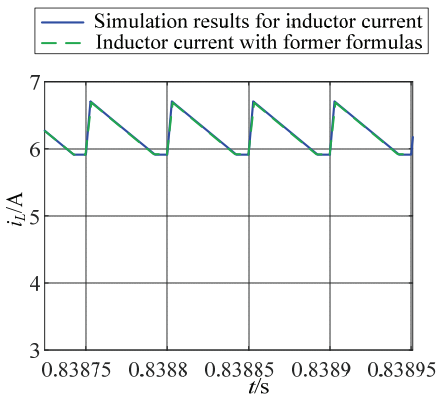


Fig. 13. Simulation verification for inductor current analyses in PST (3).

as the green dotted line. Similarly, in Fig. 13, $\Delta p = d_1$, and it belongs to PST (3). The shape and value of the simulation inductor current shown as the blue line in Fig. 13 are almost the same as the inductor current waveform by analyses and calculations shown as the green dotted line.

2) Current Stress Limitation:

Firstly, with a fixed V_{in}, 280 V for instance, i_{stress}* can be achieved by the current stress minimization scheme in Section IV-A. According to the current stress minimization scheme in Section IV-A, i_{stress}* is obtained when d_1 reaches its maximum and Δp is in PST (3). As shown in the simulation results shown in Fig. 14, the minimum current stress i_{stress}* can be achieved when $d_1 = 0.88$ and $\Delta p = 0.8446$, which is between 1-d_2 and d_1. i_{stress}* is 6.5 A when $V_{in} = 280$ V. The horizontal plane is the current stress threshold which is equal to λi_{stress}* = 1.1 i_{stress}*.

Then, the range of (d_1, Δp), meeting that the current stress limitation, is lower than 1.1 i_{stress}*, when V_{in} is fixed to 280 V is obtained as shown in the yellow area in Fig. 15.

Similarly, as shown Fig. 15, when V_{in} varies inside the scope of the buck-boost mode, every range of (d_1, Δp) under various values of V_{in} considering the current stress limitation can be obtained. The intersection area of these ranges, where the current stress is lower than the threshold over the entire

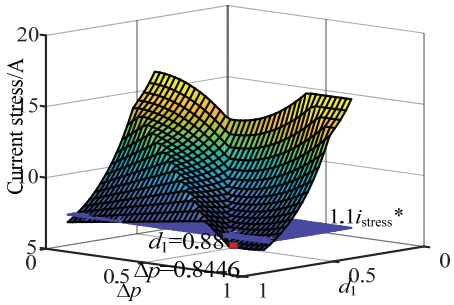


Fig. 14. Current stress varying with the shifted phase and d_1 when $V_{in} = 280$ V.

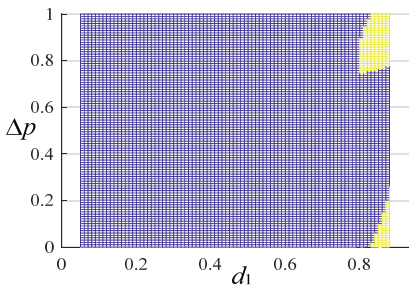


Fig. 15. Appropriate area of (d_1, Δp) for limited current stress when V_{in} =280 V.

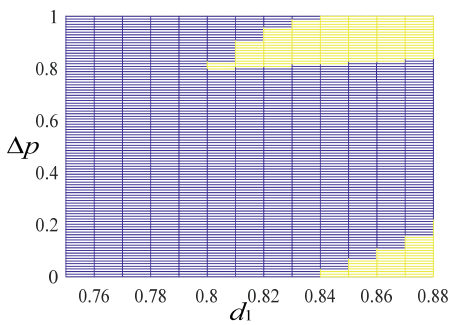


Fig. 16. Intersection area of (d_1, Δp) for limited current stress over the entire range of V_{in}.

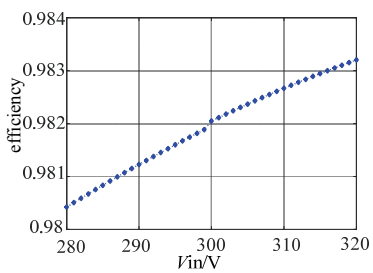


Fig. 17. Optimized efficiency when V_{in} varies.

range of V_{in} in the buck-boost mode, is shown as the yellow area in Fig. 16, where the efficiency optimization is conducted.

3) Efficiency Optimization:

V_{in} varies from 280 V to 320 V and can be divided into 41 steps with a step size of 1 V. Based on the analysis in Section IV-B, the maximum η_1, η_2, …, η_{41} in the range given in Fig. 16 is shown in Fig. 17.

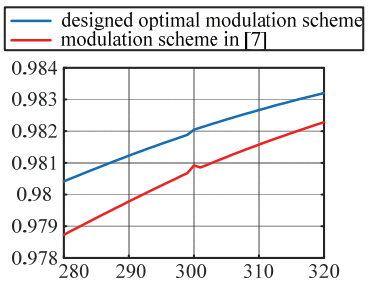


Fig. 18. Simulation results of the efficiencies of two optimization schemes.

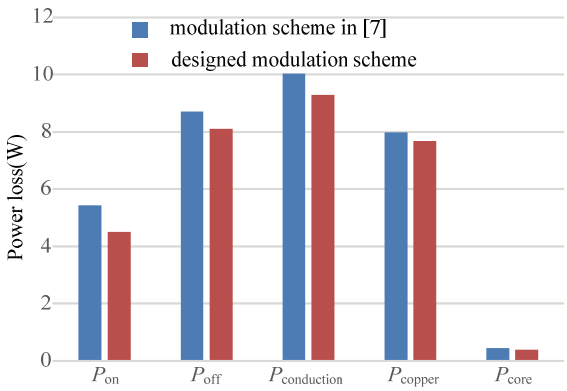


Fig. 19. Simulation comparisons of the efficiency of each part for the two optimization schemes.

With the same procedure used in Section IV-B, the optimized modulation parameter (d_1, Δp) considering both current stress limitation and efficiency optimization is (0.88, 0.99).

4) Simulation Comparisons of the Efficiencies between the Designed Modulation Scheme and the Modulation Scheme in [7]:

Power losses and efficiency can be calculated with the mathematical formulations (29)-(39) for loss evaluation. Efficiency with the designed optimal modulation scheme is compared with that with the modulation scheme in reference [7], which obtained the highest efficiency among previous studies, as shown in Fig. 18. A higher efficiency for an NIBB in the buck-boost mode is achieved with the designed optimal modulation scheme. Then, taking V_{in} = 280 V as an example, comparisons of the simulation losses for each part between the designed modulation scheme in this paper and the one in [7] are shown in Fig. 19. Power losses in each part are reduced with the modulation scheme designed in this paper.

B. Experimental Verifications

1) Experimental Verifications for the Inductor Current Analyses and Formulations:

In the first step, experiments are conducted to validate the formulations and analyses on inductor current waveforms with given values of V_{in} and d_1. V_{in} is 280 V, which is lower than V_{out} = 300 V. d_1 is 0.85, which is larger than d_2.

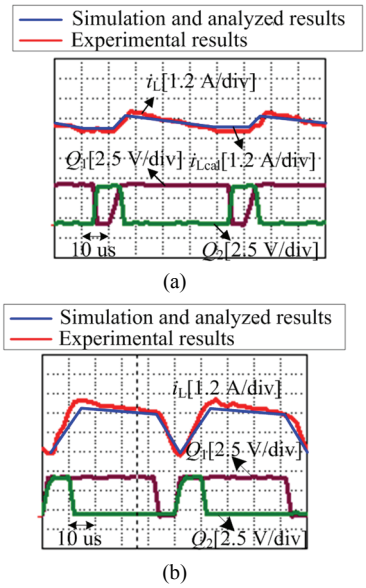


Fig. 20. Experimental verifications for the inductor current analyses in: PST (1); PST (3).

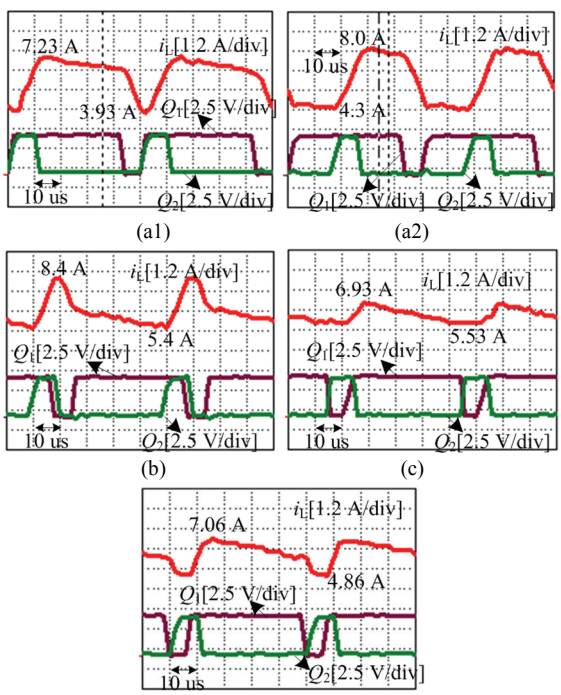
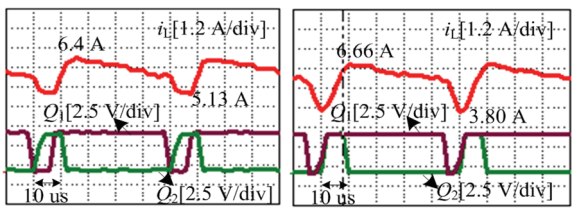


Fig. 21. Inductor current waveforms of experiments. (a1) Phase-shift situation in Fig. 4(a); shifted phase is 0. (a2) Phase-shift situation in Fig. 4(a); shifted phase is 0.36. (b) Phase-shift situation in Fig. 4(b); shifted phase is 0.80. (c) Phase-shift situation in Fig. 4(c); shifted phase is 0.83. (d) Phase-shift situation in Fig. 4(d); shifted phase is 0.93.

Experimental verifications for the inductor current analyses and formulas in PST (1) and PST (3) are shown in Fig. 20(a) and (b). The shape and value of the experimental inductor current waveforms shown as the red lines in these figures are consistent with the inductor current waveforms by analyses and simulations shown as the blue lines.

TABLE IV
CURRENT STRESS WITH VARIOUS VALUES OF D_1

	d_1= 0.80	d_1= 0.85	d_1= 0.88
V_{in}=280 V	7.29 A	6.93 A	6.33 A
V_{in}=320 V	6.70 A	6.06 A	5.67 A



(a) (b)

Fig. 22. Inductor current waveforms of modulation schemes with two design methods. (a) Modulation scheme designed with current stress minimization. (b) Designed optimal modulation scheme.

With regard to the verifications for the current stress analyses, four types of the experimental results are shown in Fig. 21, corresponding to PSTs in Fig. 4(a), (b), (c) and (d), respectively. The trend of the current stress follows the conclusion provided in section IV-A. The current stress reaches its minimum in PST (3), as shown in Fig. 4(c). This satisfies the conclusion on the minimum current stress in Section IV-A.

For the current stress in PST (3), d_1 is varied and the relationship between the current stress and d_1 is validated. Experimental results for the current stress with various values of d_1 when V_{in} = 280 V and 320 V are shown in Table IV. The current stress decreases with d_1 increasing for every V_{in}, which satisfies the conclusion on the minimum current stress in Section IV-A.

2) Current Stress Limitation Verifications with the Designed Modulation Scheme

Then, experiments are conducted to verify that the inductor current stress with the designed optimal modulation scheme meets the current stress limitation as stated in Section IV-C. With a fixed input voltage, Fig. 22 shows experimental inductor current waveforms with the designed modulation and one with minimal current stress. The inductor current shown in Fig. 22(a) is obtained with the modulation scheme designed by the current stress minimization method in Section IV-A, with which the minimal current stress among all types of modulation schemes is obtained. The inductor current shown in Fig. 22(b) is obtained with the designed optimal modulation scheme. The current stress, equal to the maximum in the inductor's current waveform with the designed modulation scheme, is similar to the minimal current stress shown in Fig. 22(a).

In Fig. 23, over the entire input voltage range in the buck-boost mode, the current stress with the designed modulation scheme is smaller than the limited current stress λi_{stress}* = 1.1i_{stress}*. The designed modulation scheme meets the current stress limitation.

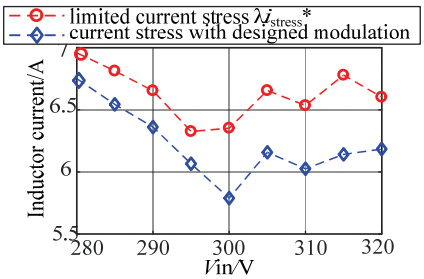


Fig. 23. Current stress limitation with the proposed optimization scheme.

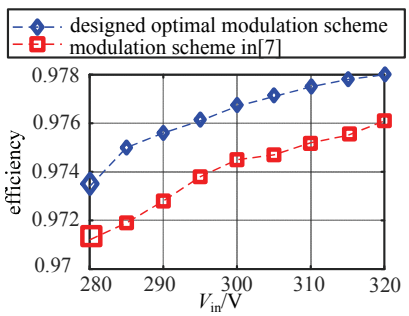
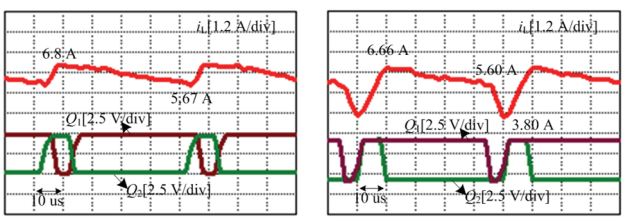


Fig. 24. Experimental results showing the efficiency of two optimization schemes.



(a) (b)

Fig. 25. Experimental inductor current waveforms with the: (a) Modulation scheme in [7]. (b) Designed modulation scheme.

3) Efficiency Optimization Verifications with the Designed Modulation Scheme

Finally, the efficiency with the designed optimal modulation scheme is compared with the efficiency with the modulation scheme in reference [7], which obtained the highest efficiency among previous studies, as shown in Fig. 24. A higher efficiency for an NIBB at the buck-boost mode is achieved with the designed optimal modulation scheme. Despite of the small efficiency improvement, the fact that the designed modulation scheme with the proposed design method achieve the optimal efficiency among all of the existing modulation schemes is verified.

With regard to the loss comparisons for each part, take V_{in} = 280 V as an example. Because the power losses for each part cannot be easily measured directly by experimental instruments, they are calculated by substituting experimental inductor current waveforms obtained with the designed modulation scheme and the one in [7] into the loss models in (29) - (37). Fig. 25 shows experimental inductor current waveforms with the designed modulation scheme and the one

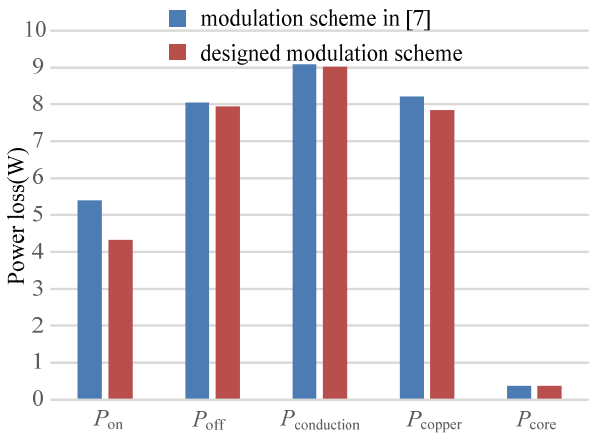


Fig. 26. Experimental power losses comparisons between two modulation schemes.

in [7], which achieves i_1, i_2, i_3 and i_4. By substituting them into loss models, the power losses for each part can be obtained and shown in Fig. 26. The power losses for each part with the designed modulation scheme are smaller than those with the modulation scheme in [7]. The same conclusions in terms of power losses and efficiency as the former simulations and loss calculations shown in Fig. 18 and Fig. 19 are obtained. In addition, the shapes of experimental efficiency and power loss results in Fig. 24 and Fig. 26 are consistent with those of the simulation and calculated results in Fig. 18 and Fig. 19. This validates the provided mathematical formulations for the loss evaluation.

Efficiency optimization and current stress limitation over the entire input voltage range of the buck-boost mode are both realized with the designed optimal modulation scheme by the proposed design methodology.

VI. Conclusion

Non-inverting Buck-Boost converters have been extensively used in wide-input-voltage-range applications. To overcome the drawback of low-efficiency in the buck-boost mode, this paper tries to reduce the total loss through improving the modulation scheme. A general phase-shift modulation scheme for a NIBB is proposed in this paper. Furthermore, an offline design method for the optimal modulation optimization scheme over the entire input voltage range at the buck-boost mode is provided, with converter efficiency optimized and switch current stress limited. The proposed design method has three merits.

1) The general phase-shift modulation considers all of the possible situations of the switching states, which is suitable for both two-switch and four-switch NIBBs.
2) Analytic current expressions for all of the possible scenarios are derived completely so the current stress and the converter efficiency can be analyzed and calculated in detail.
3) With the designed optimal modulation scheme, both efficiency optimization and current stress limitation over the entire input voltage range are realized.

The feasibility and validity of the whole design process have been confirmed by experimental results.

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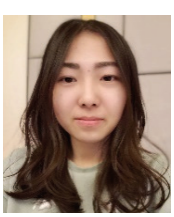

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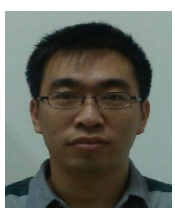

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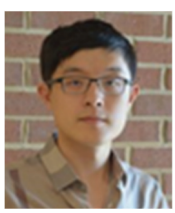

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