JPE 19-5-7

https://doi.org/10.6113/JPE.2019.19.5.1133
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Capacitors Energy Strategy Based Cascaded H-Bridge Converter for DC Port Failures

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Abstract

In this paper, a capacitors energy strategy based Cascaded H-bridge Converter (CHBC) for steady DC link voltage is proposed, which allow the CHBC to work while DC power fails. The topology of the CHBC is analyzed to construct the proposed strategy. The capacitors energy strategy is deduced based on the principle that the DC link voltage should be steady, the switch state should be smooth and the switch frequency should be normal. Experiments based on a three-module prototype, including static experiment, start experiment and step change experiment, proves the correctness of the strategy. They also verified the excellent fault tolerance ability and good dynamic performance of the proposed strategy.

Key words: CHBC, Capacitors energy strategy, Steady DC link voltage

I. INTRODUCTION

Fault-tolerant is essential in the multilevel back-to-back converters since it is reported that 21% of the failures of converter are due to semiconductor device faults [7]. In addition, based a survey which included 200 products from 80 companies, 34% of the responders selected semiconductor power devices as the most fragile components [8]. Thus, strict reliability and safety rules are required in power systems [9]. The short-circuit faults and open-circuit faults are the two main fault categories of power electronics components. These faults result in various faults in multilevel back-to-back converter. When a power electronics component is broken due to a short-circuit, it becomes unable to output resulting in a DC link voltage unbalance.

With increasing application needs in the high voltage field, the cascaded H-bridge converter (CHBC) is widely used [1]-[3]. Fig. 1 illustrates a back to back converter that uses a CHBC as its output. In this converter, the rectifier transforms power from AC to DC, and the CHBC inverts DC to AC as its output. The output AC is relatively high, while its frequency and amplitude are controlled. Since all of the modules of the CHBC are connected with each other, a fault in one module may cause the output to breakdown [4]. Among the various faults, a rectifier component fault prevents the rectifier from constantly providing DC power for the corresponding module, which renders the whole module useless [5]. To generate a normal output voltage, typical modules bear a higher voltage when some of the modules breakdown. As a result, they become even more fault-prone than usual. Moreover, the rectifier failure module produces distortion and harmonic in the output voltage, which disturbs the user of the device [6].

To achieve to goals of fault-tolerant control, auxiliary component, circuits and legs are added to conventional converter topologies. The authors of [13] presented a single-phase multi-level inverter topology for PV applications, which added auxiliary components on the output line of the converter. The topology has the capability of fault-tolerant operation in case of single switch open faults. Similarity, the authors of [14] added auxiliary components on the neutral-point. In addition, the auxiliary circuits are also widely used in the fault-tolerant of multi-level converters. The authors of [15] presented a multilevel active-clamped converter with an auxiliary circuit, which considers both open-circuit and short- circuit faults. Additionally, [16]-[18] presented a variety of auxiliary circuits for the voltage balance of multi-level converters. However, they are not directly applied to the fault-tolerant control. They demonstrated efficient voltage balancing capability which is suitable for the fault-tolerant operation. These studies also indicated that the power loss of an inductor auxiliary circuit is less than the power loss of a capacitor auxiliary

Manuscript received Jan. 22, 2019; accepted Apr. 30, 2019
Recommended for publication by Associate Editor Liqiang Yuan.
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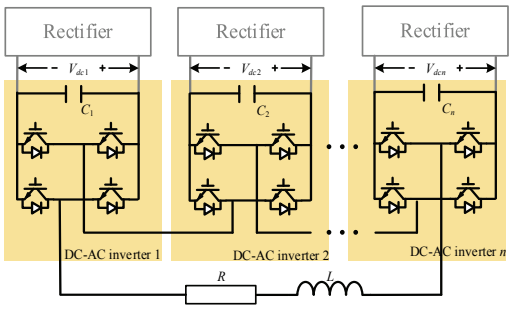


Fig. 1. Topology of a back to back cascaded converter.

circuit, since capacitor based circuits need to limit current by resistance. Although the auxiliary circuit can keep the converter working in some fault states, it increases the hardware cost of the converter [19]. In addition, the efficiency of the converter is decrease when the auxiliary circuit is added. Thus, a voltage balance strategy without an auxiliary circuit needs to be studied when the converter has broken down.

Solutions to the DC power balance in a CHBC that works as a rectifier is a heated topic. When a CHBC is used as rectifier, its DC power fault is equivalent to no load [20]-[23]. The authors of [20] keep the DC power steady by adopting PI controllers. However, experiment result verified that PI controllers cannot keep DC link voltage steady when one CHBC module is no load. The authors of [21] proposed a voltage balancing strategy with an extended operating region for a CHBC, which can balance the DC link voltage when one module is no load. However, the switch state jumps when this strategy is working. To solve the switch state jump, a 3-D space modulation based on a 3-module CHBC has been proposed [22]. Nevertheless, the 3-D concept is difficult to extend since the number of dimensions increases with the number of modules.

Some voltage balance strategies are applied 3LNPC cascaded converters, which can also balance the DC link voltage when the load has broken down. Based on the3-D concept, the N-D concept is proposed for 3LNPC cascaded converters. However, due to the complexity of the N-D concept, the experiment of N-D voltage balance is also less than 6 modules [24]. The authors of [25] proposed a voltage balance strategy that uses the opposite vector of SVPWM. Its voltage balance capability is strong, with the price of increasing switch state. Based on [25], the strategy in [26] smoothed the voltage balance by sacrificing a part of the dynamic performance. In addition, it is able to balance the DC link voltage when one source of the load is broken down. In addition, some power balance and fault-tolerant strategy methods are proposed to balance the power of three-phase cascaded inverters.

In this paper, a Capacitors Energy Strategy (CES) has been proposed for the CHBC, without using an auxiliary circuit. Although the CES increase the complex of the modulation, it can keep the voltage steady in response to a DC power fault while avoiding a switch state jump. Section II introduces the

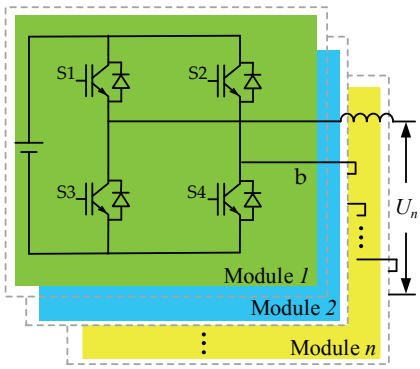


Fig. 2. Topology of a CHBC.

TABLE I
RELATIONSHIP BETWEEN SWITCH STATES OF POWER MODULES AND OUTPUT VOLTAGE

S1	S2	S3	S4	Switch State
On	Off	Off	On	+Vdc
On	On	Off	Off	0
Off	Off	On	On	0
Off	On	On	Off	-Vdc

topology and the switch states of the CHBC. Section III illustrates the proposed principle of voltage balance modulation in the presence of a DC power fault. Section IV illustrates the capacitors energy strategy. In the voltage balance process, the switch state of a cascaded inverter changes. If the switch state jumps from 1 to -1, the harmonic of the output voltage is an aberration. Experimental results verify that the strategy possesses good dynamic performance in Section V. Finally, some conclusions are drawn in Section VI.

II. CONFIGURATION

A. Topology of CHBC

Although the CHBC topology is well known, the switch state should also be elaborated to explain the power flow of the converter. The CHBC is usually employed in high voltage high power applications, where the switching devices are connected in series to reduce harmonic spectrum currents and voltages. At the same time, the CHBC can also reduce switching time and noise. The CHBC topology is shown in Fig. 2. Each converter module has its own DC link voltage. Once one module is working, the switch state outputs three kind of voltages $+V_{dc}$, 0, $-V_{dc}$. Therefore, the n module CHBC could provide a 2n+1 level output voltage.

Table I illustrates the switch of a CHBC module. The four switch states synthesize three kind of output voltage, V_{dc}, 0 and - V_{dc}. In the CHBC, the relationship between the DC link voltage and the output voltage are shown as follows.

Switch state 1: If i_s is positive, the DC port releases its energy to the grid, its power is equal to the DC link voltage product i_s, and vice versa.

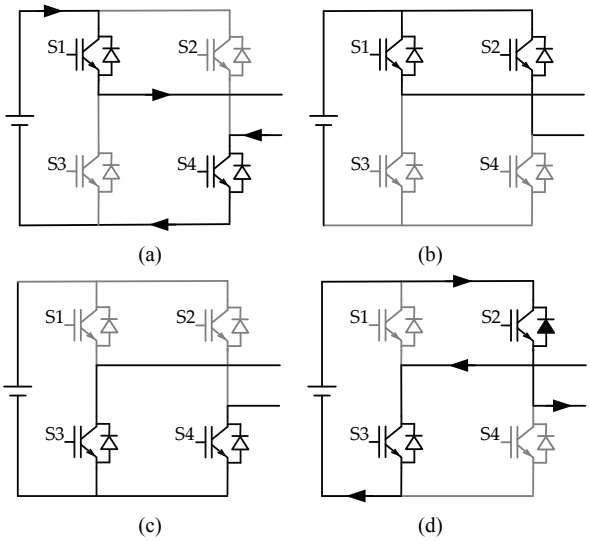


Fig. 3. Switch states of a CHBC module. (a) Switch state 1. (b) Switch state 2. (c) Switch state 3. (d) Switch state 4.

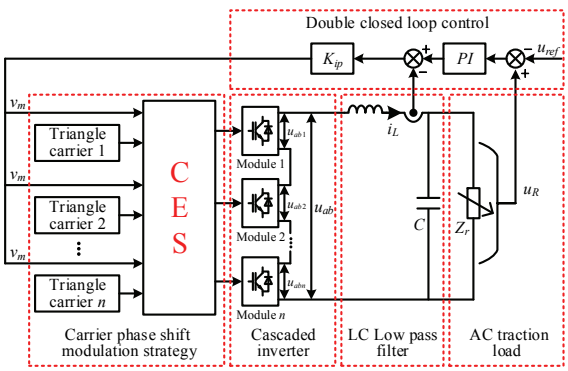


Fig. 4. Theory of PSC modulation.

Switch state 2: There is no energy exchange between the DC port and the grid, regardless of what i_s is.

Switch state 3: This state is the same as Switch state 2.

Switch state 4: If i_s is positive, the DC port absorbs energy from the grid, its power is equal to the DC link voltage product i_s, and vice versa.

Generally, if i_s is positive, switch state 1 increases the DC link voltage of the module, switch state 2 and switch state 3 protect the DC link voltage from changing, switch state 4 decrease the DC link voltage of the module, and vice versa. The power flow of the CHBC module mentioned above is shown in Fig. 3.

B. Control Strategy of the CHBC

A control strategy of a CHBC is shown in Fig. 4. The double closed loop control strategy is applied in this paper. The outer loop control strategy is designed to control the output voltage. The inner loop control strategy is designed to change the dynamic response of the system. The output voltage and inductance current are detected to get involved in the control. The carrier phase shift strategy is used as the

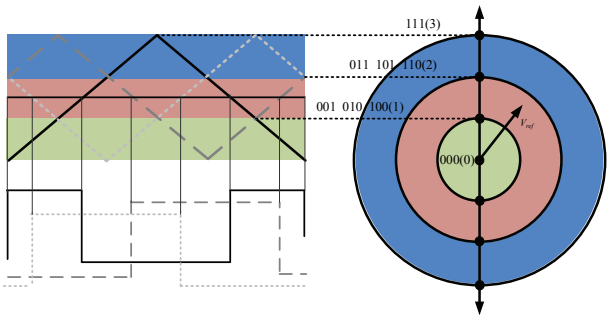


Fig. 5. Theory of PSC modulation.

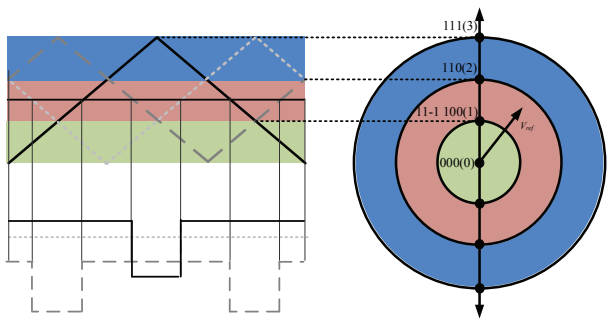


Fig. 6. Theory of voltage balance modulation.

modulation strategy. Every inverter model has the same modulation wave produced by the controller. However, the triangle angle waves are different. The phase angle of each module is 2π/n by turn, when n represents the number of cascaded inverter models. The theory of the voltage balance modulation strategy is used to drive the inverter model. After the basic modulation, the CES is used when the module suffers from a DC-link port fault. Thus, the CES selects a proper switch state to keep the voltage balance.

The working principle of phase shift carrier (PSC) modulation is illustrated in Fig. 5 when there is no voltage balance strategy working in the CHBC. Under this modulation, the initial phase of the carrier shifts 360°/*n* by turn so that the duty time of the PWM is split equally among each module by turn. Using three modules as an example, the modulation wave is partitioned by the horizontal straightness passing through the intersection of the two carrier waves. The number of the zone is equal to the number of modules. Under this modulation, the PWM signal shift by turn so that the duty time of the PWM is split equally among each module by turn.

The principle of the voltage balance strategy is shown in Fig. 6. When i_s is positive, if the DC link voltage of the module needs to be increased, it exchanges their Vdc switch state to the modules that have a 0 switch state or a - Vdc switch state for the voltage balance. Particularly, if the DC link voltage of module needs to be increased, it exchanges the - Vdc switch state to the modules that have a 0 switch state or a Vdc switch state for voltage balance. As can be seen from the input of the cascaded converter, the exchanging action has no effect on its output voltage. Therefore, in theory this voltage balance strategy brings no harmonic current for

CHBC. However, the exchange action reduced the regular input voltage of each module when compared to the PSC.

III. CAPACITORS ENERGY STRATEGY

Assuming that all of the DC link voltages of the N module CHBC are equal, the expressions are shown in (1).

$$\begin{cases} C_1 = C_2 = \cdots = C_n = C \\ V_{dc1} = V_{dc2} = \cdots = V_{dcn} = V_{dc} / n \end{cases} \tag{1}$$

If the DC power of one module fails, the expressions are shown as (2).

$$\begin{cases} C_1 = C_2 = \cdots = C_n = C \\ V_{dc1} = V_{dc2} = \cdots = V_{dcn-1} = V_{dc} / (n-1) \end{cases} \tag{2}$$

To keep the DC link voltage steady, the energy stored in the capacitors reaches the minimum value.

$$E = \frac{1}{2}\sum_{i=1}^{n-1} C_i V_{dci}^2 = \frac{C V_{dc}^2}{2(n-1)} \tag{3}$$

Define DC link voltage drift as:

$$\Delta V_{dci} = V_{dci} - \frac{V_{dc}}{n-1} \tag{4}$$

Define a positive-definite cost function J to indicate the energy drift from the minimum in (5).

$$J = \frac{1}{2} C \sum_{i=1}^{n-1} \Delta V_{dci}^2 \tag{5}$$

If a definite negative ΔJ can be guaranteed through proper PWM outputs, the voltages fluctuates towards balanced values. That is:

$$\frac{dJ}{dt} = C\sum_{i=1}^{n-1} \Delta V_{dci} \frac{dV_{dci}}{dt} = C\sum_{i=1}^{n-1} \Delta V_{dci} i_{dci} \le 0 \tag{6}$$

Where i_{dci} is the current of the capacitor Ci. The theorem is the capacitors energy theorem multilevel N-module cascaded inverter. When one of the DC link voltage experiences a fault, the voltages of the capacitors become unbalanced. Thus, the PWM reduces J to zero, which makes the voltages tend to be balanced. Generally, the DC-link voltages of all the modules should decrease their voltage as more as possible to keep their DC-link voltage balance.

An n module single phase cascaded inverter is shown in Fig. 7. The switch state of each converter can be defined to Si, which 1,0,-1. The equivalent model indicates that the operating currents of the capacitors charge or discharge. Thus, different switch states influence the DC link voltage balance.

Defined ***m*** as the switch state of the N module single phase cascaded inverter. Si is the switch state of each converter. Therefore, m can be calculated as (7).

$$\boldsymbol{m} = \sum_{i=1}^{n} S_i \tag{7}$$

Defined ***min*** as the power of the N module single phase cascaded inverter. It can be calculated as (8). According to the capacitors energy theorem, ***min*** is the minimum for the capacitor voltage balance.

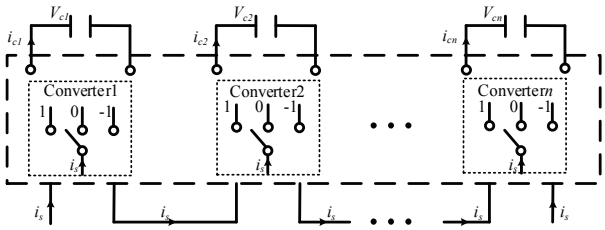


Fig. 7. Mathematic model of a CHBC.

TABLE II
CES PRINCIPAL

m	i_s	M_1	M_2	…	M_{n-1}	M_n
+1	+1			…		+1
+1	-1	+		…		
-1	+1	+		…		
-1	-1			…		-1

$$\boldsymbol{min} = \sum_{i=1}^{n} V_{dci} i_s S_i \tag{8}$$

In the voltage balance process, the switch state of the cascaded inverter changes. If the switch state jumps from 1 to -1, the harmonic of the output voltage is an aberration. In order to ensure that the output voltage changes smoothly, the switch state of each module should satisfy formula (9). Si' is the switch state of the last switch cycle.

$$\left| S_i - S_i^{'} \right| < 2 \tag{9}$$

In the voltage balance process, the switch state of the cascaded inverter changes. If the switch state jumps from 1 to -1, the harmonic of the output voltage would is an aberration. In order to ensure that the output voltage changes smoothly, the switch state of each module should satisfy formula (9). Si' is the switch state of the last switch cycle. The principal of the CES is shown as Table II. In this table, once the module that is supposed to be increased (decreased) has no ability to increase (decrease), this operation shifts to a nearby module. In addition, in the arrangement based principle of the CES, all of the modules of the CHBC like to keep their DC-link voltage as small as possible.

IV. LIMITATIONS

To ensure the limitations of the proposed strategy, the limitation calculation has been done as follows.

$$\Delta P_f = \int_0^{2\pi} V_{dc} \cdot S_f \cdot i_s dt \tag{10}$$

Where ΔPf is the energy of a faulty module per period. Once it is negative, the capacitor of the faulty module does not loss its energy. In other words, its DC-link voltage is kept balanced. Otherwise, its DC-link voltage is lost. The results of calculation are shown as Fig.8.

Where ΔP' is the unbalance degree, which is shown as:

$$\Delta P' = n\Delta P_f / (\Delta P_f + \sum \Delta P_i) \tag{11}$$

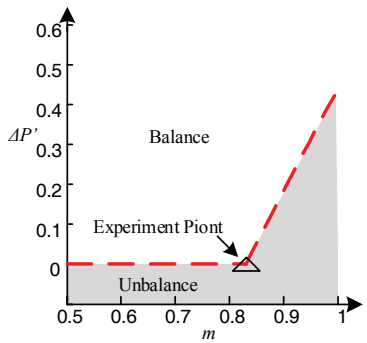


Fig. 8. Calculation results showing the voltage balance capability.

TABLE III
PROTOTYPE PARAMETERS

Parameter Name	Parameter value	numbers
Filter capacitor	90 V/50 Hz	1
Filter inductance	5 mL	1
DC link voltage (Vdc)	50V	3
dc-link capacitor	470 μF	3
Carrier wave frequency	750 Hz	-
Modulation depth	0.83	
Number of modules	3	-
Load of CHBC	50Ω	1

Where ΔPi is the energy of each module per period. Once $\Delta P'$ is 0, the DC-link voltage one module is faulty. The calculate result shows that, a 3-module CHBC can work normally when one module suffers from a DC-link fault, and the modulation is under 0.83. In this case, the output energy of the CHBC is supplied by the two normal modules. Thus, the power of the two modules increases. The increasing of the power of the normal module is calculated as:

$$\Delta P_n' = n\Delta P_n / (n-1) \tag{12}$$

Where $\Delta P_n'$ and ΔP_n are the power of the normal module before and after a fault. The calculation shows the increasing of the power decrease as the number of the module gains.

V. EXPERIMENT

A three module CHBC prototype has been designed and build in the laboratory. Two experiments are conducted thereon to illustrate the dynamic performance of the proposed strategy. The parameter and the prototype are shown in Table III and Fig. 9, respectively.

The first experiment has been carried out to verify the topology and the modulation of the prototype. Fig. 10(a) shows a static wave of the PSC modulation of the CHBC. A seven-level output voltage is synthesized by a three module CHBC, while the switches of each module are on and off by turn. Fig. 10(b) shows a static wave of the output voltage when the proposed strategy works, and module 3 is regarded as the one that suffers from DC output loss. Based on the capacitors energy strategy, most of the switch states that can

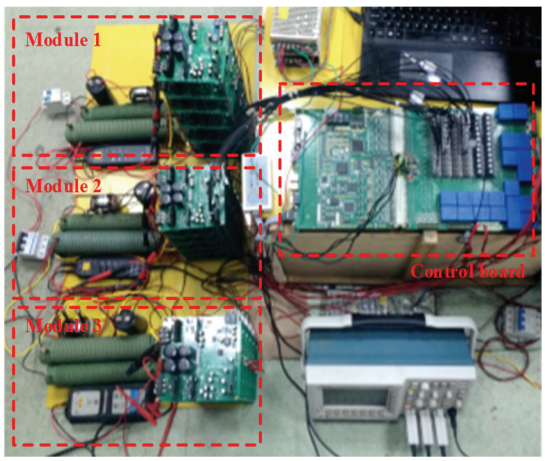
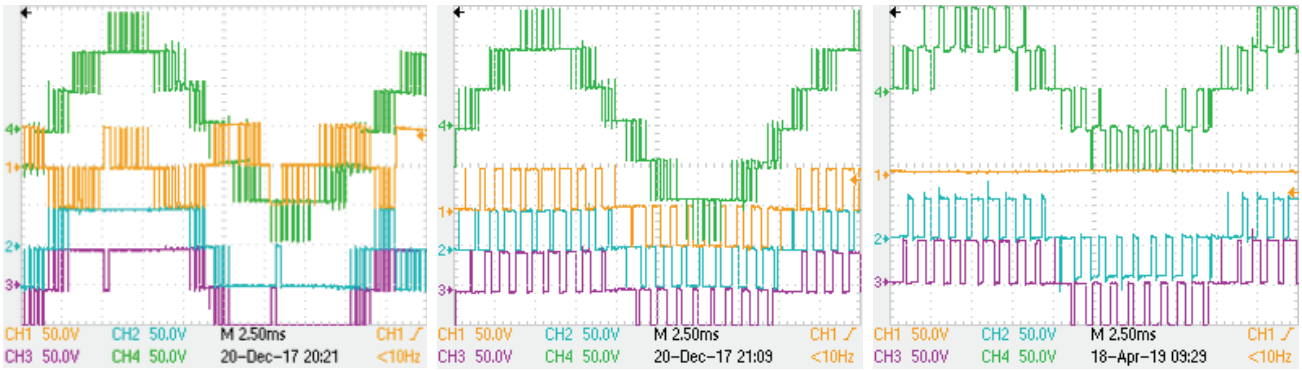


Fig. 9. Prototype of a 3-module CHBC.

absorb energy is utilized by this module. However, the output voltage of the CHBC remains normal, despite the fact that the output voltage of each module is rearranged by the proposed strategy. Fig. 10(b) shows no voltage balance strategy being used when the DC-link voltage of one module has failed. The output voltage distortion came as the DC-link voltage of the failed module decreased to zero.

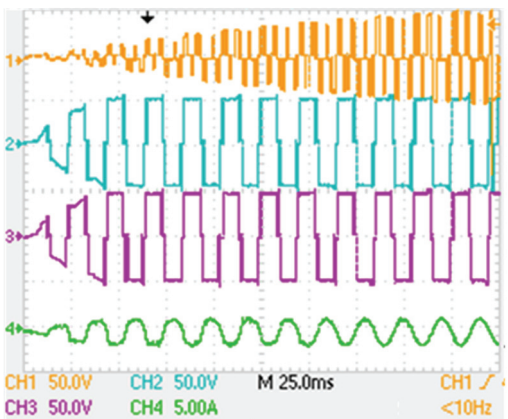
Fig. 11 shows the start states of a CHBC when one rectifier fails. Because of the DC link voltage loss, the DC link voltage and output voltage of the faulty module are 0 at the beginning of the experiment. After about 0.2s, the DC link voltage of the faulty module recovered to normal. Due to the proposed strategy, the number of times of the switch increased in the fault module to keep the DC link voltage steady. Although the switch states of all the modules were rearranged, the total voltage of the CHBC remained unchanged. Fig. 11(a) shows the output voltage of 3 modules and the current of the CHBC. Because of the fault of the DC part, the output voltage is initially zero. Gradually, with the DC link voltage recovering, the output voltage becomes normal. Fig. 11(b) illustrated the DC link voltage of each module and the current of the CHBC. Fluctuation appears when the DC link voltage of the faulty module is balanced. This fluctuation indicates that the proposed strategy dynamically keeps the DC link voltage steady. In Fig. 11(c), the DC link voltage of the faulty module, the output voltage of the cascaded converter, the output voltage of the faulty module, and the current of the CHBC are shown. With the DC link voltage of the fault module returning, the output voltages are also normal. Fig. 11(d) illustrates the output voltage of the cascaded converter and all of the modules. All of the modules work under a limited switch frequency, even the switch frequency of the faulty module increased.

A step change experiment when one rectifier failed is illustrated in Fig. 12, where the output voltage of each module, the current of a CHBC, the DC link voltage, and the output voltage of a CHBC are shown. When the step change occurred, the voltage of the faulty module kept steady with only slight fluctuations, and the output current was not disturbed during



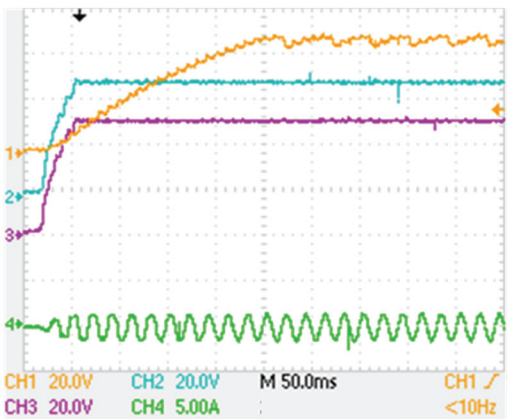
(a) (b) (c)

Fig. 10. Static experiment waves of a CHBC (CH1: Output voltage of module 1, CH2: Output voltage of module 2, CH3: Output voltage of module 3, CH4: Output voltage of CHBC). (a) PSC modulation of a CHBC. (b) Proposed strategy of a CHBC. (c) DC-link voltage failure of a CHBC.



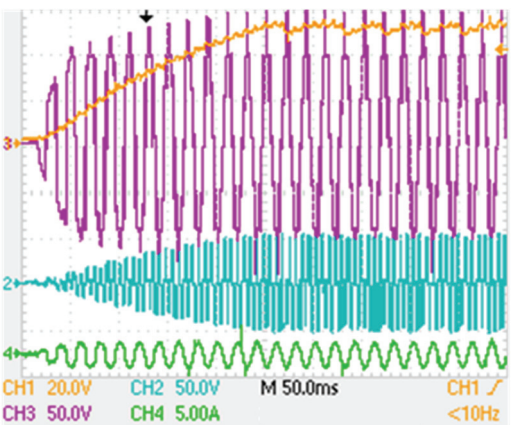
(CH1: Output voltage of module 1, CH2: Output voltage of module 2, CH3: Output voltage of module 3, CH4: Output voltage of a CHBC)

(a)



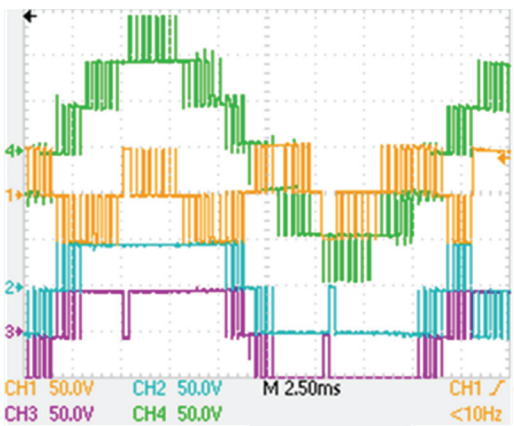
(CH1: DC link voltage of module 2, CH2: Output voltage of a CHBC, CH3: Output voltage of module 3, CH4: i_s)

(b)



(CH1: DC link voltage of module 1, CH2: Output voltage of module 1, CH3: Output voltage of a CHBC, CH4: i_s)

(c)



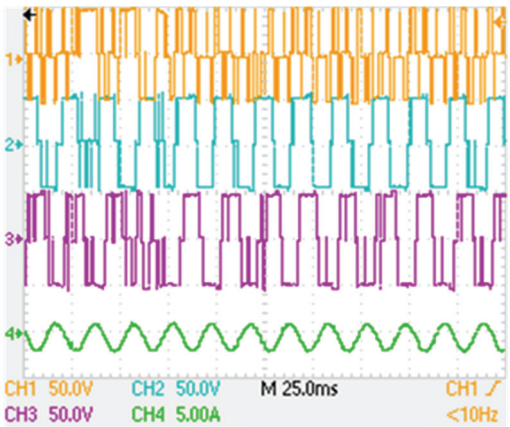
(CH1: Output voltage of module 1, CH2: Output voltage of module 2, CH3: Output voltage of module 3, CH4: Output voltage of a CHBC)

(d)

Fig. 11. Start states experiment when one rectifier is faulty. (a) Output voltage of 3 modules. (b) DC link voltage of 3 modules. (c) Experimental waves of the faulty module. (d) Proposed strategy of a CHBC.

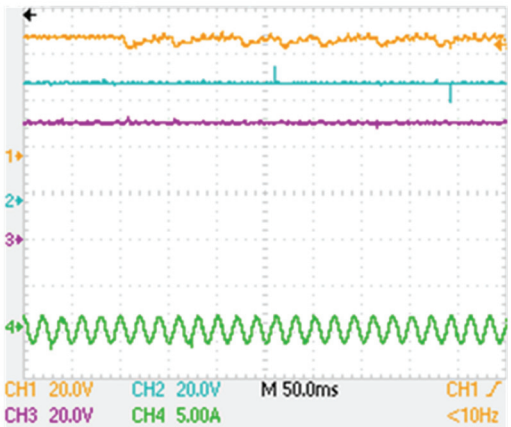
the step change. Similarly, in the start experiment, the output voltage of a CHBC remained normal.

To verify the dynamic characteristic of the proposed strategy, another step change has been done, as shown in Fig. 13. The experimental process is shown as follows. At the time of t1, the DC port of one module failed. At the time of t2, when the DC link voltage of the failed module is less than half that of the normal module, the proposed strategy is used and the DC



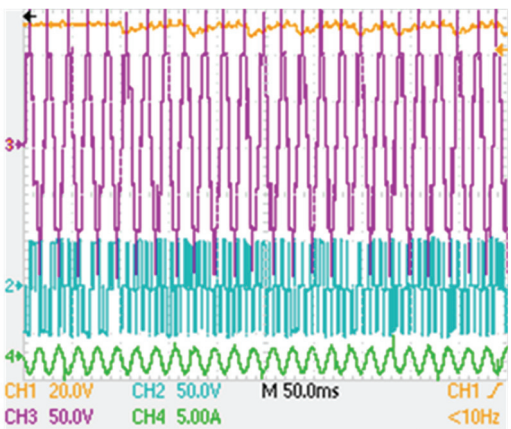
(CH1: Output voltage of module 1, CH2: Output voltage of module 2, CH3: Output voltage of module 3, CH4: Output voltage of a CHBC)

(a)



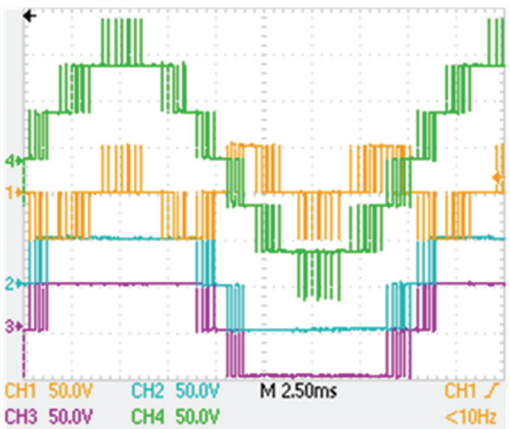
(CH1: DC link voltage of module 1, CH2: DC link voltage of module 2, CH3: DC link voltage of module 3, CH4: i_s)

(b)



(CH1: DC link voltage of module 1, CH2: Output voltage of module 1, CH3: Output voltage of a CHBC, CH4: i_s)

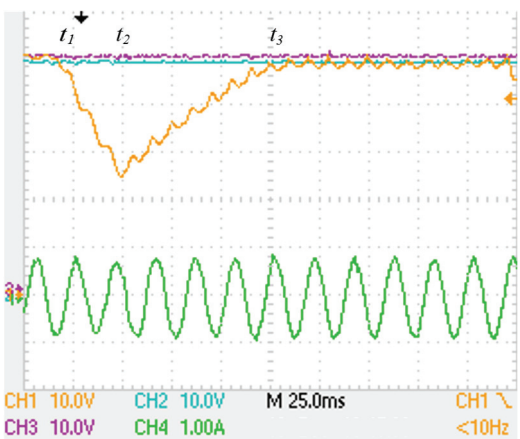
(c)



(CH1: Output voltage of module 1, CH2: Output voltage of module 2, CH3: Output voltage of module 3, CH4: Output voltage of a CHBC)

(d)

Fig. 12. Step change experiment when one rectifier is faulty. (a) Output voltage of 3 modules; (b) DC link voltage of 3 modules. (c) Experiment wave of the faulty module. (d) Proposed strategy of a CHBC.



(CH1: DC link voltage of module 1, CH2: DC link voltage of module 2, CH3: DC link voltage of module 3, CH4: i_s)

Fig. 13. Step change experiment when one rectifier is faulty.

link voltage starts to raise. After about 0.1s, the DC link voltage recovers. This experiment illustrates the strong dynamic performance of the proposed strategy.

VI. Conclusion

A capacitors energy strategy of a CHBC for voltage stability has been proposed. The proposed strategy permits the CHBC to work under a DC power fault, while keeping the DC link voltage balanced, the switch state continuous and the switch frequency normal. In addition, the output voltage of the CHBC remain normal. However, the output voltage of each module is rearranged by the proposed strategy. Experiments have verified that under the starting and normal working conditions, the proposed strategy can keep the DC link voltage steady when the modulation depth remains under 0.8. In other words, the proposed strategy is able to protect the CHBC from DC power faults.

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