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Average Current Control for Parallel Connected Converters

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Abstract

A current sharing controller is proposed in this paper for parallel-connected converters. The proposed controller is based on the calculation of the magnitudes of system current space vectors. Good current distribution between parallel converters is achieved with only one Proportional-Integral (PI) compensator. The proposed controller is analyzed and the circulating current impedance is derived for paralleled systems. The performance of the new control strategy is experimentally verified using two parallel connected converters employing Space Vector Pulse Width Modulation (SVPWM) feeding a passive *RL* load and a 2.2 kW three-phase induction motor load. The obtained test results show a reduction in the current imbalance ratio between the converters in the experimental setup from 53.9% to only 0.2% with the induction motor load.

Key words: Converters, Current control, DC-AC power conversion, PWM converters

I. INTRODUCTION

Voltage-fed converters are often connected in parallel in high power applications to achieve the required current ratings of the system. Parallel connected converters offer other significant advantages in terms of reliability and system efficiency [1]-[4]. However, these circuits introduce significant issues of their own. One of the most important drawbacks of connecting converters in parallel is the flow of circulating current between the converters. This refers to the unequal distribution of load current between the paralleled converter units. This results in increases in the losses and current distortion, along with a degradation in system reliability, which could potentially damage the converters [5].

Circulating currents exist due to differences in converter parameters, modulation and carrier waveforms, which are impossible to eliminate in practice. To reduce circulating currents, separate (and isolated) sources [6] or isolating transformers [7] can be employed. However, this comes at a considerable price in terms of cost, size and system efficiency. Inter-module reactors employed to limit high frequency ripple currents [8]-[10] are ineffectual in limiting the flow of low frequency circulating current components.

It is possible to eliminate inter-module reactors by sharing converter switching times to remove the circulating current pathway [11]. However, this approach leads to undesirably high *dv*/*dt* values. A more cost-effective approach is to use advanced active control techniques to improve the current sharing between parallel connected converters without any galvanic isolation and with much smaller passive components. One such technique is "average current control" [12]-[14] where the instantaneous average value of the converters' ac phase current is calculated, and the error signal between each of the converter currents and the calculated average value are utilized to modify the reference modulating signal and improve current sharing between converters. However, this requires a critical communications link between the parallel connected units, which produces time delays that have a detrimental effect on system performance and stability [15]. Good current distribution between parallel connected converters can be achieved with minimal communications between converters [16]. However, the current sharing control loop in [16] adopts a low pass filter and a PI controller. As a result, this approach has a trade-off between good current distribution

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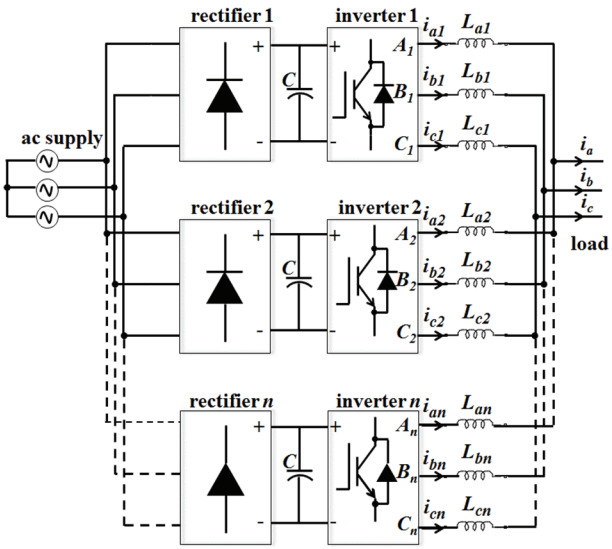


Fig. 1. Parallel connected converters.

and good voltage regulation. In addition, the presence of the low pass filter can have negative consequences on the dynamic response of the controller. To overcome these limitation, repetitive control can be adopted to control zero-sequence circulating current (ZSCC) without data sharing [17]. All of the active control methods mentioned above offer good current sharing performance at the cost of a heavy computational burden.

A new "average current" sharing control scheme is proposed in this paper for *n* parallel-connected, three-phase converters. Unlike conventional average current controllers, which are normally based on rotating or stationary reference frame approaches, the proposed control strategy is based on the calculation of the system current space vector magnitudes. The error in the current space vector magnitude signal is used to modify the output voltage amplitude to achieve excellent load current sharing performance without adversely affecting the converter output voltage regulation. Accordingly, only one PI compensator is needed for each of the inner control loops, which significantly reduces the computational requirements of the controller.

Fig. 1 shows a schematic diagram of the proposed system. The n parallel converters use separate but not isolated dc links and small current sharing reactors L_{an}-L_{cn}. In this study, the new control scheme is implemented on two parallel voltage-fed SVPWM converters, and its performance is experimentally verified using two 1.25 kVA converters feeding a three-phase passive *RL* load and a 2.2 kW induction motor load. Excellent current sharing results are achieved with a reduction in the current imbalance ratio between the two converters from 53.9% (with no current sharing control) to only 0.2% (with the proposed average current control strategy).

The remainder of this paper is organized as follows. Section II presents an outline of the proposed current sharing control scheme. A mathematical analysis of *n*-parallel converters with and without the activation of the proposed controller is presented in Section III. It also includes a derivation of the effective circulating current impedance and an examination of the system voltage regulation. The stability of the system and the tuning of the controller parameters are discussed in Section IV. An experimental verification of the performance of the proposed controller is presented in Section V. Some conclusions are given in Section VI.

II. Outline of the Proposed Controller

Considering the system shown in Fig. 1, a common mode h^{th} harmonic current flows in the *n* parallel converters superimposed on the balanced three-phase currents because of the closed current paths that exist between the converters. The *j*th converter *ac* currents can be written as:

$$\begin{aligned} i_{aj}(t) &= I\,sin(\omega t) + \Delta i_j \\ i_{bj}(t) &= I\,sin(\omega t - 2\pi/3) + \Delta i_j \\ i_{cj}(t) &= I\,sin(\omega t - 4\pi/3) + \Delta i_j \end{aligned} \tag{1}$$

where $\Delta i_j = K\,sin(h\omega t)$.

The magnitude of the current space vector for the j^{th} converter $|\mathbf{I}_j|$ is then given by:

$$\begin{aligned} |\mathbf{I}_j| &= \sqrt{2/3\left(i_{aj}^2(t) + i_{bj}^2(t) + i_{cj}^2(t)\right)} \\ &= \sqrt{\left(I^2 + 2K^2\left(sin(h\omega t)\right)^2\right)} \end{aligned} \tag{2}$$

Equation (2) shows that $|\mathbf{I}_j|$ contains common mode current Δi_j within its formulation, meaning that it can be used for current sharing control [16]. In this way, each of the converters needs to employ only one PI compensator to achieve equal current sharing and only the number of units in operation needs to be shared instead of three compensators and three pieces of shared information, i.e. the three average values of the converter phase currents [12].

A block diagram of the proposed control scheme is shown in Fig. 2. Two control loops are employed; an external *dq* load current control loop and an inner current sharing control loop. Fig. 3 shows a block diagram of the load current controller used to provide separate control of the direct and quadrature axis currents. The difference between the *j*th converter current space vector magnitude and the average of the current space vector magnitudes is fed to a PI compensator which then produces a suitable deviation in the base modulation index. Thus, the current magnitude $|\mathbf{I}_j|$ is forced to track the average of the current magnitudes $|\mathbf{I}_{av}|$ and an equal current distribution is obtained.

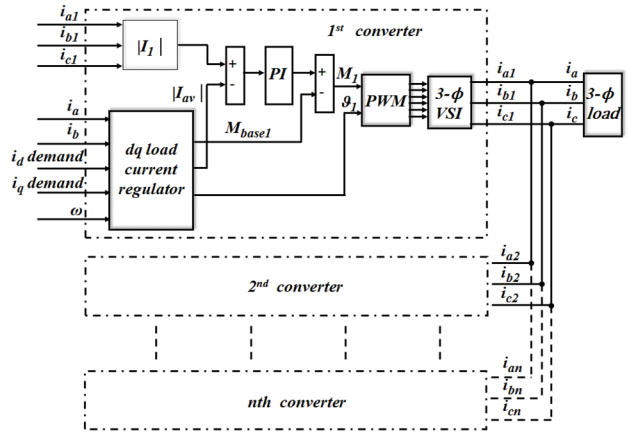


Fig. 2. Block diagram of the proposed controller.

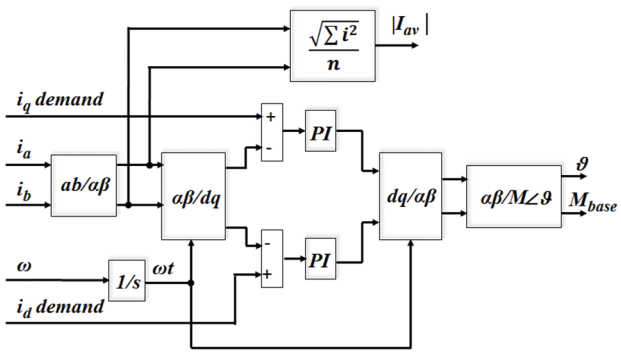


Fig. 3. Block diagram of the *dq* current regulator.

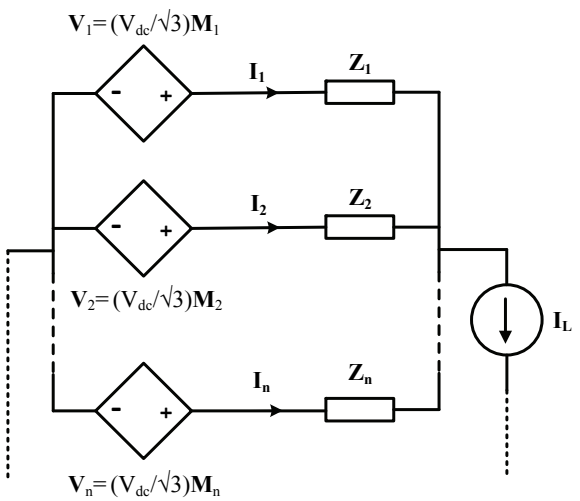


Fig. 4. Simple equivalent circuit for n three-phase converters connected in parallel.

III. Mathematical Description

Parallel-connected converters can be represented by the average equivalent circuit model shown in Fig. 4, where $\mathbf{V}_j$ is a dependent voltage source representing the voltage space vector of the j^{th} converter, and $\mathbf{I}_j$ is the corresponding current space vector. In this simple equivalent circuit representation,

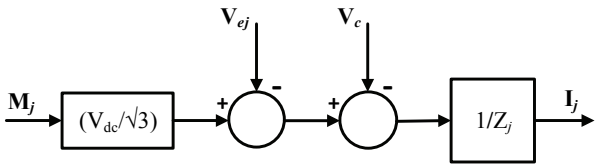


Fig. 5. Converter model in block diagram form without current sharing control.

the inter-module reactors are modelled as an impedance $\mathbf{Z}_j$ while the load is represented by a constant current source. This is a reasonable approach since the inductance of the inter-module reactors is normally much lower than the load inductance. $\mathbf{V}_c$ is the voltage space vector at the common coupling point, and $\mathbf{I}_L$ is the load current space vector. Each PWM converter is represented by a dependent dc voltage source whose value is a function of the modulation index ($V_j = M_j V_{dc}/\sqrt{3}$), where V_{dc} is the dc link voltage.

A. Uncontrolled System

For an uncontrolled system with no current sharing control, each converter can be represented in block diagram form as shown in Fig. 5. The bias voltage source V_{ej} is used to model the reduction in the converter output voltage due to switch voltage drops and converter deadtime effects. Using the principle of superposition, the current space vector $\mathbf{I}_j$ can be expressed as:

$$\mathbf{I}_j = \frac{(V_{dc}/\sqrt{3})}{\mathbf{Z}_j}\mathbf{M}_j - \frac{1}{\mathbf{Z}_j}\mathbf{V}_{ej} - \frac{1}{\mathbf{Z}_j}\mathbf{V}_c \tag{3}$$

The circulating current in the j^{th} converter, given by the equation $\mathbf{I}_{cirj} = \mathbf{I}_j - \mathbf{I}_{av}$, can then be derived as:

$$\mathbf{I}_{cirj} = \frac{(V_{dc}/\sqrt{3})}{\mathbf{Z}_j}(\mathbf{M}_j - \mathbf{M}_{av}) - \frac{1}{\mathbf{Z}_j}(\mathbf{V}_{ej} - \mathbf{V}_{eav}) \tag{4}$$

where $\mathbf{M}_{av}$ is the average modulation index, and $\mathbf{V}_{eav}$ is the average bias voltage for the n converters. Equation (4) shows that the circulating current has two components; one due to the differences in the values of the modulation indexes and one due to the differences in the dead-time effects and the device voltage drops producing different bias voltage values.

B. Controlled System

Following the activation of the current sharing control inner loop, each of the converters can be represented by the block diagram model shown in Fig. 6, where $\mathbf{G}_c(s)$ is the transfer function of the PI compensator, which is expressed as:

$$\mathbf{G}_c = K_p + \frac{K_i}{s} = K_p\left(\frac{1 + T_i s}{T_i s}\right) \tag{5}$$

where K_p and K_i are the proportional and integral gains, and T_i is the integral time constant.

Assuming a proportional compensator for the sake of

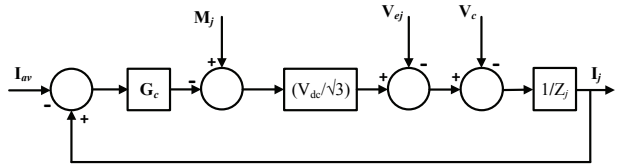


Fig. 6. Inverter block diagram with the proposed average current sharing control.

simplicity ($\mathbf{G}_c = k_p$), the current space vector of each converter can be defined as:

$$\mathbf{I}_j = \frac{(\mathrm{V_{dc}}/\sqrt{3})}{\mathbf{Z}_j + K_p(\mathrm{V_{dc}}/\sqrt{3})}\mathbf{M}_j - \frac{1}{\mathbf{Z}_j + K_p(\mathrm{V_{dc}}/\sqrt{3})}(\mathbf{V}_{ej} + \mathbf{V}_c) + \frac{K_p(\mathrm{V_{dc}}/\sqrt{3})}{\mathbf{Z}_j + K_p(\mathrm{V_{dc}}/\sqrt{3})}\mathbf{I}_{av} \tag{6}$$

Given the following equation for the circulating current ($\mathbf{I}_{cirj} = \mathbf{I}_j - \mathbf{I}_{av}$):

$$\mathbf{I}_{cirj} = \frac{(\mathrm{V_{dc}}/\sqrt{3})}{\mathbf{Z}_j + K_p(\mathrm{V_{dc}}/\sqrt{3})}(\mathbf{M}_j - \mathbf{M}_{av}) - \frac{1}{\mathbf{Z}_j + K_p(\mathrm{V_{dc}}/\sqrt{3})}(\mathbf{V}_{ej} - \mathbf{V}_{eav}) \tag{7}$$

Comparing (7) with (4), the effective circulating current impedance is increased from $\boldsymbol{Z}_j$ to $\boldsymbol{Z}_j + K_p(\mathrm{V_{dc}}/\sqrt{3})$ by the activation of the proposed current controller. Thus, the circulating current can be significantly reduced with a suitable selection of compensator parameters. Furthermore, the current sharing performance of the parallel connected converters can be made nearly independent of any mismatch in $\boldsymbol{Z}_j$ if the value of $K_p(\mathrm{V_{dc}}/\sqrt{3})$ is significantly higher than the impedance of the current sharing reactors.

C. Load Current and Voltage Regulation Analysis

In conventional virtual impedance approaches [16]-[19], the load current $\mathbf{I}_L$, and hence the common coupling point voltage space vector $\mathbf{V}_c$, are significantly affected by the actions of the current sharing controller. This is not the case with the proposed average current controller, which increases the effective impedance seen by the circulating current with no adverse effects on the load current and voltage regulation. This can be verified by comparing the load current space vector equation for the uncontrolled system with the corresponding equations for the system described in [16] and the system employing the proposed average current sharing control strategy.

Fig. 5 shows that the total load current space vector can be obtained from a summation of the current space vectors of the parallel connected modules. Assuming $\mathbf{Z}_1=\mathbf{Z}_2=\mathbf{Z}_n=\mathbf{Z}$, the equation for the uncontrolled system is:

$$\mathbf{I}_L = \frac{(\mathrm{V_{dc}}/\sqrt{3})}{\mathbf{Z}}\sum_{j=1}^{n}\mathbf{M}_j - \frac{1}{\mathbf{Z}}\sum_{j=1}^{n}\mathbf{V}_{ej} - \frac{1}{\mathbf{Z}}\sum_{j=1}^{n}\mathbf{V}_c \tag{8}$$

In [16], the activation the control strategy produced a load current vector expressed as:

$$\mathbf{I}_L = \frac{(\mathrm{V_{dc}}/\sqrt{3})}{\mathbf{Z} + K_p(\mathrm{V_{dc}}/\sqrt{3})(1 - G_f)}\sum_{j=1}^{n}\mathbf{M}_j - \frac{1}{\mathbf{Z} + K_p(\mathrm{V_{dc}}/\sqrt{3})(1 - G_f)}\sum_{j=1}^{n}(\mathbf{V}_{ej} + \mathbf{V}_c) \tag{9}$$

Equation (9) shows that the load current in [16] is reduced when compared with the uncontrolled system (equation (8)), since the magnitude of the LPF transfer function G_f is always < 1 at frequencies greater than the filter cut off frequency. This influences the system voltage regulation (i.e. the common coupling point voltage space vector $\mathbf{V}_c$ is altered by the current sharing controller).

In contrast, load current vector produced by activation of the average current control strategy proposed in this paper can be calculated from (6) as follows:

$$\mathbf{I}_L = \frac{(\mathrm{V_{dc}}/\sqrt{3})}{\mathbf{Z} + K_p(\mathrm{V_{dc}}/\sqrt{3})}\sum_{j=1}^{n}\mathbf{M}_j - \frac{1}{\mathbf{Z} + K_p(\mathrm{V_{dc}}/\sqrt{3})}\sum_{j=1}^{n}(\mathbf{V}_{ej} + \mathbf{V}_c) + \frac{K_p(\mathrm{V_{dc}}/\sqrt{3})}{\mathbf{Z} + K_pK_b}\mathbf{I}_L \tag{10}$$

which may be simplified to:

$$\mathbf{I}_L = \frac{(\mathrm{V_{dc}}/\sqrt{3})}{\mathbf{Z}}\sum_{j=1}^{n}\mathbf{M}_j - \frac{1}{\mathbf{Z}}\sum_{j=1}^{n}\mathbf{V}_{ej} - \frac{1}{\mathbf{Z}}\sum_{j=1}^{n}\mathbf{V}_c \tag{11}$$

Equations (8) and (11) are identical, which demonstrates that the load current is not affected by the proposed current sharing controller. The system voltage regulation is not influenced (i.e. the common coupling point voltage space vector $\mathbf{V}_c$ is not altered) by the virtual impedance emulation introduced by the proposed current sharing controller.

IV. Stability Analysis

An equivalent continuous time model of the current sharing controller that accounts for the sampling time delay and the computation time of the algorithm is needed to tune the PI-compensator within the current sharing controller [20]. Fig. 7 shows a block diagram representation a converter model with the proposed current sharing control scheme, where the sampling and computation delays (T_d) are modelled by an e^{-sT_d} time delay block in the forward path.

The PWM duty cycle is updated twice every carrier period, which produces a computation delay of half a period of the carrier waveform. An additional quarter-carrier period sampling delay is introduced into the control loop since asymmetrical

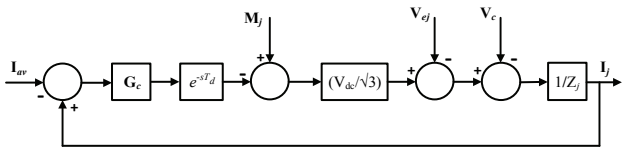


Fig. 7. Converter block diagram with average current sharing control considering time delay effects.

regular sampled PWM is adopted. Thus, the open loop transfer function **G** is given by:

$$\mathbf{G} = K_p\left(\frac{1+T_i s}{T_i s}\right)\frac{k e^{-sT_d}}{(1+T_a s)} \tag{12}$$

where $k = (\mathrm{V_{dc}}/\sqrt{3})/r$, and T_a is the time constant (L/r) of the current sharing reactors. The proportional gain maximum value can be selected so the open loop gain is unity with a suitable phase margin Φ_m [21]. Then the open loop phase angle at the crossover frequency ω_c is given by:

$$\begin{aligned}\angle G(j\omega_c) = tan^{-1}(\omega_c T_i) - \frac{\pi}{2} - \omega_c T_d \\ - tan^{-1}(\omega_c T_a) = -\pi + \Phi_m\end{aligned} \tag{13}$$

For small values of r, $\omega_c T_a \gg 1$, $tan^{-1}(\omega_c T_a) \approx \pi/2$, and

$$\omega_c = \frac{tan^{-1}(\omega_c T_i) - \Phi_m}{T_d} \tag{14}$$

The maximum value of ω_c can be obtained from (14) as:

$$\omega_{c(max)} = \frac{\frac{\pi}{2} - \Phi_m}{T_d} \tag{15}$$

Setting the magnitude of **G** to unity at $\omega_{c(max)}$, the maximum possible value of K_p is:

$$K_p = \frac{T_i \omega_{c(max)}\sqrt{1+\left(T_a \omega_{c(max)}\right)^2}}{k\sqrt{1+\left(T_i \omega_{c(max)}\right)^2}} \tag{16}$$

As $T_a \omega_{c(max)} \gg 1$ and $T_i \omega_{c(max)} \gg 1$ [20], equation (16) is simplified to:

$$K_p = \frac{T_a \omega_{c(max)}}{k} = \frac{L \omega_{c(max)}}{V_{dc}/\sqrt{3}} \tag{17}$$

K_p is a function of the dc link voltage, the inductance of the current sharing reactors, and the crossover frequency, which in turns depends on the sampling and computation delay (T_d).

The integral time constant $(T_i = K_p/K_i)$ is selected so that the assumption $tan^{-1}(\omega_{c(max)} T_i) \approx \pi/2$ is valid. Using a value of $tan^{-1}(\omega_{c(max)} T_i) = 89.5^\circ$ gives:

$$T_i = \frac{tan(89.5^\circ)}{\omega_{c(max)}} \tag{18}$$

For a phase margin of 60°, and using the parameters of the

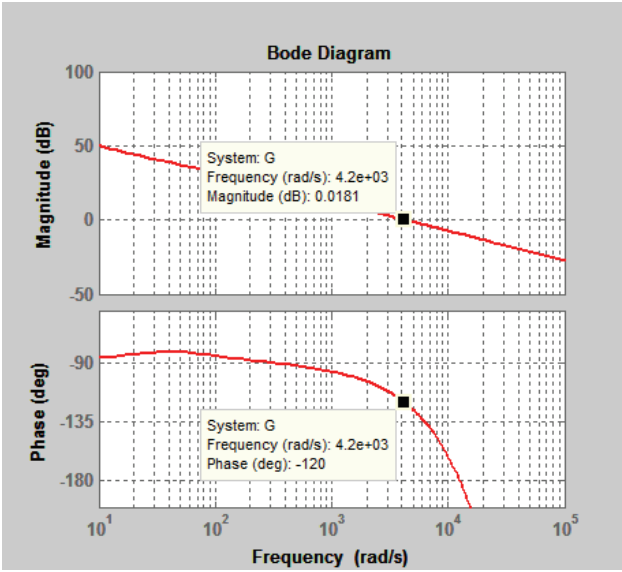


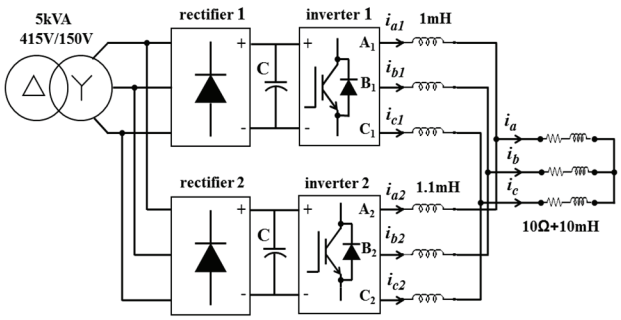
Fig. 8. Bode plots of the open loop forward path with the delay effect; K_p=0.036 and K_i=1.33.

experimental system used in this investigation (L=1 mH, r=0.05 Ω, V_{dc}=202.5 V and T_d=0.125 ms), the system crossover frequency is about 4190 rad/sec (666 Hz), approximately one tenth of the switching frequency (6 kHz) and more than ten times the *ac* line frequency, which ensures both switching noise immunity and a fast dynamic response [22]. The PI controller gains are $K_p = 0.036$ and $K_i = 1.33$ (T_i=0,027 s) and corresponding bode plots of the open loop transfer function are shown in Fig. 8.

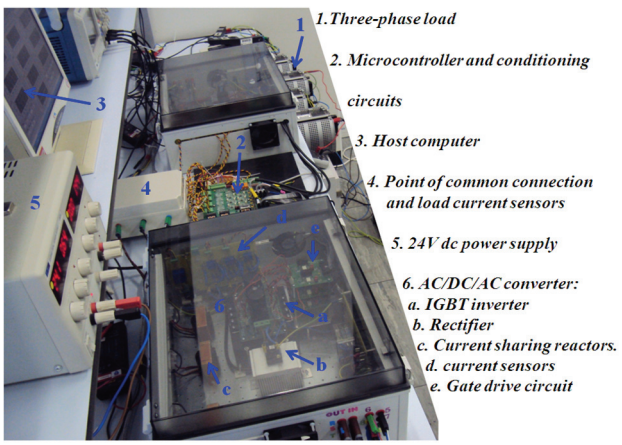
V. Experimental Verification

A test rig based on two parallel, diode front-end, 1.25kVA converters and a 340uF dc link capacitor, was constructed (Fig. 9) to verify the proposed average current control strategy. Both of the converters were supplied from one 50Hz, 5kVA three-phase transformer. Each of the converters was constructed using six discrete IGBTs (IRG7PH35UD1PbF). Six 1mH current sharing reactors with an internal resistance of 0.05Ω were employed. A 12 kHz sampling frequency was chosen to reduce the PWM sampling delay, which results in an increased control bandwidth [21]. The converter switching frequency was 6 kHz. Exaggerated differences in the inter-module reactors and converter PWM dead time were deliberately introduced into the test rig. Three additional 0.1mH inductors were connected in series with the 1mH inter-module reactors (one in each phase) of converter 2. A 20% dead time increment, relative to the first converter, was introduced into the second converter.

For the sake of convenience, one TMS320F28335DSP microcontroller using two independent interrupt service routines was used in the experimental test rig to implement the control algorithms. However, in a practical implementation,

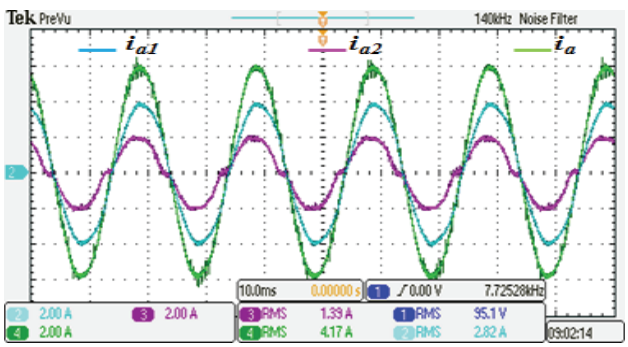


(a)



(b)

Fig. 9. Experimental setup with a passive *R-L* load. (a) Circuit diagram. (b) Photograph.



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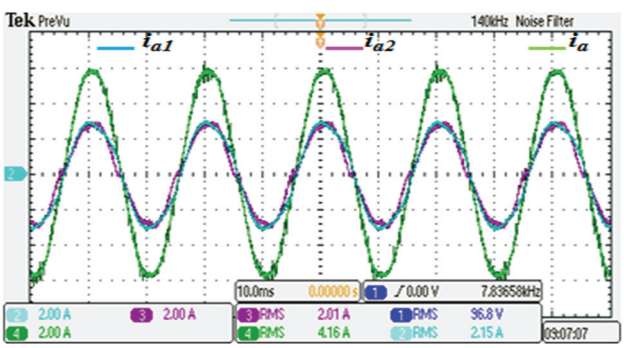


(b)

Fig. 10. Experimental current waveforms, passive *R-L* load (2A/div, 10ms/div). (a) With the current sharing controller de-activated. (b) With the current sharing controller.

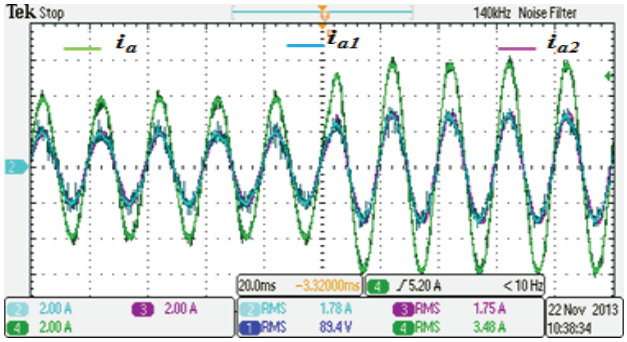


Fig. 11. Experimental current waveforms, transient response with the current sharing control, passive R-L load (2A/div, 20ms/div).

each of the converters would have independent control hardware. Experimental results were obtained for two different types of load; a passive *RL* load and an induction motor load.

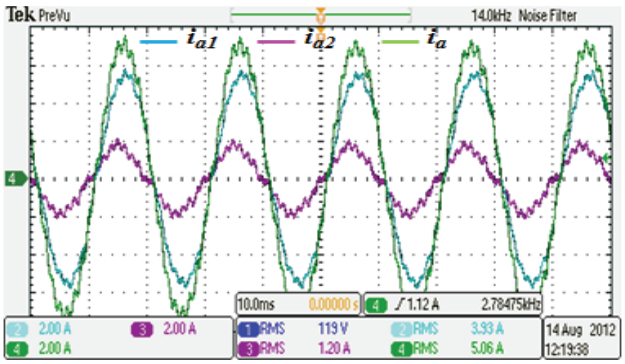
A. Passive R-L Load

Three single-phase resistors (10Ω ± 10%) and inductors (10mH ± 10%) were used to construct the three-phase passive load of the test rig. A photograph of the test rig with the passive *R-L* load is shown in Fig. 9(b). Fig. 10(a) shows converter and load current waveforms without any form of current sharing control. It can be seen that there is significant imbalance and distortion. The "current imbalance ratio" between the converters, defined as the difference in the converter currents relative to the total load current, was measured at 37.68%, which leads to uneven thermal stress and likely switch failure. Fig. 10(b) shows current waveforms when the proposed controller is activated. Good current distribution is achieved with a lower distortion and a current imbalance ratio of around 3.3%, despite the presence of a significant imbalance in the load impedances. Fig. 11 demonstrates the transient performance of the proposed controller during an abrupt change in the desired quadrature axis load current from 4A to 6A.

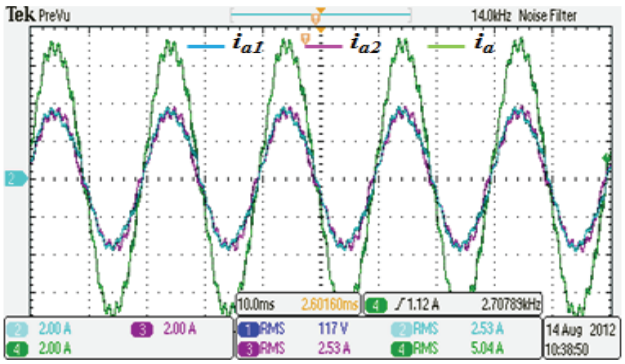
B. Three-Phase Induction Motor Load

In these tests, the passive *R-L* load was replaced by a three-phase, 2.2 kW induction motor (with the same previously mentioned deliberate imbalances in the inter-module reactors and switching dead times). Open loop constant Volt/Hertz control with a ramp function was implemented to generate the required SVPWM modulation index. The internal current sharing control loop was not affected by the type of load and it remains intact. Fig. 12(a) shows the stator and converter currents without any form of current sharing control. The current distribution is clearly unequal with a substantial current imbalance ratio of 53.9%. Activation of the proposed average current sharing controller [Fig. 12(b)] results in excellent current sharing between the two converters with a current imbalance ratio of only 0.2%.

Figs. 13-14 show corresponding current waveforms at lower stator frequencies, which provides further validation of the

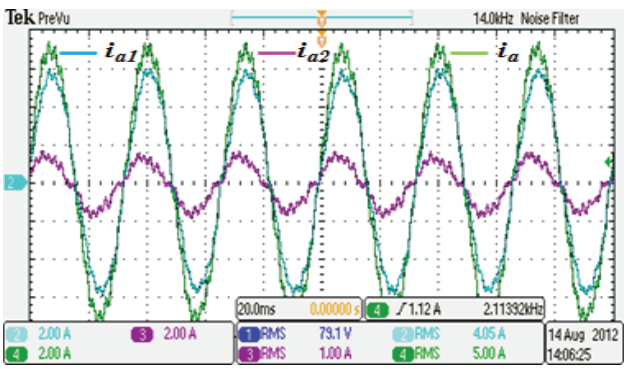


(a)

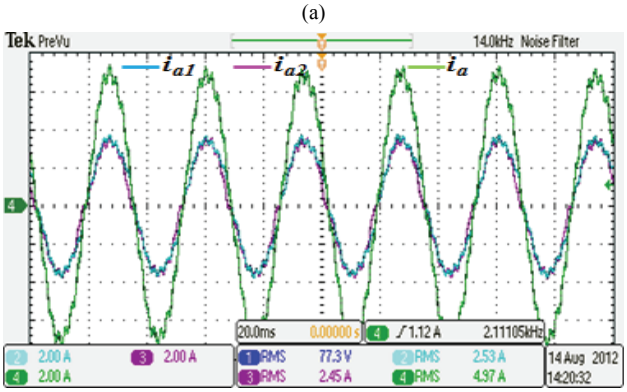


(b)

Fig. 12. Experimental current waveforms at 50 Hz, induction motor load (2A/div, 10ms/div). (a) With the current sharing controller de-activated. (b) With the current sharing controller.

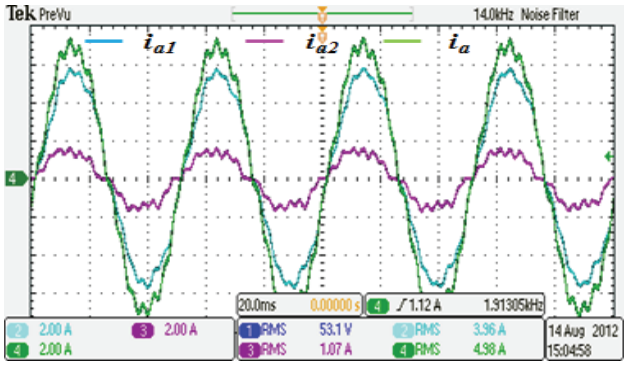


(a)

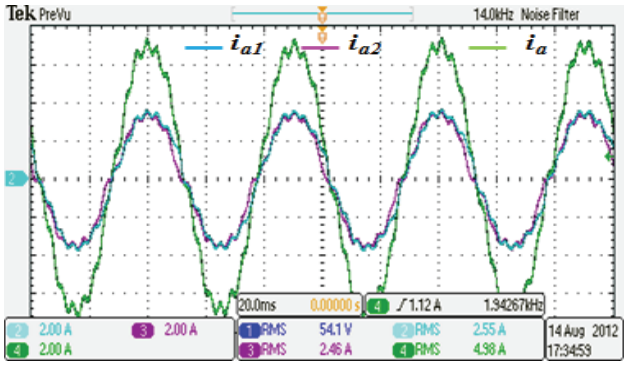


(b)

Fig. 13. Experimental current waveforms at 30 Hz, induction motor load (2A/div, 10ms/div). (a) With the current sharing controller de-activated. (b) With the current sharing controller.



(a)



(b)

Fig. 14. Experimental current waveforms at 20 Hz, induction motor load (2A/div, 10ms/div). (a) With the current sharing controller de-activated. (b) With the current sharing controller.

effectiveness of the proposed control strategy. At 30 Hz, the current unbalance ratio is 58% without current distribution control [Fig. 13(a)] and is reduced to 1.6% when the proposed control is activated [Fig. 13(b)]. Similarly, at 20 Hz, the current unbalance ratio was reduced from 61% without current control [Fig. 14(a)] to 1.8% when the proposed controller was activated [Fig. 14(b)]. Better current sharing performance was obtained at higher frequencies due to the increase in the circulating current impedance.

VI. Conclusion

A new average current control method, based on the calculation of the current space vector magnitude, is proposed in this paper for current sharing control in parallel connected three-phase converters. The proposed current sharing control method requires each converter to use only one PI compensator in the current sharing control loop. The proposed method achieves an excellent current distribution with no adverse effects on the converter common coupling point voltage. This strategy is demonstrated with two parallel connected converters employing conventional Space Vector PWM (SVPWM). However, it can be used with any PWM control scheme and can be straightforwardly extended to more than two converter units.

The proposed controller is experimentally verified using a

test circuit comprised of two parallel connected, 1.25kVA three-phase voltage fed converters. The obtained results show that the new average current control strategy achieves good current distribution between the converters. In addtion, it reduces the value of the imbalance current ratio in the laboratory test circuit from 53.9% to only 0.2% when driving a three-phase induction motor load.

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