Soft-Switching T-Type Multilevel Inverter

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Abstract

In order to improve the conversion efficiency and mitigate the EMI problem of conventional hard-switching inverters, a new soft-switching DC-AC inverter with a compact structure and a low modulation complexity is proposed in this paper. In the proposed structure, resonant inductors are connected in series for the arm branches, and resonant capacitors are connected in parallel for the neutral point branches. With the help of resonant components, the proposed structure achieves zero-current switching on the arm branches and zero-voltage switching on the neutral point branches. When compared with state-of-art soft-switching topologies, the proposed topology does not need auxiliary switches. Moreover, the commutation algorithm to realize soft-switching can be easily implemented. In this paper, the principle of the resonant operation of the proposed soft-switching converter is presented and its performance is verified through simulation studies. The feasibility of the proposed inverter is evaluated experimentally with a 2.4-kW prototype.

Key words: Multilevel inverter, Soft switching, T-type topology, ZVZCS

I. INTRODUCTION

Multilevel inverters have been widely utilized in high power conversion systems due to their ability to reduce the harmonic distortion of the AC-side waveforms and the voltage stress of power semiconductors [1]. The topologies of conventional multilevel inverters include diode-clamped multilevel inverters, capacitor-clamped multilevel inverters, T-type multilevel inverters, nested multilevel inverters, cascaded H-bridge multilevel inverters, and modular multilevel inverters [1]-[7]. All of these topologies operate at the hard-switching mode, which results om extra switching losses and high dv/dt problems.

One of the aforementioned topologies, which is very attractive for industrial applications, is the hard-switching T-type inverter [7]. However, due to the severe commutation condition of the hard-switching mode for this topology, a high voltage drop and a high current appeared at the same time on the switches during very short turn-on and turn-off transients, which introduces considerable switching losses. The reverse recovery current of the freewheeling diode and

the tailing current of the IGBT make the switching losses and EMI problem even worse. These switching losses limit the switching frequency of the converters for medium-power and high-power applications [1].

The severe commutation condition also results in a high voltage overshoot due to the stray inductance of the commutation loop and a high current overshoot due to the reverse recovery effect of the freewheeling diodes. Fast changes of the voltage during switching transients also leads to a high dv/dt problem, which is the source of conducted emissions and radiated emissions [8]. The high dv/dt at the output voltage also causes a transmission line effect for long cables which is unfriendly for loads [9], [10]. Soft-switching techniques are possible solutions to mitigate these problems for multilevel DC-AC inverters.

Soft-switching techniques for DC-AC inverters have been developing for the past several decades [11]-[27]. These techniques can be categorized as: resonant DC-link based inverters [12]-[14], resonant pole based inverters [15]-[17], AC-link based inverters [18]-[20], and soft-switching multilevel inverters [21]-[27]. With the help of auxiliary switches and different resonant principles, the zero-voltage switching or zero-current switching can be obtained for these topologies. The soft-switching techniques helps reduce switching losses and decrease dv/dt significantly. Therefore, the volume of the heat sink and the EMI filter can be easily reduced. The

soft-switching topology can also help to improve the switching frequency of the inverter, and the volume of the output filter can be reduced. At the same time, the soft-switching topology provides a good commutation condition. As a result, the dynamic voltage average problem is solved and the power semiconductors can be easily connected in series to construct high voltage inverters.

However, all of the aforementioned topologies have disadvantages that limit their application. The auxiliary resonant commutated pole converter is constructed by paralleling the main switches with a resonant capacitor and importing an auxiliary commutation branch. In this structure, the extra active switches and passive components increase the complexity of the inverter. AC-link based inverters need very few passive components and do not need auxiliary switches. However, their commutation and modulation algorithms are too complicated to implement.

T-type based soft-switching multilevel inverters with passive snubber circuits were proposed in [21]-[23]. Although these topologies can achieve zero-voltage zero-current switching, additional diodes, capacitors and inductors are required as passive snubber circuits. This requirement increases the volume and total cost of the converter. Soft-switching topologies with active snubber circuits for T-type three-level converters were proposed in [24]-[26]. The additional power semiconductors and passive components significantly increase the control complexity and reduce the robustness of the converters. All of the state-of-art soft-switching techniques for T-type converters need additional semiconductors, capacitors, and inductors of the auxiliary commutation circuits. This increases the number of components, size, overall cost, and control complexity.

The quasi-resonant technique has been fully researched in DC-DC conversion applications [28]-[31]. With the help of quasi-resonant operation, the switching losses can be significantly decreased. However, all of these studies focused on DC-DC converters. The converter output voltage magnitude can be regulated with quasi-resonant technique, but the voltage polarity cannot be changed.

A new T-type zero-voltage zero-current switching (ZVZCS) three-level converter [27] is introduced in this paper. The proposed topology combines the T-type structure and the quasi-resonant technique. In this structure, the resonant inductors are connected in series with the arm branches, and the resonant capacitors are connected in parallel with the neutral point branches. When compared with conventional soft-switching DC-AC topologies [11]-[26], this topology has a compact structure and does not require auxiliary power semiconductors. The number of passive components is also reduced. In this paper, the operation of the soft-switching T-type DC-AC converter is explained in greater detail and more analysis are added for soft-switching operation. The parameter analysis and the selection of circuit components
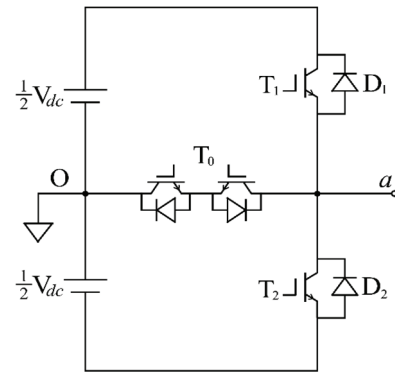

Fig. 1. Conventional single-phase T-type three-level inverter.

are also illustrated. Moreover, a loss calculation and a FFT analysis are added and compared to conventional hard-switching converters. Experimental results are also added to this paper to validate the feasibility of the proposed soft-switching converter.

This paper is organizing as follows. The operation principle of the proposed soft-switching T-type multilevel converter is presented in Section II. In Section III, the parameter analysis and design considerations are illustrated. The results of simulations, loss calculations, and FFT analyses are shown in section IV. Section V demonstrates the results of an experimental implementation. Finally, some conclusions are given in section VI.

II. OPERATION PRINCIPLE OF THE PROPOSED INVERTER

A. Conventional T-Type Inverter

The topology of a conventional single-phase T-type three-level inverter is shown in Fig. 1. In the T-type inverter, each phase is constructed by one bidirectional switch and two unidirectional switches [2]. The bidirectional switches provide a controllable path between the load terminal and the neutral point of the inverter. A three-level output voltage can be generated by selecting different switches to be turned on [27].

The voltage from the load terminal to the neutral point is ½ V_{dc} when T_1 is ON, it is -½ V_{dc} when T_2 is ON, and it is zero when the bidirectional switch T_0 is ON. Through a proper modulation algorithm, such as three-level SPWM or SVPWM, a sinusoidal output can be obtained. It should be noted that, for hard-switching operation, the dead band must be preserved between two different switching states.

B. Proposed Soft-Switching T-Type Inverter

Fig. 2 shows the proposed single-phase soft-switching T-type three-level inverter. Two resonant inductors L_{r1} and L_{r2} are connected in series with the switches T_1 and T_2, respectively. In addition, a resonant capacitor C_r is connected in parallel with the bidirectional switch T_0. This circuit structure determines the zero-voltage turn-off for T_0 and the
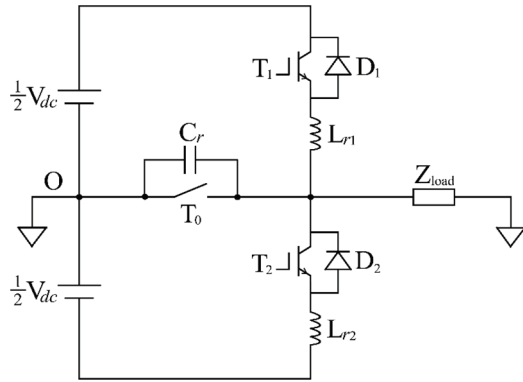
Fig. 2. Proposed single-phase soft-switching T-type three-level inverter.

TABLE I
SWITCHING STATE AND CIRCUIT STATE

	Switching State	Circuit State
Positive half-cycle	T_0 ON, T_1 OFF	T_0 Freewheeling
	T_0 OFF, T_1 ON	Quasi-Resonant
	T_0 OFF, T_1 OFF	D_1 Freewheeling
Negative half-cycle	T_0 ON, T_2 OFF	T_0 Freewheeling
	T_0 OFF, T_2 ON	Quasi-Resonant
	T_0 OFF, T_2 OFF	D_2 Freewheeling

zero-current turn-on for both T_1 and T_2. By designing an accurate turn-on time for T_0 and accurate turn-off times for T_1 and T_2, the zero-voltage turn-on for T_0 and the zero-current turn-off for T_1 and T_2 can be obtained.

As shown in Fig. 2, the proposed soft-switching T-type inverter has a symmetrical structure, which means that during a positive half-cycle, T_0 and T_1 turn on and off alternatively to generate output voltage, while during a negative half-cycle, T_0 and T_2 switch alternatively to generate output voltage.

The switching states and corresponding circuit states of the proposed soft-switching T-type inverter are shown in Table I and in Fig. 3. Since the proposed topology has a symmetrical structure, operation during the positive half-cycle of a sinusoidal period is similar to operation during the negative half-cycle. For the sake of simplicity, only the resonant modes during the positive half-cycle are analyzed.

During the positive half-cycle, assuming that the initial state of the inverter is T_0 freewheeling. T_0 is in the turn-on state with a load current and T_1 is in the turn-off state. At the initial state, the output voltage is zero. At time zero, T_0 is turned off with ZVS due to a parallel-connection with C_r. T_1 is turned on with ZCS since this switch is in a series-connection with L_{r1}. From this moment, the resonant process begins. Ignoring the voltage drop of the power semiconductors, an equivalent circuit during the resonant process is shown in Fig. 4. The relationship between the voltage of resonant capacitor and the current of the resonant inductor is described by (1) and (2). The initial conditions of the resonant process are given as $u_{Cr}(0) = 0$ and $i_{Lr}(0) = 0$.
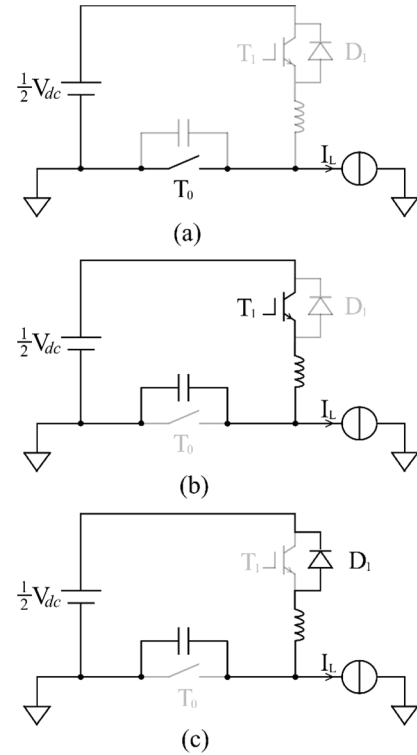

Fig. 3. Circuit states. (a) T_0 is ON and T_1 is OFF. (b) T_0 is OFF and T_1 is ON. (c) T_0 and T_1 are OFF.
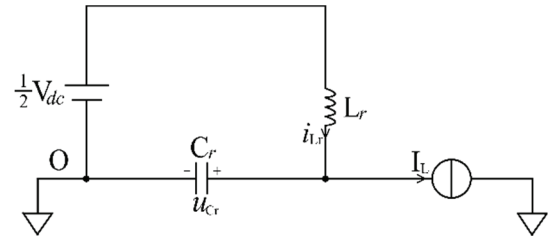

Fig. 4. Equivalent circuit when T_0 is OFF and T_1 is ON.

$$C_r \frac{du_{cr}}{dt} = i_{Lr} - I_L \tag{1}$$

$$L_r \frac{di_{Lr}}{dt} = \frac{1}{2}V_{dc} - u_{cr} \tag{2}$$

By defining the characteristic impedance and resonant frequency of the resonant network, which are $Z_r = \sqrt{\frac{L_r}{C_r}}$ and $\omega_r = \frac{1}{\sqrt{L_r C_r}}$, the capacitor voltage u_{cr} and inductor current i_{Lr} can be given by (3) and (4), respectively.

$$u_{cr} = \frac{1}{2}V_{dc} - \frac{1}{2}V_{dc}cos\omega_r t - I_L Z_r sin\omega_r t \tag{3}$$

$$i_{Lr} = I_L + \frac{1}{Z_r}\left(\frac{1}{2}V_{dc}sin\omega_r t - I_L Z_r cos\omega_r t\right) \tag{4}$$

(3) and (4) can be further simplified and given as (5) and (6).

$$u_{cr} = \frac{1}{2}V_{dc} - V_r cos(\omega_r t - \theta_r) \tag{5}$$

$$i_{Lr} = I_L + \frac{V_r}{Z_r} sin(\omega_r t - \theta_r) \tag{6}$$

where:

$$V_r = \sqrt{(V_{dc}/2)^2 + (I_L Z_r)^2} \tag{7}$$

$$\theta_r = arcin(I_L Z_r / V_r) \tag{8}$$

To obtain ZVS for the neutral point branch and ZCS for the arm branch, (9) and (10) should be satisfied. (9) makes sure the neutral point switch voltage can be decreased to zero, and (10) makes sure the arm switch current can be decreased to a negative value. According to the definition in (7), it is possible to find that (9) and (10) are always satisfied.

$$V_{dc} < 2V_r \tag{9}$$

$$I_L < V_r / Z_r \tag{10}$$

During the resonant process, the maximum voltage on the neutral point switch and the maximum current on the arm switch are given by (11) and (12). The voltage stress and current stress provide a guide to select semiconductor switches. Typically, a high resonant impedance gives a high voltage stress and a low current stress on the switches, while a low resonant impedance gives a low voltage stress and a high current stress on the switches. The current stress for the neutral point switches is the same as the conventional T-type converter.

$$u_{Cr(max)} = \frac{1}{2} V_{dc} + V_r \tag{11}$$

$$i_{Lr(max)} = I_L + \frac{V_r}{Z_r} \tag{12}$$

If T_1 is turned off when the free-wheeling diode is conducting, i.e. i_{Lr} is negative, ZCS of T_1 is achieved. The beginning of this interval is given as (13), and (14) shows the ending of this interval. The middle time point T_{1on} is defined and given by (15).

$$t_1 = \frac{\pi + 2\theta_r}{\omega_r} \tag{13}$$

$$t_2 = \frac{2\pi}{\omega_r} \tag{14}$$

$$T_{1on} = \frac{t_1 + t_2}{2} = \frac{3\pi + 2\theta_r}{2\omega_r} \tag{15}$$

The instant when the resonant capacitor voltage u_{Cr} decreases to zero is given by (16). This moment is defined as T_{on}, and it is a constant value. If T_0 is turned on at this moment, ZVS for T_0 can be achieved.

$$T_{on} = \frac{2\pi}{\omega_r} \tag{16}$$

After T_0 is turned on, the freewheeling state can be sustained as long as necessary.

The interval of the freewheeling state where T_0 turns on is defined as T_{off}, which is a controllable input variable for the proposed soft-switching T-type inverter. The next resonant
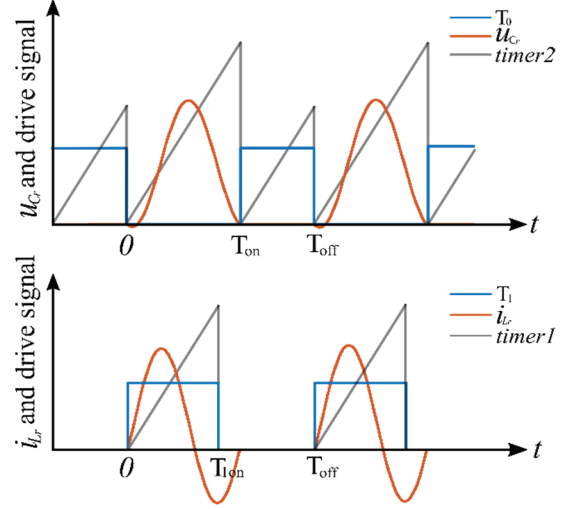

Fig. 5. Modulation principle of the proposed soft-switching T-type inverter.

cycle repeats after the freewheeling state ends. This resonant principle guarantees soft-switching operation for all of the switches.

In the following, a principle based on pulse density modulation is presented to generate a sinusoidal voltage for an AC load. The average output voltage, during the resonant process, can be calculated by (17).

$$V_{average} = \frac{1}{T_{on}} \int_0^{T_{on}} \frac{1}{2} V_{dc} - V_r cos(\omega_r t - \theta_r) \, dt$$
$$= \frac{1}{2} V_{dc} \tag{17}$$

During the interval of the freewheeling state, the output voltage is zero. This interval can be sustained as long as necessary. Therefore, the output voltage can be modulated by selecting an appropriate T_{off}. (18) shows how an appropriate T_{off} is chosen according to the pulse density modulation theorem.

$$\frac{T_{on}}{T_{on} + T_{off}} V_{average} = |V_{ref} sin(\omega t + \theta)| \tag{18}$$

where V_{ref} is the reference output voltage magnitude. Therefore, T_{off} can be expressed by (19).

$$T_{off} = T_{on} \left(\frac{V_{average}}{|V_{ref} sin(\omega t + \theta)|} - 1 \right) \tag{19}$$

A diagram of the proposed modulation method is shown in Fig. 5 and is summarized as follows.

At the beginning of each resonant cycle, the load current I_L is sampled and the turn on time of T_1 is calculated through (15). Then the turn on time of T_0 is calculated by (19). The turn off time of T_0 is calculated by (16), which is a constant value. Then T_1 turns on, T_0 turns off and the resonant cycle begins. Two timers are required to implement the modulation algorithm. Timer1 counts T_{1on} and after the T_{1on} interval, T_1
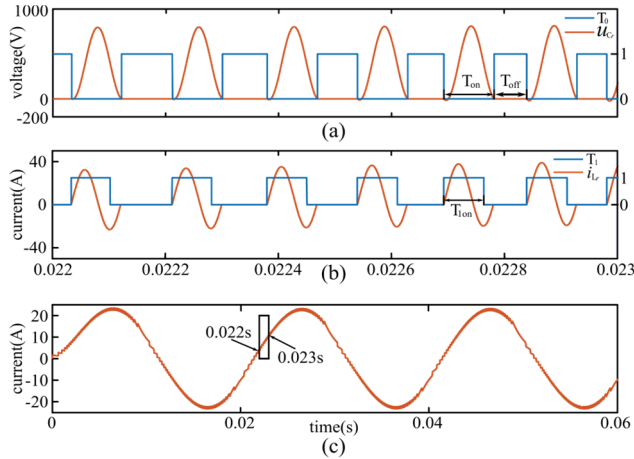
Fig. 6. Operation principle of the proposed soft-switching T-type inverter. (a) u_{Cr} and T_0 gate signal. (b) i_{Lr} and T_1 gate signal. (c) Load current.

Fig. 7. Topology diagram of the proposed three-phase soft-switching T-type inverter.

turns off with ZCS. Timer2 counts T_{on} and after the T_{on} interval, T_0 turns on with ZVS. Then timer2 resets and T_{off} starts counting. After the T_{off} interval, the load current is sampled again and the same calculations should be done for the next pulse cycle.

The aforementioned principle can be applied to the negative half-cycle with minor changes, where $V_{ref}sin(\omega t + \theta)$ has a negative sign. It should be noted that the reference direction of I_L should be changed when calculating the turn-on time of the lower arm switch T_2. Fig. 6 shows a typical waveform for this operation principle.

C. Proposed Three-Phase Soft-Switching T-Type Inverter

Fig. 7 shows a topology diagram of the proposed three-phase soft-switching T-type inverter. Each of the phases is modulated and controlled individually, which is similar to single-phase modulation. The only difference is that the modulating signals should be phase-shifted by 120 degrees.

In order to improve the voltage utilization of the DC-link, the third-harmonic can be injected into the modulation scheme. With the help of third-harmonic injection modulation, the output voltage magnitude can be 15.5% higher than the modulation algorithm given by (18) and (19) at the same voltage rating of the DC-link. A modulation algorithm with third-harmonic injection is given by (20) and (21).

$$\frac{T_{on}}{T_{on} + T_{off}} V_{average} = \left| V_{ref}sin(\omega t + \theta) + \frac{1}{6}V_{ref}sin(3\omega t + 3\theta) \right| \tag{20}$$

$$T_{off} = T_{on}\left(\frac{V_{average}}{\left| V_{ref}sin(\omega t + \theta) + \frac{1}{6}V_{ref}sin(3\omega t + 3\theta) \right|} - 1 \right) \tag{21}$$
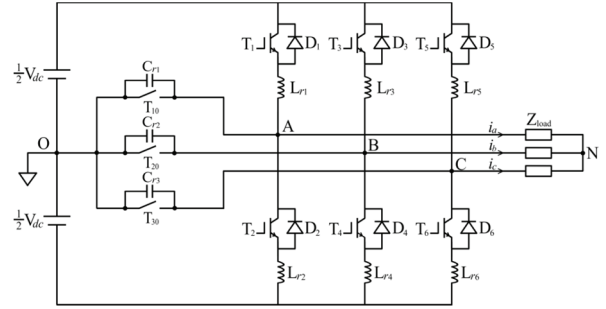
III. Design Considerations for the Soft-Switching T-Type Inverter

A. Parameters Design of the Soft-Switching T-Type Inverter

The critical parameters of the soft-switching T-type inverter include the output current, output voltage, DC-link voltage, characteristic impedance and resonant frequency. To reduce the DC-link voltage and the voltage stress of the components, third-harmonic injection modulation is implemented when designing the parameters of the soft-switching T-type inverter.

For a 2.4-kW prototype with an output phase voltage of $110V_{rms}$ and a line frequency of 60Hz, the line current can be calculated by (22). At unit power factor, the line current is calculated as $7.3A_{rms}$.

$$I_{L\_rms} = \frac{P_N}{3V_{PH\_rms}cos\varphi_N} \tag{22}$$

With the third-harmonic injection modulation, the minimum DC-link voltage is given by (23). For a $110V_{rms}$ output voltage, the minimum DC-link voltage is 270V, and consider the voltage fluctuation of the neutral point, the DC-link voltage is selected as 300V.

$$V_{dc(min)} = V_{PH\_rms}\sqrt{6} \tag{23}$$

The resonant frequency determines the size of the resonant components and the size of the output filter. A higher resonant frequency can significantly decrease the inductance and the capacitance of the resonant network. To show the advantages of the proposed soft-switching T-type inverter, the resonant frequency is selected in the range from 50kHz to 100kHz.

The characteristic impedance determines the voltage stress of the resonant capacitor and the current stress of the resonant inductor. Since the neutral point switch is paralleled with the resonant capacitor, they have the same voltage stress. Since the arm switch is in series with the resonant inductor, they have the same current stress. When compared with the conventional hard-switching T-type inverter, the proposed soft-switching T-type inverter has extra voltage stress for the neutral point switch as given in (24), and extra current stress for the arm switch as given in (25).

$$V_{stress\_extra} = \sqrt{(V_{dc}/2)^2 + (I_L Z_r)^2} \qquad (24)$$

$$I_{stress\_extra} = \sqrt{\left(\frac{V_{dc}}{2Z_r}\right)^2 + I_L^2} \qquad (25)$$

To limit the voltage stress, it is fair to assume that (26) is satisfied, so the extra voltage stress is less than the DC-link voltage.

$$V_{stress\_extra} = \sqrt{(V_{dc}/2)^2 + (I_L Z_r)^2} < V_{dc} \qquad (26)$$

To limit the current stress, it is fair to assume that (27) is satisfied, so the extra current stress is less than twice the peak line current.

$$I_{stress\_extra} = \sqrt{\left(\frac{V_{dc}}{2Z_r}\right)^2 + I_L^2} < 2I_L \qquad (27)$$

For most applications, the range of the characteristic impedance can be calculated and is given by (28).

$$\frac{V_{dc}}{2\sqrt{3}I_L} < Z_r < \frac{\sqrt{3}V_{dc}}{2I_L} \qquad (28)$$

Considering that the resonant inductor is heavier and occupies a larger area than the resonant capacitor, for the first prototype, a lower characteristic impedance is selected which is given by (29). It should be noted that I_L is the peak line current.

$$Z_r = \frac{V_{dc}}{4I_L} \qquad (29)$$

The resonant frequency is selected to be around 70kHz. According to the definition of the characteristic impedance and resonant frequency, the parameters of the resonant network are calculated as $L_r = 17.6uH$ and $C_r = 0.33uF$.

B. Voltage and Current Stress of the Components

With the design parameters, the voltage and current stress of the passive components and semiconductor switches can be calculated. The neutral point switch and the resonant capacitor have the same voltage stress, which is given by (30).

$$u_{Cr(max)} = \frac{1}{2}V_{dc} + \sqrt{(V_{dc}/2)^2 + (I_L Z_r)^2} \qquad (30)$$

According to (30), the voltage stress of the neutral point branch is 317.7V. The current stress of the neutral point switch is the peak line current, which is 10.3A.

The arm switch and the resonant inductor have the same current stress, which is given by (31).

$$i_{Lr(max)} = I_L + \sqrt{\left(\frac{V_{dc}}{2Z_r}\right)^2 + I_L^2} \qquad (31)$$

According to (31), the current stress of the arm branch is 33.4A. The voltage stress of the arm switch is given by (32), which is calculated as 467.7V for the prototype.
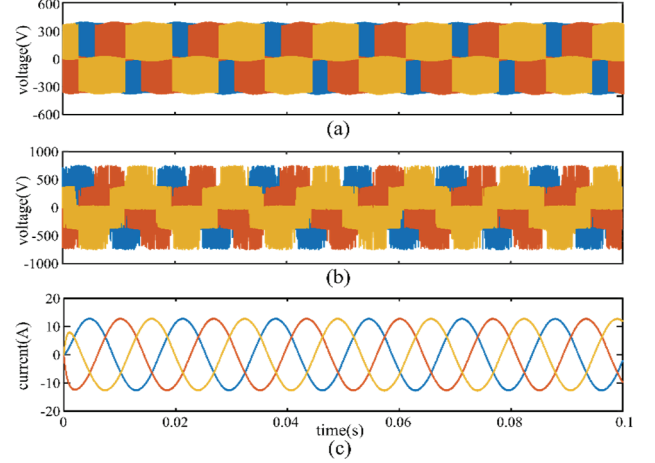

Fig. 8. Simulation results of the proposed three-phase soft-switching T-type inverter. (a) Voltage from the terminal to the neutral point V_{ABCO}. (b) Line-to-line voltage V_{AB}, V_{BC}, and V_{CA}. (c) Output current i_{abc}.
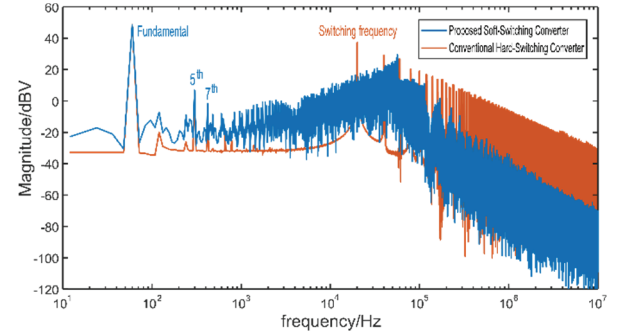

Fig. 9. FFT analysis of simulated phase voltage.

$$u_{arm(max)} = V_{dc} + \sqrt{(V_{dc}/2)^2 + (I_L Z_r)^2} \qquad (32)$$

With the calculated voltage and current stress, the passive components and semiconductor switches can be selected.

IV. SIMULATION RESULTS AND LOSS ANALYSIS

A. Simulation Results

To verify the proposed modulation algorithm of the soft-switching T-type inverter, simulation studies are implemented through MATLAB/Simulink. The simulation parameters are given as $V_{dc} = 300V$, $L_r = 17.6uH$, $C_r = 0.33uF$, $R_{load} = 15\Omega$, $L_{load} = 6mH$, $V_{PH\_rms} = 110V$, $f = 60Hz$, $P_N = 2.4kW$, and $cos\varphi_N = 0.98$.

Fig. 8 shows simulation results of the output voltage and current. For a comparison with a conventional hard-switching converter, a FFT analysis is implemented for the phase voltage, and the result is shown in Fig. 9. It can be seen that the high frequency noise is effectively suppressed. Unlike the conventional hard-switching converter, which has high harmonics located at the switching frequency and its extension, the proposed soft-switching converter utilizes pulse density

TABLE II
LOSS PARAMETERS OF THE IKW40N120H3

	Expression
V_{CE} (V)	$1.0 + 0.038I_C$
V_F (V)	$1.4 + 0.031I_D$
E_{on} (mJ)	$0.001I_C^2 + 0.06I_C + 0.3$
E_{off} (mJ)	$0.0667I_C$

modulation and the harmonics caused by the switching action are spread to a wide range. These characteristics make it easier for the proposed soft-switching converter to meet EMI standards when connected to a power grid.

According to the obtained simulation results, the THD of the terminal to neutral point voltage V_{ABCO} is 117.59%, the THD of the line-to-line voltage is 95.02%, and the THD of the output current i_{abc} is 0.99%.

B. Loss Calculation and Comparison

In order to compare the efficiency of the proposed inverter with a conventional hard-switching inverter, a conventional T-type inverter was also designed and simulated at the same voltage and power ratings.

The power switches of both inverters are IKW40N120H3. The bidirectional switch is constructed by two IGBTs that are connected in anti-series. The switching frequency of the hard-switching T-type inverter is 20 kHz. Based on the datasheet of the IKW40N120H3, the voltage drop and switching loss are given in Table II.

The conduction loss for one switch is calculated by (33), where T is a fundamental period. The total conduction loss is the sum of three neutral point switches and six arm switches.

$$P_{loss\_con} = \frac{1}{T}\int_0^T (V_{CE}I_C + V_F I_D)\, dt \qquad (33)$$

The switching loss for one switch is calculated by (34). Since the reverse recovery loss is not given in the datasheet, this loss is ignored when calculating the total loss of the hard-switching T-type inverter. The total switching loss is the sum of three neutral point switches and six arm switches.

$$P_{loss\_sw} = \frac{1}{T}\sum_T E_{on}(I_C) + E_{off}(I_C) \qquad (34)$$

Considering the ESR of resonant inductors, the loss of the resonant inductors must be calculated. The resonant inductors utilized in these experiments are SRP1770TA-2R2Ms which give a total ESR of 19.2mΩ for each arm [32]. The resonant inductor loss for one arm is calculated by (35). The total ESR loss of the resonant inductors is the sum of six arms.

$$P_{ESR\_loss\_inductor} = \frac{1}{T}\int_0^T R_L i_L^2\, dt \qquad (35)$$

The core loss of the resonant inductor is also estimated. According to the Steinmetz equation, which is given in (36),

the core loss is related to the core material (K_1, α, β), the resonant frequency (f), and the flux swing (ΔB). The core material of the SRP1770TA-2R2M is carbonyl powder, and the characteristics are given in [33]. According to the characteristics of carbonyl powder, at the resonant frequency, the core loss of the resonant inductors is estimated to be around 10% of the ESR loss. Thus, the core loss is ignored in the efficiency calculation.

$$P_{core\_loss\_inductor} = K_1 f^\alpha \Delta B^\beta \qquad (36)$$

Considering the voltage drop on the semiconductors and the ESR of the resonant inductors, the voltage of the resonant capacitor cannot go back to zero exactly after one resonant period is over. The remaining voltage on the resonant capacitor causes extra switching loss for the soft-switching T-type inverter. The extra switching loss for one neutral point switch is calculated by (37), where V_{Cr0} is the remaining voltage of the resonant capacitor, which is about 5V. The total extra switching loss is the sum of three neutral point switches.

$$P_{loss\_extra\_sw} = \frac{1}{T}\sum_T \frac{1}{2} C_r V_{Cr0}^2 \qquad (37)$$

For the conventional hard-switching T-type inverter, the conduction loss and switching loss are considered. For the proposed soft-switching T-type inverter, the conduction loss, the extra switching loss, and resonant inductor loss are considered. The results of the loss calculation are shown in Table III. As can be seen from the table, the dominant power loss in the proposed soft-switching inverter is the conduction loss of the arm switches. Meanwhile, for the hard-switching inverter, the dominant power loss is the switching loss of both the arm switches and the neutral point switches.

It can be seen that although the proposed soft-switching T-type inverter has higher conduction losses, the total power losses have been significantly reduced when compared with the conventional hard-switching inverter, which is about 5% in the full-load condition.

It should also be noted that the switching frequency of the proposed inverter is almost three time higher than that of the hard-switching inverter. Thus, the proposed inverter has a better output THD for a given output filter.

V. EXPERIMENTS

A prototype of the proposed inverter with a rated output power of 2.4 kW was made to verify the feasibility of the new topology. To show the advantage of the soft-switching inverter, the resonant frequency was set to a relative high value, which is 66.8 kHz. All of the design parameters of the prototype are the same as those of the simulation model. The selection of the passive components and semiconductor switch are shown in Table IV.

The resonant inductor is constructed by 8 high current

TABLE III
POWER LOSS COMPARISON BETWEEN THE PROPOSED SOFT-SWITCHING INVERTER AND A CONVENTIONAL HARD-SWITCHING INVERTER

Load Power Loss (W)	25%		50%		75%		100%	
	Hard Switching Inverter	Proposed ZVZCS Inverter	Hard Switching Inverter	Proposed ZVZCS Inverter	Hard Switching Inverter	Proposed ZVZCS Inverter	Hard Switching Inverter	Proposed ZVZCS Inverter
Conduction losses of arm switches	4.62	37.79	10.01	40.26	16.04	44.48	22.55	50.15
Conduction losses of neutral point switches	4.64	4.57	9.85	9.47	15.67	14.74	22.10	20.40
Switching losses of arm switches	33.64	-	49.71	-	65.96	-	82.18	-
Switching loss of neutral point switches	33.85	7.20	50.43	7.20	67.22	7.20	84.16	7.20
Resonant inductor losses	-	7.73	-	8.82	-	10.55	-	12.86
Efficiency	87.87%	91.07%	90.40%	94.76%	91.07%	95.83%	91.25%	96.23%

TABLE IV
PARAMETERS OF THE EXPERIMENT SETUP

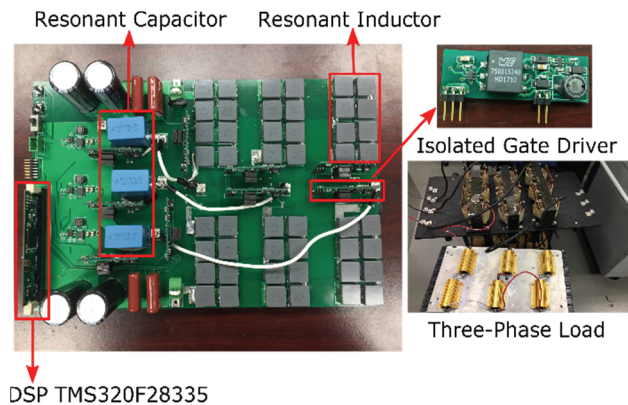| Component	Value
Resonant Inductor	SRP1770TA-2R2M
Resonant Capacitor	B32654A7334J
IGBT	IKW40N120H3

Fig. 10. Experimental setup.

shielded SMD inductors that are connected in series. The part number of the resonant inductor is SRP1770TA-2R2M. The capacitance of the resonant capacitor is 0.33μF, which gives a characteristic impedance of 7.3Ω. According to (32) and (31), the voltage stress of the arm switches is 467.7V, and the current stress of the arm switches is 33.4A. 1200V 40A IGBT IKW40N120H3s are selected for both the neutral point switches and the arm switches since they can provide enough of a voltage margin. It should be noted that 650V IGBTs can also be utilized, and that they achieve a higher operation efficiency.

The experiment setup is shown in Fig. 10. In the power circuit, 6 arm switches and 3 neutral point switches are driven by 9 isolated gate drivers. It should be noted that, since all of the switches are working in soft-switching mode, a 0-Ω external gate resistor can be chosen. The inverter is controlled by a TMS320F28335. The three-phase load is constructed by power resistors and inductors. For each phase, it contains a
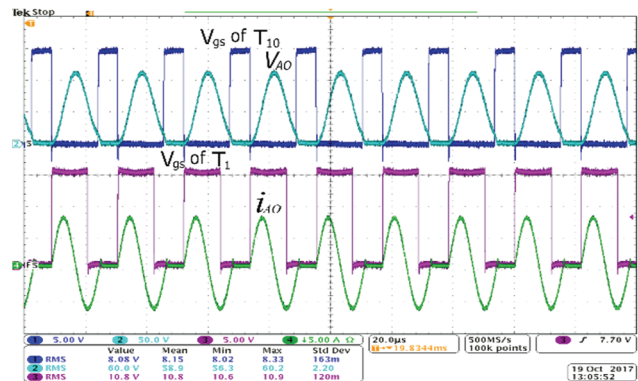

Fig. 11. Gate signals and resonant voltage/current signals during the positive half period.

resistor bank and an inductor bank, which give a total resistance of 15Ω and a total inductance of 6mH.

To validate the soft-switching operation, the gate signals and resonant voltage/current signals are measured. Fig. 11 shows gate signals of the neutral point switch and the voltage on the resonant capacitor. It can be observed that the neutral point switch is turned on when the resonant period ends. However, because of the voltage drops of the switches and the ESR of the resonant inductor, the resonant voltage cannot go back to zero exactly. The remaining resonant voltage causes extra switching losses of the neutral point switches, which is considered in loss analysis in Table III.

The gate signal of the upper arm switch and the current of the resonant branch can also be observed in Fig. 11. It can be seen that the arm switch is turned off when the current goes through the freewheeling diode, which means zero-current switching is obtained for the arm switches.

Fig. 12 shows the same signals during the negative half period. During the negative half period, the upper arm switch is never turned on.

After the soft-switching operation is validated, the three-phase operation is implemented. In Fig. 13, the line currents and one of the phase voltages are shown. Fig. 14 shows the phase voltages and one of the line currents. It can be seen that the peak of the voltage pulses is no longer constant, since the
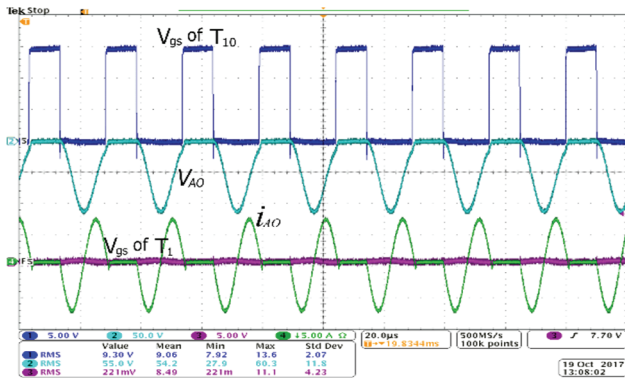
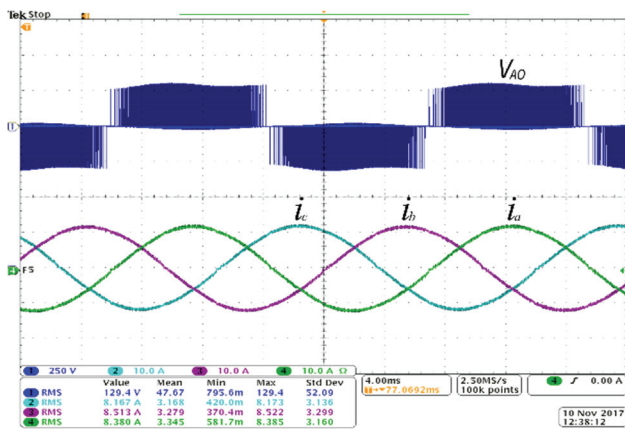Fig. 12. Gate signals and resonant voltage/current signals during the negative half period.
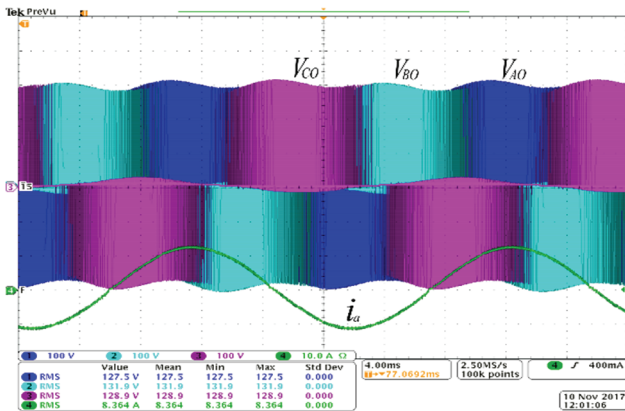

Fig. 15. Line-to-line voltage V_{AB}, V_{BC}, and V_{CA}.

Fig. 13. Line current i_{abc} and phase voltage V_{AO}.

Fig. 16. DC-link voltage V_{dc1}, V_{dc2}; phase voltage V_{AO}; line current i_a.

Fig. 14. Phase voltage V_{ABCO} and line current i_a.

Fig. 17. FFT analysis of the experimental phase voltage.

maximum resonant voltage is related to the load current. Fig. 15 shows the line-to-line voltages of the inverter.

In Fig. 16, the DC-link voltages, the phase voltage, and line current are shown. It can be seen that the well-known 6th harmonic voltage ripple appears on the DC-link.

A FFT analysis of the experimental phase voltage is implemented and shown in Fig. 17. It can be seen that the proposed soft-switching T-type inverter spreads the switching noise to a wide range around the resonant frequency of 66.8kHz. The harmonics roll off at a rate of -40dB/decade
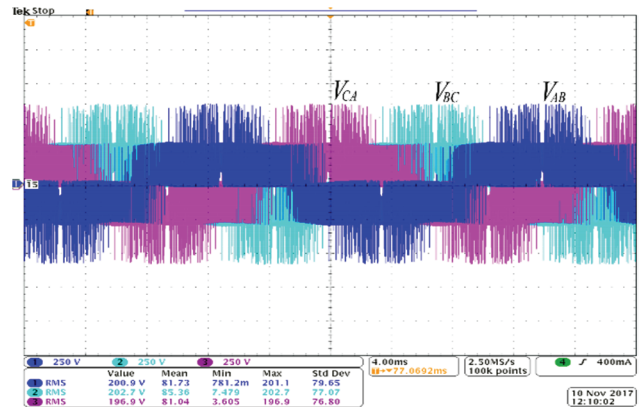
when the frequency is higher than the resonant frequency.

The efficiency of the prototype is also measured. In the full-load operation, the input power from the DC source is 2400W and the output from the inverter is 2275.9W, which gives an efficiency of 94.8% when compared with an analytical value of 96.23%. Efficiency curves at load conditions of 25%, 50%, 75% and 100% are shown in Fig. 18. The efficiency of the proposed inverter can be further increased by selecting a higher characteristic impedance, which can decrease the resonant current. The conduction loss of the semiconductor switches and the loss of the resonant
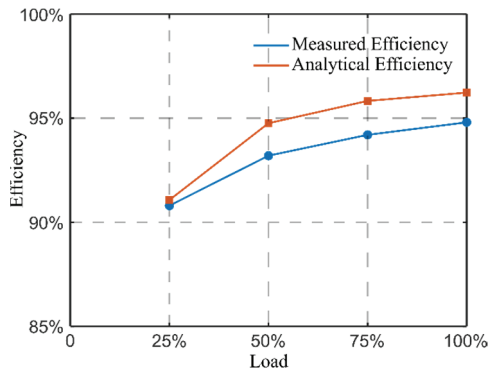
Fig. 18. Efficiency curve of the proposed soft-switching T-type inverter.

inductors are decreased with a lower resonant current, which is at the cost of a higher voltage stress.

VI. Conclusions

This paper presents a new soft-switching T-type multilevel inverter. Soft-switching operation for all of the switches is obtained through series-connecting the arm switches with resonant inductors and parallel-connecting the neutral point switches with resonant capacitors. The proposed inverter has a simple structure including two resonant inductors and one resonant capacitor for each phase. It can eliminate switching losses and accommodate the series connection of switches for high voltage applications. It can also decrease *dv/dt* at the output voltage. The pulse density based modulation algorithm also reduces the control complexity. The design considerations of the proposed soft-switching T-type inverter are illustrated. Simulation studies verify the operation of the proposed soft-switching T-type inverter. Loss calculation shows that the proposed soft-switching T-type inverter has a higher efficiency than conventional hard-switching T-type inverters. Experimental results show the feasibility of implementation for the proposed inverter.

Acknowledgment

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