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Improvement of Output Linearity of Matrix Converters with a General R-C Commutation Circuit

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ABSTRACT

In this paper, a matrix converter with improved low frequency output performance is proposed by achieving a one-step commutation owing to a general commutation circuit applicable to *n*-phase to *m*-phase matrix converters. The commutation circuit consists of simple resister and capacitor components, leading to a very stable, reliable and robust operation. Also, it requires no extra sensing information to achieve commutation, allowing for a one-step commutation like a conventional dead time commutation. With the dead time commutation strategy applied, the distortion caused by commutation delay is analyzed and compensated, therefore leading to better output linear behavior. In this paper, detailed commutation procedures of the R-C commutation circuit are analyzed. A selection of specific semiconductor switches and commutation circuit components is also provided. Finally, the effectiveness of the proposed commutation method is verified through a two-phase to single-phase matrix converter and the feasibility of the compensation approach is shown by an open loop space vector modulated three-phase matrix converter with a passive load.

Keywords: Matrix converter, Current commutation, Dead time compensation

1. Introduction

Recently, as a direct AC-AC power conversion system, increasing attention has been paid to the matrix converter in application fields where factors including smaller size, higher power density and easier maintenance are desired. The matrix converters have attractive characteristics such as sinusoidal input currents, controlled input power factor, regeneration capability along with the basic function to produce output voltages with variable amplitude and frequency. Meanwhile, continuous effort has been made to solve such revealed problems as commutation, protection and the relatively complicated switching strategy, making the matrix converters more practical. Owing to these efforts, the matrix converter finds its

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application in variable power conversion, AC drive and renewable power generation [1-2].

The key element in a matrix converter is the fully controlled four-quadrant bidirectional switches, which are capable of conducting bidirectional currents and blocking bidirectional voltages. Reliable current commutation between the bidirectional switches is very critical and practical for the safe operation of matrix converters. All the switches have to be preciously controlled so as to guarantee continuous current flow for inductive loads. A four-step commutation method based on the information of the output current direction is proposed in [3]. Furthermore, a so-called two-step semi-soft commutation method of measuring the voltage across the individual semiconductor device is found in [4]. Another technique based on the knowledge of the relative magnitudes of the input voltages is given in [5]. These mentioned techniques can handle the commutation problem.

These commutation methods, however, may have some drawbacks such as relatively long commutation time and/or requirement of high performance logic devices to shorten the commutation time. During commutation sequences, the unwanted output voltage errors occur and the resultant output voltage may be distorted. Such output voltage distortion is strictly dependent on semiconductor device characteristics and commutation delay time. Especially when the pulse width modulation (PWM) pulse is narrower than the time for completing a commutation sequence in the low frequency operation, the distorted phenomena become more severe.

Several works have been done in order to improve output linearity. A PWM pattern is proposed to avoid incomplete commutation in [6]. In [7], technique acting in an alpha-beta domain is presented to eliminate the distortion effects. In [8], a compensation technique is used to cancel nonlinear effects in the *d-q* reference domain. These methods can all help to improve the matrix converter output linearity. However, they all require relatively complicated algorithms. Moreover, if the matrix converter is used in motor drive, the compensation performed in a *d-q* reference frame or alpha-beta reference frame may be sensitive to angle measure error.

In this paper, a matrix converter with improved output linearity is proposed, which is based on a one-step commutation like a conventional dead time commutation. The one-step commutation makes it an easy task to analyze and compensate the distortion caused by commutation delay. Thus, better linear behavior output can be obtained.

The one-step commutation can be directly incorporated into the commutation circuit recently suggested in [9]. In the conventional commutation strategies, they all require extra sensing information to perform commutation. However, due to possible noise and perturbation, especially around a zero-crossing point where the direction of current or voltage is changed, sensors may have some measuring ambiguity. The commutation circuit in [9] utilizes a simple R-C circuit as a commutation aid, eliminating the need of current or voltage sensing, which leads to a stable and reliable operation.

In this paper, the R-C commutation circuit analysis and the operating principle of the general commutation circuit are dealt with for self-completeness. Also, the verification and validity of the proposed commutation method are shown by experimental results. Finally, the effectiveness of the proposed compensation method is verified by an open loop space vector modulated matrix converter with passive load.

2. General R-C Commutation Circuit

2.1 Review of commutation techniques

Reliable current commutation between switches in matrix converters is more difficult than in conventional voltage source inverters because there are no natural freewheeling paths. The commutation has to be actively controlled at all times with respect to two basic rules. These rules can be visualized by considering just two switch cells on one output phase of a matrix converter. It is important that no two bidirectional switches are switched on at any instant. This would result in line-to-line short circuits and the destruction of the converter due to over currents. Also, the bidirectional switches for each output phase should not all be turned off at any instant. This would result in the absence of a path for the inductive load current, causing large over voltages. These two considerations cause a conflict because semiconductor devices cannot be switched instantaneously

due to propagation delays and finite switching times.

Various solutions for commutation were proposed. In [3], a four step commutation strategy is given. By sensing the output current direction and gating the switches in a specific determined sequence, the direction of current flow through the commutation cells can be controlled. However, this kind of technique based on current direction information has some problems because it is difficult to reliably determine the output current direction in a switching power converter, especially at low current levels. To avoid this problem, in [4], a technique using the voltage across the bidirectional switch to determine the current direction has been developed. This method is more reliable than the current sensing method, but a relatively expensive complicated digital gate array, such as a complex programmable logic device (CPLD) or field programmable gate array (FPGA), has to be used to implement the control logic. Another alternative approach in [5] relies on the knowledge of the relative magnitudes of the input voltages instead of considering the direction of the output current.

Whether the current direction based commutation methods or the voltage level based techniques are used, all require peripheral sensing circuit. The extra circuit part may add complexity to the overall system and possible sensing error or sometimes sensing mistakes may cause damage to the system or devices.

2.2 R-C commutation circuit

Fig. 1(a) shows the circuit topology of a two-phase to single-phase matrix converter. The converter mainly consists of two bidirectional switches, S_A and S_B. v_{sa} and v_{sb} are the input voltage sources and i_o the output current. Actually, the bidirectional switches S_A and S_B can be made of any structure such as the common-collector or common-emitter arrangements, while, in this paper, the arrangement shown in Fig. 1(a) is used. Extra elements C_{sA}, C_{sB}, R_s are added for commutation purpose. The typical gating signals for bidirectional switches are shown in Fig. 1(b). It should be noted that a short dead time t_d is inserted.

Fig. 2 shows the three-phase to three-phase matrix converter with the R-C commutation circuit. As seen in Fig. 2, the converter contains nine bidirectional switches,

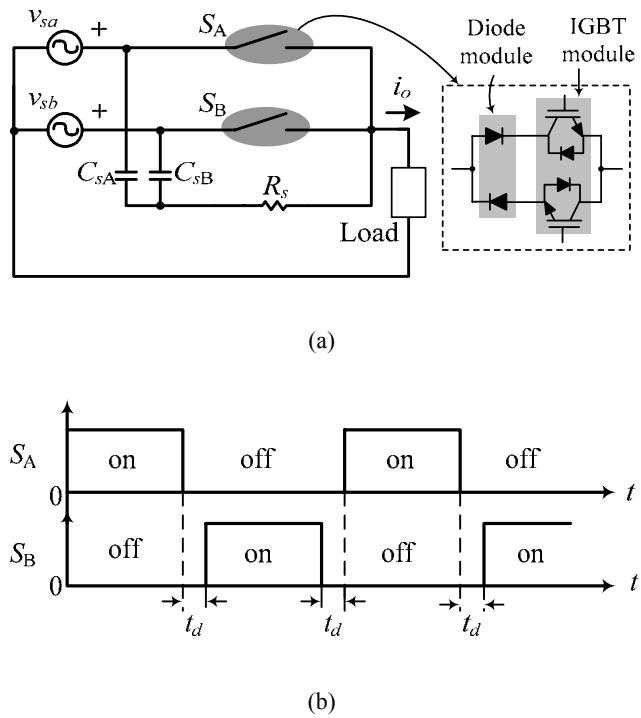

Fig. 1 Two-phase to single-phase matrix converter with the R-C commutation circuit (a) Circuit (b) PWM signals of the bidirectional switches

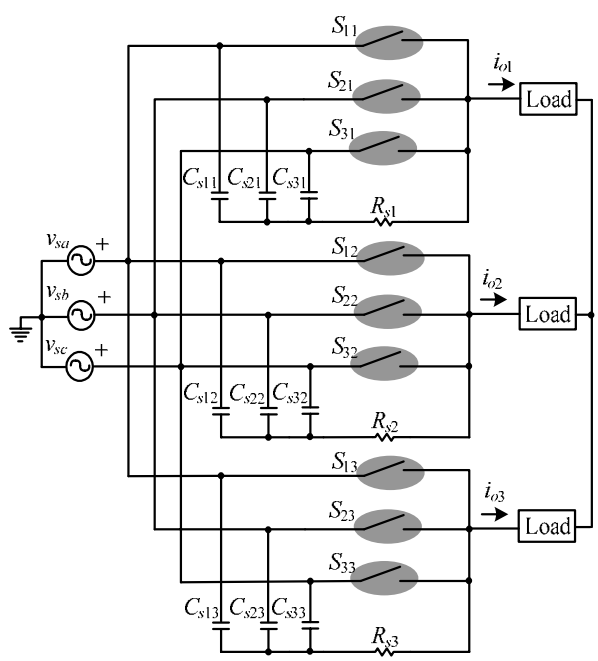

Fig. 2 Three-phase to three-phase matrix converter with the R-C commutation circuit

which are S_{11}, S_{12}, S_{13}, S_{21}, S_{22}, S_{23}, S_{31}, S_{32} and S_{33}. C_{s11}, C_{s21}, C_{s31}, C_{s12}, C_{s22}, C_{s32}, C_{s13}, C_{s23}, C_{s33}, R_{s1}, R_{s2} and R_{s3} are added as commutation circuits.

The same technique can be easily applied to the general n-phase to m-phase matrix converter. Fig. 3 shows the n-phase to m-phase matrix converter with the general R-C commutation circuit. It can be seen from Fig. 1 to Fig. 3 that the R-C commutation circuit topology can be considered as a general approach to solve the matrix converter commutation problem.

3. Operating Principle

In order to explain the operating principle of the commutation circuit, the operation of two-phase to single-phase matrix converter can be considered. Fig. 4(a) is the schematic of a two-phase to single-phase matrix converter with the R-C commutation circuit. Fig. 4(b) shows the gating signal for the IGBTs (S_1 S_2, S_3 and S_4). It should be noted that a short period of dead time t_d is inserted in the PWM signal. IGBT switches S_1 and S_2 share the same gating signal, as do S_3 and S_4. Hence, compared with conventional commutation technique, the gating logic for completing the commutation can be quite easy and simple.

According to the input voltage polarity and output current direction, there exist four possible commutation cases. The condition when the input voltage and output current are both positive is dealt with as an example. Operation under other conditions will be quite similar. It is assumed that the switching frequency f_s is much higher than the source frequency f_i and output frequency f_o. Also, for convenience, it is defined that C_{s1}=C_{s2}=C_s and R_{s1}=R_{s2}=R_s. The input voltage and output current are defined in (1) and (2) respectively.

$$v_s(t) = V_i \sin(\omega_i t) = V_i \sin(\theta) \tag{1}$$

$$i_o(t) = I_L \sin(\omega_o t + \varphi) = I_L \sin(\theta + \phi) \tag{2}$$

where $\phi = (\omega_o - \omega_i)t + \varphi$. The notations V_i and I_L will be the amplitude of input voltage and output current respectively.

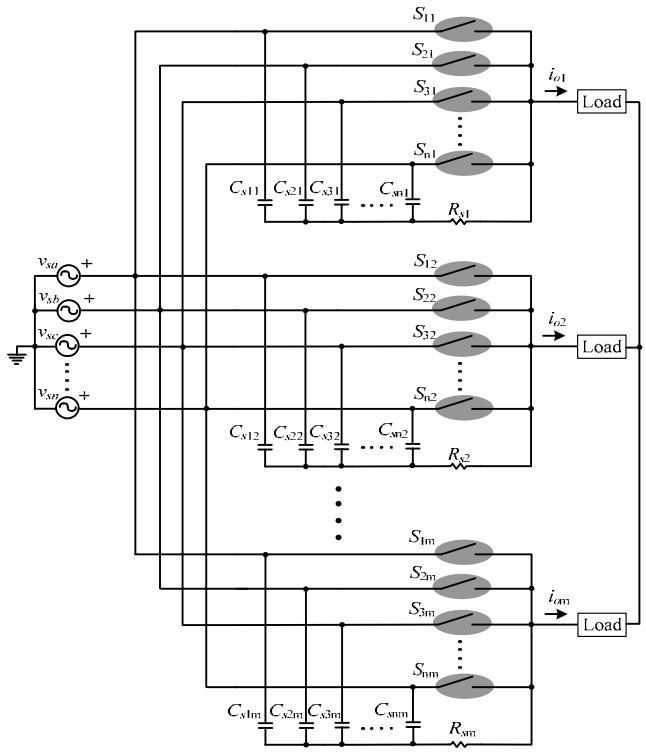

Fig. 3 n-phase to m-phase matrix converter with the R-C commutation circuit

3.1 Turing off S_3-S_4 and turning on S_1-S_2

Fig. 5 shows a set of typical operating waveforms. Fig. 6 shows the commutation modes, and the actual current path is denoted by a bold line in Fig. 6.

Mode-I: Mode-I is the initial circuit state. S_1 and S_2 are off, S_3 and S_4 are on. Output current I_o flows through D_3-S_3. Initially, v_1=V_s and v_2=0.

Mode-II: When dead time begins at t_1, all the four IGBTs are turned off together and mode-II begins. Since C_{s1}-R_s path and C_{s2}-R_s path imply the same impendence, I_o will flow through these two loops equally and the two commutation capacitor (C_{s1}, C_{s2}) will be charged by this current.

At the end of dead time, S_1 and D_2 will have the maximum voltage stress,

$$v_{\max} = V_s + \frac{1}{2} R_s \cdot I_o + \frac{I_o}{2C_s} \cdot t_d \tag{3}$$

From (3), it can be seen that a smaller dead time will be preferred to reduce the voltage stress across

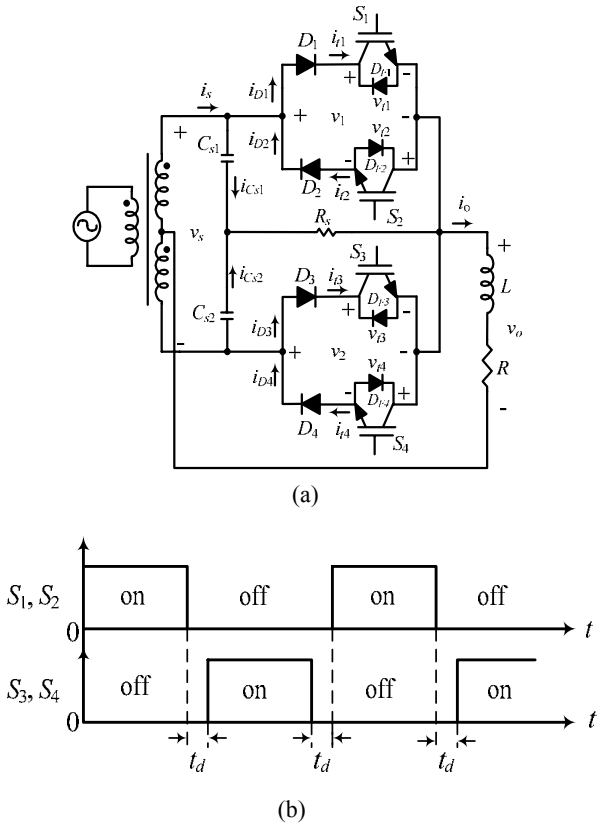

Fig. 4 Two-phase to single-phase matrix converter
(a) Schematic (b) IGBTs' gating signal

semiconductor devices. Actually, the choice of dead time will depend on the turn-off characteristics of IGBT. It is recommended that the dead time be set just enough to safely turn off the IGBT. In (3), it is worth noting that the notations V_s and I_o will be instant sampled values of (1) and (2) respectively. By substituting (1) and (2) into (3) and collecting terms, equation (4) can be obtained.

$$V_{\max} = V_i + \frac{I_L}{2} \cdot \left(R_s + \frac{t_d}{C_s} \right) \cdot \tag{4}$$

Equation (4) determines the voltage rating of semiconductor devices. It can be seen from (4) that $V_{\max}$ is proportional to R_s and inverse to C_s.

Mode-III: When S_1 and S_2 are simultaneously turned on at t_2, dead time ends and mode-III starts. I_o commutates to D_1-S_1 loop. v_1 jumps to zero and v_2 jumps to $-V_s$ immediately.

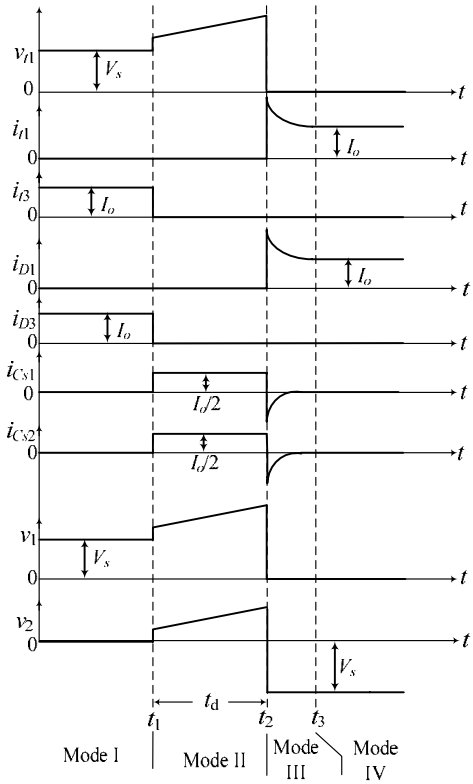

Fig. 5 Commutation waveforms (set I)

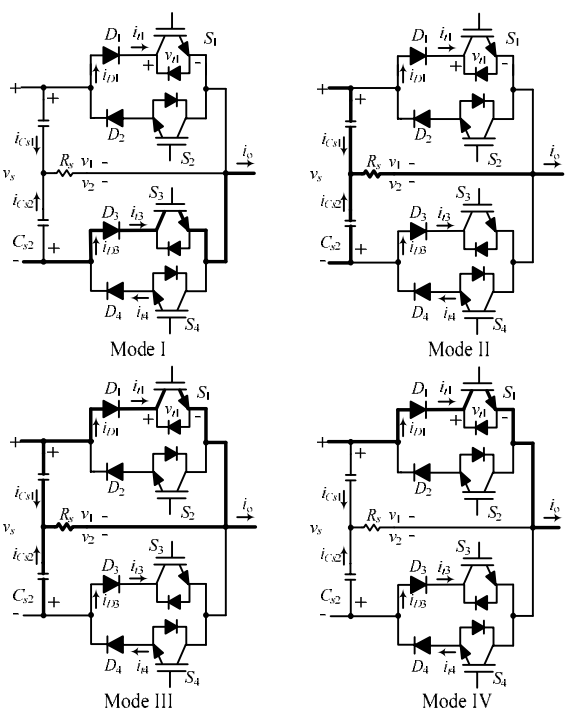

Fig. 6 Commutation modes (set I)

The previously charged C_{s1} will discharge through C_{s1}-D_1-S_1-R_s. C_{s2} will charge toward $-V_s$ by the source. In this mode, there exist three current components in the circuit; the load current, the C_{s1} discharging current and the C_{s2} charging current.

At the beginning of mode-III, i_{t1} and i_{D1} have the maximum value $i_{\max}$,

$$i_{\max} = \frac{1}{R_s}\left(2V_s + \frac{I_o t_d}{C_s}\right) + \frac{3}{2} I_o \cdot \tag{5}$$

Since V_s and I_o will be instant sampled values of (1) and (2) respectively, by substituting (1) and (2) into (5) and collecting terms, (6) can be obtained,

$$I_{\max} = \frac{2V_i}{R_s} + \left(\frac{3}{2} + \frac{t_d}{R_s C_s}\right) \cdot I_L \cdot \tag{6}$$

Equation (6) determines the current rating of semiconductor devices. As seen from (6), $I_{\max}$ is inversely proportional to both R_s and C_s.

By (4) and (6) and choosing proper passive component value, a specific IGBT and diode can be selected.

Mode-IV: After discharging C_{s1} and charging C_{s2}, all the commutation procedure ends at t_3. The output current flows through D_1-S_1. Finally, v_1=0 and v_2=-V_s.

The commutation power loss in resistor R_s can be approximately calculated by considering the summation of discharging energy of capacitor C_s.

$$\begin{aligned} E &= 2\times\frac{1}{2} C_s \sum_{j=1}^{k/4} v_{sj}^2 = 8\times\frac{1}{2} C_s \sum_{n=1}^{k/4}\left(4 f_i V_i \cdot \frac{j}{f_s}\right)^2 \\ &\approx \frac{1}{3} V_i^2 \cdot C_s \cdot k \end{aligned} \tag{7}$$

where $k = f_s / f_i$. Then, the resistor power will be

$$P = E \cdot f_i = \frac{1}{3} f_s \cdot V_i^2 \cdot C_s \cdot \tag{8}$$

In general, with n-phase input voltage source, (8) will be

$$P_n = \frac{n}{6} f_s \cdot V_i^2 \cdot C_s \cdot \tag{9}$$

3.2 Turing off S_1-S_2 and turning on S_3-S_4

Fig. 7 shows a set of typical operating waveforms when turning off S_1-S_2 and turning on S_3-S_4. Fig. 8 shows the commutation modes, and the practical current path is shown with a bold line in Fig. 8.

Mode-I: Mode-I is the initial circuit state. S_1 and S_2 are on, S_3 and S_4 are off. Output current I_o flows through D_1-S_1. Initially, v_1=0 and v_2=-V_s.

Mode-II: When dead time begins at t_1, all the four IGBTs are turned off together and mode-II begins. I_o will flow through C_{s1}-R_s loop and C_{s2}-R_s loop equally, C_{s1} and C_{s2} will be charged by this current.

Mode-III: When S_3 and S_4 are simultaneously turned on at t_2, dead time ends and mode-III begins. v_1 jumps to V_s and v_2 jumps to 0 immediately. C_{s1} will continue to be charged by the source to V_s. C_{s2} will be discharged toward 0. At t_2, since v_2 implies a negative value, D_3 will be reversely blocked. A current will flow through S_4-D_4.

Mode-IV: At t_3, D_4 is reversely blocked and D_3 conducts to a flow current.

Mode-V: After charging C_{s1} and discharging C_{s2}, all the commutation procedure ends at t_4. The output current flows through D_3-S_3. Finally, v_1=V_s and v_2=0.

4. Improvement of output linearity

4.1 Output voltage linearity

In matrix converter operation, some small linearity errors between the output voltages and their commands will exist due to semiconductor device voltage drop and commutation procedure. The semiconductor forward voltage drop effect is well-known and inherent to any power semiconductor devices. Considering the bidirectional switch arrangements shown in Fig. 1(a), regardless of the conducting current direction, there will be a diode and an IGBT carrying load current. The total voltage drop effect combines the voltage drops of the diode and the IGBT which are carrying the current.

Commutation sequence will also result in output distortion. The term of switching edge uncertainty is used to show such an effect [8]. If the time interval used to complete the commutation is relatively long, output distortion will be increased.

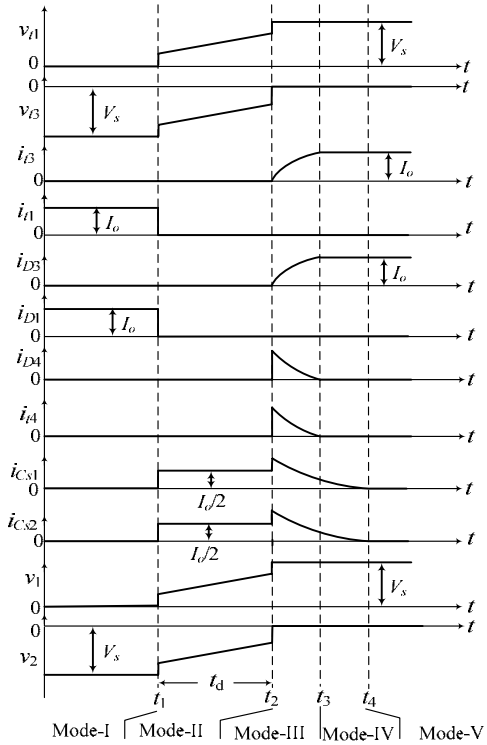

Fig. 7 Commutation waveforms (set II)

Especially when the PWM pulse is narrower than the time for completing a commutation sequence, this distortion phenomenon becomes more severe. Thus, several methods have been developed in order to improve the output linearity [6-8].

4.2 PWM duty ratio compensation

With a simple R-C commutation circuit added as commutation aid, dead time commutation technique can be applied to matrix converters. In this paper, the commutation timing sequence will be dealt with in order to illustrate how to improve switching edge uncertainty.

The two-phase to single-phase matrix converter in Fig. 1 is treated as an example. The commutation procedure with dead time commutation strategy is shown in Fig. 9 when the current commutates from v_{sa} to v_{sb}. Initially, S_A is on. Then S_A will be turned off and dead time begins at t_1.

During dead time t_d, the load current will flow through C_s-R_s loop. After dead time ends at t_2, S_B is turned on and the load current commutates to v_{sb}. It is noted that the

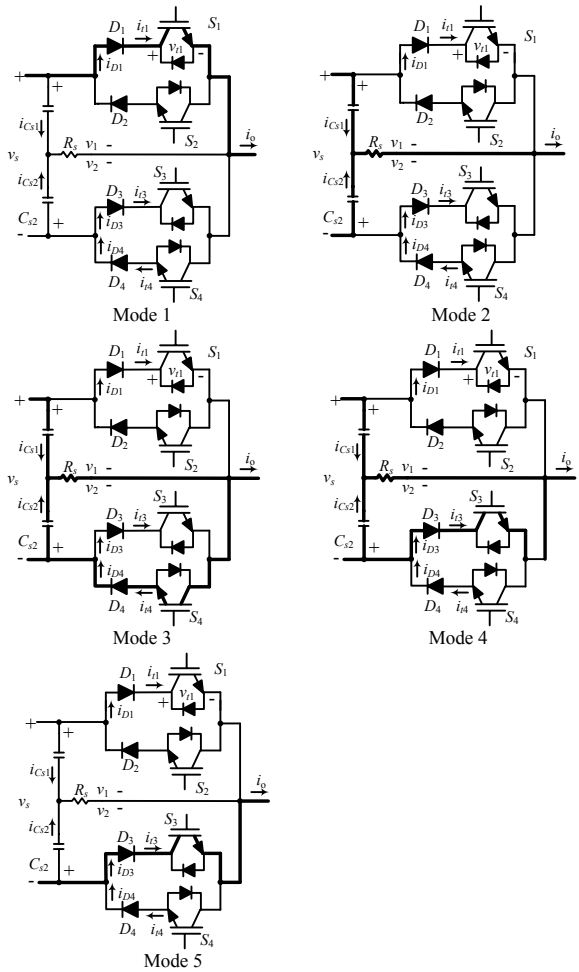

Fig. 8 Commutation modes (set II)

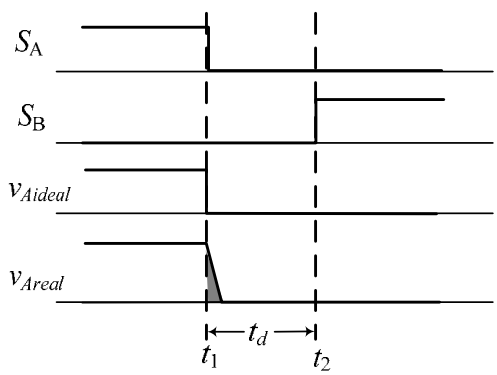

Fig. 9 Commutation procedure with dead time

switching edge uncertainty can be removed because the IGBTs in S_A and S_B are turned on or off at the same time.

As seen in Fig. 1(b), it is clear that with dead time

insertion, the width of the original control signal has been reduced by t_d when generating the gating signal. In the viewpoint of output voltage synthesis, this means that the effective time duration to form the output voltage has been reduced. Thus, output distortion occurs. Especially when the PWM pulse is narrower than the dead time t_d, the pulse will be cancelled, leading to incomplete commutation.

The PWM duty ratio compensation is made regarding to the popularly used space vector modulation method [10]. One switching period can be divided into five sub-intervals, shown in Fig. 10. The time duration for each sub-interval is determined by the following equations.

$$\begin{aligned} T_1 &= d_1 \cdot T_s = m_c \cdot \sin\left(60^\circ - \theta_{sv}\right) \cdot \sin\left(60^\circ - \theta_{sc}\right) \\ T_2 &= d_2 \cdot T_s = m_c \cdot \sin\left(\theta_{sv}\right) \cdot \sin\left(60^\circ - \theta_{sc}\right) \\ T_3 &= d_3 \cdot T_s = m_c \cdot \sin\left(\theta_{sv}\right) \cdot \sin\left(\theta_{sc}\right) \\ T_4 &= d_4 \cdot T_s = m_c \cdot \sin\left(60^\circ - \theta_{sv}\right) \cdot \sin\left(\theta_{sc}\right) \\ T_0 &= T_s - T_1 - T_2 - T_3 - T_4 \end{aligned} \tag{10}$$

where d_1, d_2 d_3 and d_4 stand for the duty ratio for producing T_1, T_2, T_3 and T_4, respectively. m_c is the voltage conversion ratio defined as output voltage magnitude over input voltage magnitude. θ_{sc} and θ_{sv} are the phase information of the input current space vector and output voltage space vector respectively.

After dead time is inserted, the actual time duration of T_1, T_2, T_3 and T_4 will be modified by dead time t_d.

$$\begin{aligned} T_1^{'} &= T_1 - t_d \\ T_2^{'} &= T_2 - t_d \\ T_3^{'} &= T_3 - t_d \\ T_4^{'} &= T_4 - t_d \end{aligned} \tag{11}$$

Hence, a simple method to cancel the distortion effect caused by t_d will be used to compensate for the original switching intervals with t_d. Then the distortion caused by dead time insertion will be removed. Thus, equation (10) will be modified to (12).

The proposed compensation method also implies very good feasibility. It can be easily applied to other PWM modulation methods for matrix converters.

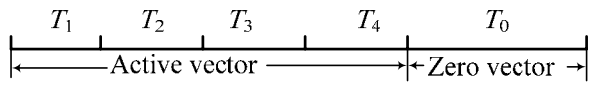

Fig. 10 PWM switching pattern

$$\begin{aligned} T_{1m} &= m_c \cdot \sin\left(60^\circ - \theta_{sv}\right) \cdot \sin\left(60^\circ - \theta_{sc}\right) + t_d \\ T_{2m} &= m_c \cdot \sin\left(\theta_{sv}\right) \cdot \sin\left(60^\circ - \theta_{sc}\right) + t_d \\ T_{3m} &= m_c \cdot \sin\left(\theta_{sv}\right) \cdot \sin\left(\theta_{sc}\right) + t_d \\ T_{4m} &= m_c \cdot \sin\left(60^\circ - \theta_{sv}\right) \cdot \sin\left(\theta_{sc}\right) + t_d \\ T_{0m} &= T_s - T_{1m} - T_{2m} - T_{3m} - T_{4m} \end{aligned} \tag{12}$$

5. Experiment Results

5.1 Operation of R-C commutation circuit

An experimental setup was made to verify the operation of the R-C commutation circuit. The converter circuit is the same as shown in Fig. 4(a) with the circuit parameters as follows:

V_i=100 V, L=5 mH, R=2.5 Ω, f_s=5 kHz,
R_s =10 Ω, C_s=0.22 μF, t_d=1 μs.

where L is the load inductance and R the load resistance.

Fig. 11 shows the overall converter operation when f_i=f_o=60 Hz. The upper two waveforms are the input and output voltage waveforms, while the lower two are the input and output currents. As seen in Fig. 11, the converter operates well. The output current curve is continuous and smooth.

Fig. 12 is the experimental voltage and current waveforms of commutation aid components when the load current commutates from the lower switches to the upper switches. Fig. 13 is the experimental voltage and current waveforms of the commutation aid component when the load current commutates from the upper switches to the lower switches.

It can be seen from Fig. 12 and Fig. 13 that the experiments results are almost identical to the analysis. In Fig. 12 and Fig. 13, it can be seen that i_{cs1} and i_{cs2} contains some resonant waves. The lower frequency part is due to the stray inductance of the switch power circuit. The higher frequency part is due to the diode forward recovery phenomena and line insertion of DC current probes.

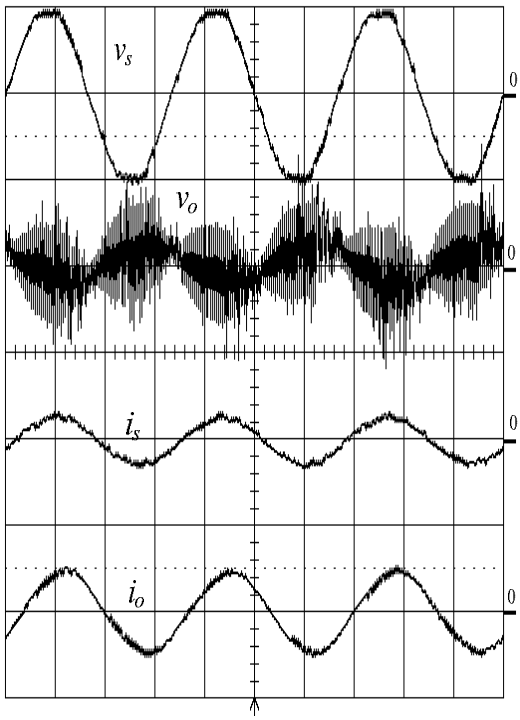

Fig. 11 Overall operation (v_s: 100 V/div, 5 ms/div; v_o: 100 V/div, 5 ms/div; i_s: 10 A/div, 5 ms/div; i_o: 10 A/div, 5 ms/div)

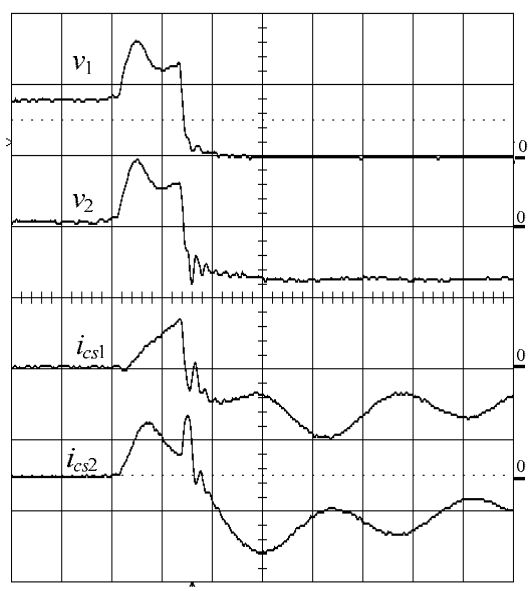

Fig. 12 Voltage and current waveforms when current commutates from the lower switches to upper switches (v_1: 50 V/div, 0.5 μs/div; v_2: 50 V/div, 0.5 μs/div; i_{cs1}: 5 A/div, 0.5 μs/div; i_{cs2}: 5 A/div, 0.5 μs/div)

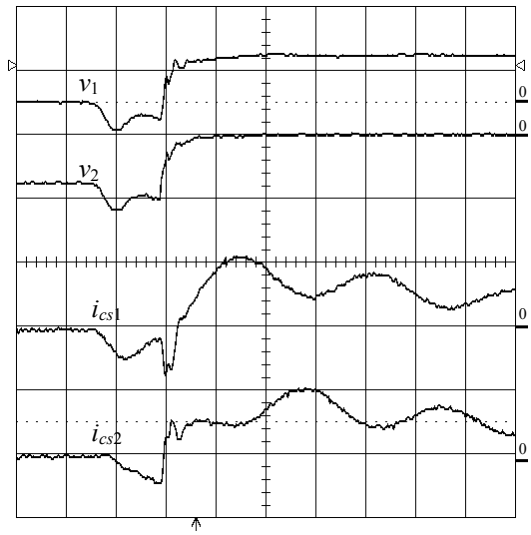

Fig. 13 Voltage and current waveforms when current commutates from the upper switches to lower switches (v_1: 50 V/div, 0.5 μs/div; v_2: 50 V/div, 0.5 μs/div; i_{cs1}: 5 A/div, 0.5 μs/div; i_{cs2}: 5 A/div, 0.5 μs/div)

Finally, it can be concluded from the experiment results that the proposed circuit is quite feasible and very practical. It solves the matrix converter current commutation problem in a simple and reliable way.

5.2 Dead time compensation

A three-phase to three-phase matrix converter experimental setup was made to verify the operation of the proposed compensation method. The converter circuit parameters are as follows:

V_i=100 V, L=12 mH, R=2.5 Ω, f_s=5 kHz,
R_s =10 Ω, C_s=0.22 μF, t_d=1 μs.

Fig. 14 and Fig. 15 show the converter input and output waveforms when m_c=0.3 and output frequency f_o=3 Hz without any compensation and with the proposed compensation, respectively.

It can be seen in Fig. 14 that the output distortion is much more serious since both m_c and f_o are low. With the proposed dead time compensation method, the performances become much better compared to the waveforms in Fig. 14, as shown in Fig. 15. It can be concluded that the proposed compensation method can improve the output linearity in quite a simple and effective way.

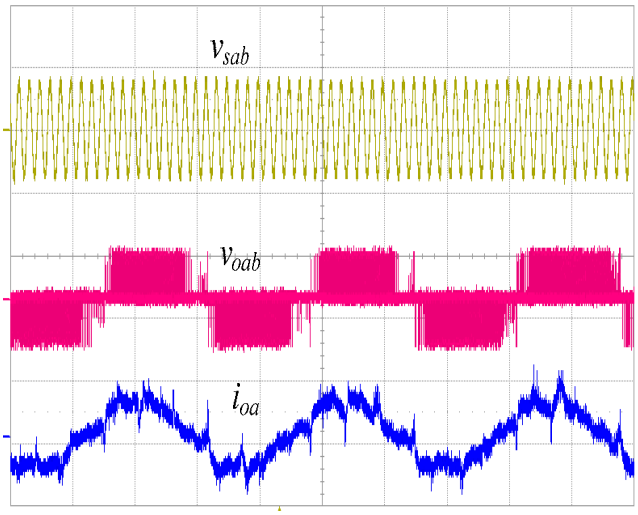

Fig. 14 Waveforms when m_c=0.3, f_o=3 Hz without compensation (v_{sab}: 200 V/div, 100 ms/div; v_{oab}: 200 V/div, 100 ms/div; i_{oa}: 5 A/div, 100 ms/div)

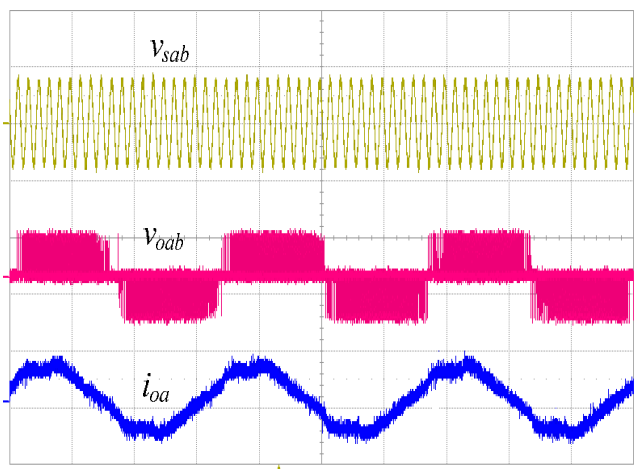

Fig. 15 Waveforms when m_c =0.3, f_o=3 Hz with compensation (v_{sab}: 200 V/div, 100 ms/div; v_{oab}: 200 V/div, 100 ms/div; i_{oa}: 5 A/div, 100 ms/div)

6. Conclusions

In this paper, a matrix converter with improved output linearity was proposed while employing a general R-C commutation circuit. The R-C commutation circuit enables safe commutation without extra sensed circuit information. Thus, the operation is very stable, reliable and robust. Operating principles and modes analysis are given. Meanwhile, with dead time commutation strategy applied, the distortion caused by commutation delay and incomplete commutation is properly compensated, leading to better output linear behavior. Finally, the feasibility and validity of the proposed schemes are verified through experimentation.

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