JPE 9-2-14

ICPE'07 Selected Paper

A Gate Drive Circuit for Low Switching Losses and Snubber Energy Recovery

Toshihisa Shimizu† and Keiji Wada*

†*Dept. of Electrician and Electronics Engineering, Tokyo Metropolitan University, Tokyo, Japan

ABSTRACT

In order to increase the power density of power converters, reduction of the switching losses at high-frequency switching conditions is one of the most important issues. This paper presents a new gate drive circuit that enables the reduction of switching losses in both the Power MOSFET and the IGBT. A distinctive feature of this method is that both the turn-on loss and the turn-off loss are decreased simultaneously without using a conventional ZVS circuit, such as the quasi-resonant adjunctive circuit. Experimental results of the switching loss of both the Power MOSFET and the IGBT are shown. In addition, an energy recovery circuit suitable for use in IGBTs that can be realized by modifying the proposed gate drive circuit is also proposed. The effectiveness of both the proposed circuits was confirmed experimentally by the buck-chopper circuit.

Keywords: Gate drive circuit, Switching loss, High-frequency switching

1. Introduction

Increasing the power density of power converters has become one of the most important issues in the power electronics field. One effective way of realizing high-power density is to increase the switching frequency, because both the volume and weight of the magnetic component can be reduced. However, there is a tradeoff between the switching frequency and the switching loss. This results in increased switching loss and hence the volume of the heat-sink of the power semiconductors cannot be reduced. This paper presents a new gate drive circuit that enables the reduction of switching loss in both the Power MOSFET and the IGBT. A distinctive feature of the gate drive circuit is that both the accelerated turn-on action and ZVS turn-off action can be realized simultaneously by adding only a small number of adjunct components to the conventional gate drive circuit. In the first section, a mechanism for increasing the turn-on loss caused by the mirror effect on the Power MOSFET is described and the circuit configuration of the proposed gate driver is also described. In the next section, the circuit configuration and the operation principle of the proposed gate drive circuit are presented. This is followed by theoretical discussion, some experimental results of both the switching devices shown, and discussion on the effectiveness of this method. In addition, a modification of the proposed gate drive circuit suitable for use in IGBTs is

Manuscript received Jan. 31, 2009; revised Feb. 23, 2009
†Corresponding Author: shimizut@tmu.ac.jp
Tel:+81-426-77-2743, Fax:+81-426-77-2756, Tokyo Metropolitan Univ.
*Dept. of Electrician and Electronics Engineering, Tokyo Metropolitan University, Tokyo, Japan

shown. This modification is focused mainly on the reduction of the turn-off loss of the IGBT. Experimental results show the effectiveness of the proposed method.

2. Operation Principle and Circuit Configuration

Figure 1 shows a conventional gate drive circuit for MOSFET or IGBT devices, and Table.1 shows the circuit parameters of the proposed circuit. It is well known that an inductance component, L_G, and a resistance component, R_G, contained in the gate/source wiring harms high speed charging/discharging of the gate voltage and that results in increased switching loss. Especially at the turn-on transition, the gate charge energy supplied from the gate drive circuit leaks from the gate terminal to the drain terminal through the mirror capacitor, C_{GD}, as shown in Fig.2. This means that the supplied energy is by-passed through the mirror capacitor. What is worse, the amount of leak charge increases because the mirror capacitor increases dramatically at low drain-source voltage condition. Hence, the gate-source voltage, V_{GS}, stays around the threshold voltage, and the on-state voltage, $V_{DS(on)}$, at the turn-on transition does not decrease quickly as shown in Fig.3. As a result, the resultant turn in loss increases dramatically. This phenomenon is called the mirror effect.

If we can compensate the gate charge of the input capacitor, C_{GS}, by some proper method, we can decrease the turn-on loss much more. What we focused on is the fact that the change of drain-gate voltage, V_{DG}, occurs at the same instance as the change of voltage of the drain-source voltage, V_{DS}. This means that the gate charge leak occurs during the fall time of drain-source voltage, V_{DS}. It is clear that we cannot collect the charge that is flowing through the mirror capacitor. But we can simulate the leak current if we detect the discharge current on the additional capacitor that is connected between the drain and the source terminal. And we can charge the input capacitor, C_{GS}, more quickly by transferring the detected current to the capacitor through a current transformer.

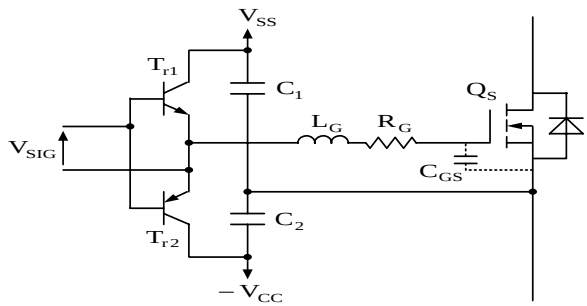


Fig. 1 Basic gate drive circuit

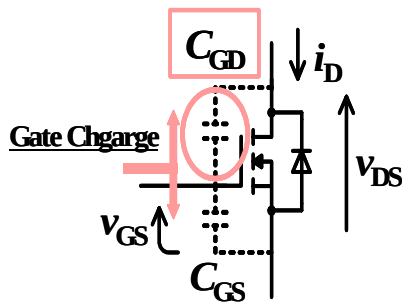


Fig. 2 Parasitic capacitor and the mirror effect

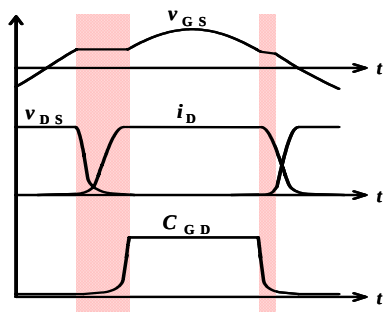


Fig. 3 Operation waveforms on the switching transition

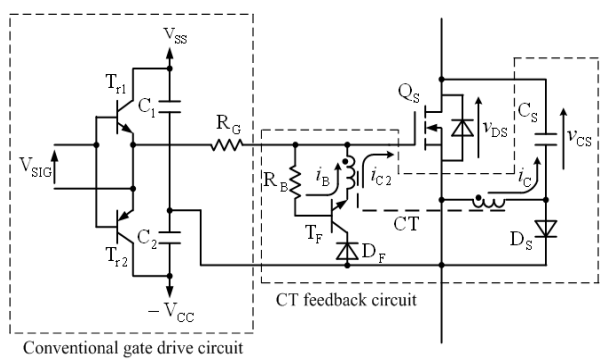


Fig. 4 Proposed gate drive circuit

Based on the above principle, we propose a new gate drive circuit as shown in Fig, 4. This circuit is composed of a CT current feedback circuit and a conventional gate drive circuit.

Detailed operation of the gate drive circuit is explained as follows.

During the turn-on transition of the main power device, Q_S, the discharge current, i_{CS}, of the capacitor, C_S, flows through the primary side of the current transformer (CT), and the current energy is transferred to the secondary winding of the CT. A small part of the secondary current of the CT, i_B, flows through the base terminal of the transistor, T_F, and makes the transistor turn-on. Then most of the secondary current, i_{C2}, flows through the gate-source terminal, and charges the input capacitor, C_{GS}, quickly. As a result, the turn-on time of the main power device is shortened and the resultant turn-on loss can be decreased. Since the transistor, T_F, is turned off automatically after the turn-on transition, the secondary winding of the CT is disconnected from the gate-source terminal. Then the CT is prevented from magnetic saturation, and we can induce the required voltage into the gate-source terminal. Another advantage of this circuit is that the capacitor, C_S, and the diode, D_S, operate as the ZVS turn-off snubber. Hence, the rise time of V_{DS} at turn-off transition of the main power device can be decreased, and the resultant turn-off loss can also be decreased simultaneously.

3. Experimental Results

Figure 5 shows the circuit configuration of the buck-chopper circuit in which the proposed gate drive circuit is used, and Table 1 shows the circuit parameters of the experimental setup. Figures 6(a) and (b) show the switching waveforms on the Power MOSFET at turn-on and turn-off transients, respectively. As shown in Fig. 6(a), the on state voltage, V_{DS}, at the turn-on transient takes on a high value on the conventional gate drive condition. On the contrary, the voltage is remarkably reduced in the proposed gate drive condition. It should also be noted that the increase rate of the drain current at the turn-on transient is much higher than the conventional one because the reverse recovery current flowing through the anti-parallel diode, D_{FW}, increases. This fact means that the reduction effect of the turn-on loss on the MOSFET may be harmed. However, it will be possible to reduce the loss much more by using a fast recovery diode as D_{FW}. At the turn-off transition, as shown in Fig. 6(b), the rate of increase of the drain voltage on the proposed gate drive condition is reduced compared to the one on the conventional condition.

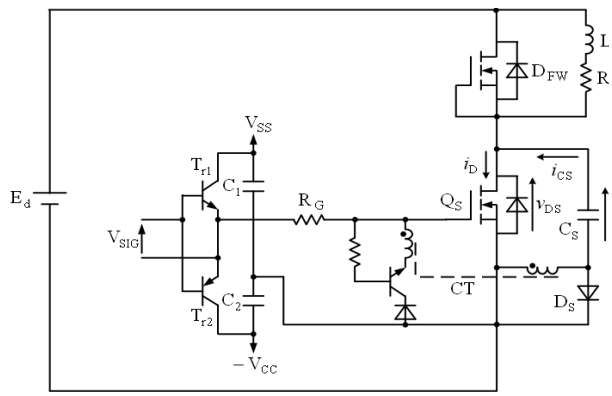
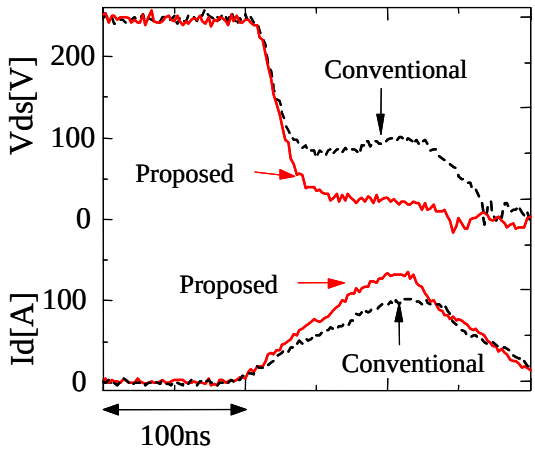


Fig. 5 Buck-chopper circuit for the switching loss measurement

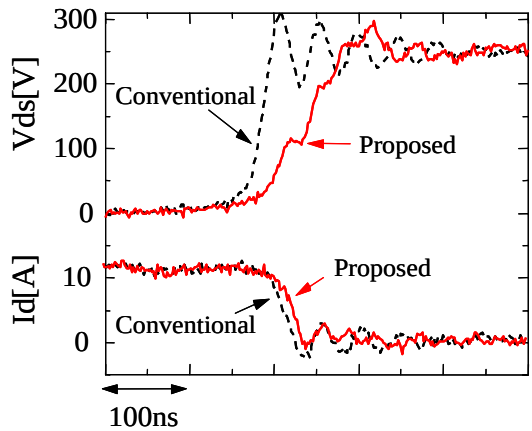
Table 1 Circuit parameters

Specifications	Value
MOSFET, Q_S	500V / 50A(2SK3132, Toshiba)
IGBT, Q_S	600V / 40A(IRGP20B60PD, IR)
Current trans, CT	Material: Ni-Zn Ferrite Dimension:ϕ =15mm,t=5mm Winding: 4turn/4turn
Transistor, T_{r1}, T_F	60V / 0.3A (2SC3596, Sanyo)
Transistor, T_{r2}	60V / 0.3A (2SA1402, Sanyo)
Gate resistor, R_G	10Ω / 1W
Snubber diode, Ds	600V / 6.0A (SDP06S60,Infenion)
Snubber capacitor, Ds	2350pF / 630V

It is clear that the turn-off loss of the MOSFET in the proposed system is reduced. Hence, the overall switching loss in the MOSFET is reduced by the proposed gate drive circuit.

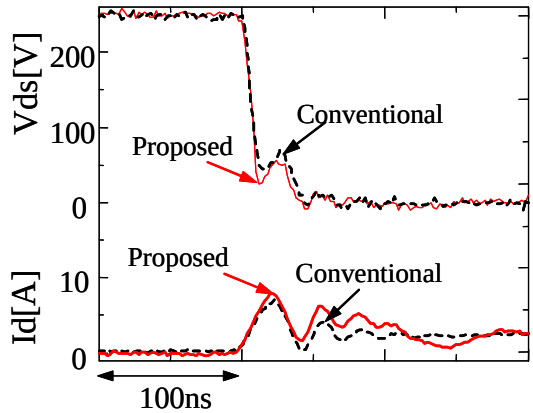


(a) turn-on waveforms

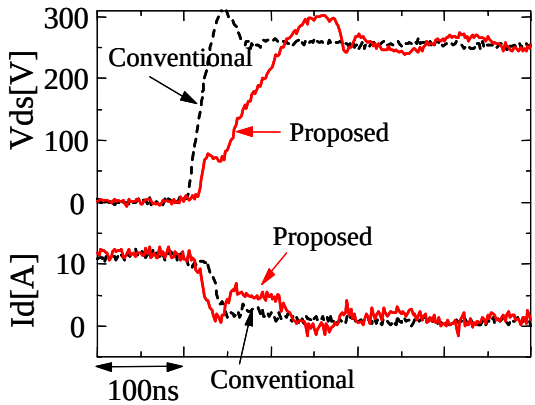


(b) turn-off waveforms

Fig. 6 Switching waveforms on the Power MOSFET



(a) turn-on waveforms

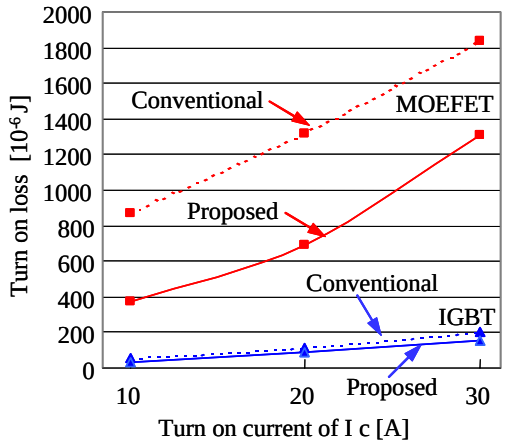


(b) turn-off waveforms

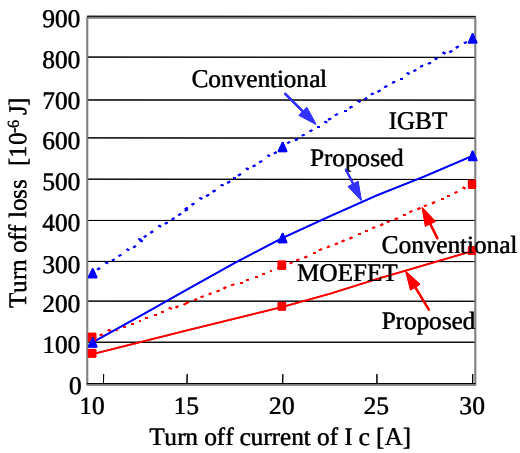
Fig. 7 Switching waveforms on the IGBT

Figures 7(a) and (b) show the switching waveforms of the IGBT at turn-on and turn-off transients, respectively. Fig. 7(a) shows the drain voltage at the turn-on transient on both the conventional and the proposed gate drive conditions. We can observe that those two waveforms coincide well, and this result is completely different from that of the MOSFET. This is because the turn-on action of the IGBT is mainly influenced by the carrier injection phenomenon in the IGBT structure and is not influenced by the mirror effect. As a result, the turn-on loss in the IGBT cannot be decreased by the proposed gate drive circuit. Figure 7(b) shows turn-off voltages in cases when the conventional gate drive circuit and the proposed gate drive circuit are used. We can see that the rate of increase of the drain voltage in the proposed gate drive condition is reduced. In the proposed gate drive condition, amplitude of the drain current during turn-off transition increases slightly. This current rise is caused by the minor carrier ejection in the IGBT junction which depends on the IGBT structure. Even though the current rise in the drain current appears, the overall turn-off loss in the IGBT is reduced compared to the one in the conventional condition.

Figure 8(a) and (b) show the measured results of turn-on and turn-off loss of the Power MOSFET and the IGBT in some current conditions. As shown in Fig. 8(a), the turn-on loss of the Power MOSFET is constantly



(a) turn-on loss



(b) turn-off loss

Fig. 8 Switching loss characteristics

decreased of about 500[uJ] compared to the loss in the conventional gate drive condition. On the contrary, the value of the turn-on loss of the IGBT cannot be decreased even when the proposed gate drive circuit is used. But the turn-on loss of the IGBT is much smaller than that of the Power MOSFET. The turn-off loss of both the Power MOSFET and the IGBT are shown in Fig. 8(b). The turn-off loss is also decreased compared to the loss in the conventional gate drive circuit. Surprisingly the reduced turn-off loss of the IGBT is much higher than that of the Power MOSFET. Differing from the results of the turn-on loss, the decrease of turn-off loss of the IGBT is almost in proportion to the turn-off current, and about 30-50% of the switching loss can be decreased.

We can summarize the experimental results as follows.

(i) On the MOSFET, both the turn-on and turn-off losses are reduced by the proposed gate drive circuit.

(ii) On the IGBT, only the turn-off loss is reduced but the turn-off loss is not reduced.

(iii) (iii) The turn off loss might have been decreased much more if we used larger capacitance as Cs. But in this case, the energy transferred from the capacitor, C_S, increases too much and causes the over-charging of the gate voltage, V_{GS}. Then, in this case, we need to transfer the surplus energy to some appropriate power consumption.

4. Snubber Energy Recovery

Previous experimental results show that the proposed gate drive circuit is useful for reducing the turn-off loss of the IGBT even though it cannot reduce the turn-on loss. In order to exploit this merit, the proposed gate drive circuit is modified to a capacitor energy recovery circuit as shown in Fig. 9. The purpose of the energy recovery circuit is to regenerate the energy being stored on the ZVS capacitor to the gate drive dc power supply. The basic concept of the energy recovery of the ZVS capacitor has been proposed by S. Finney[3]. In this paper, the recovered power is transferred to the main dc power supply. However, in this case, volume of the CT used in the practical system increases because it needs tough galvanic isolation between the primary and the secondary windings.

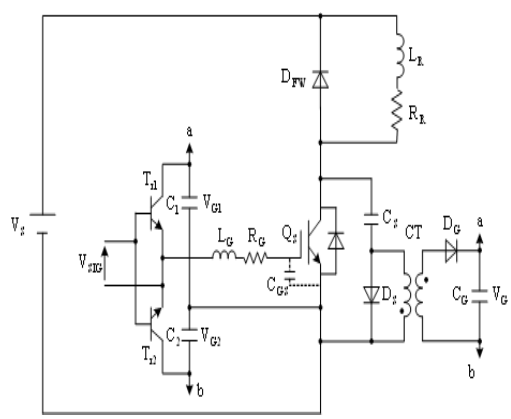
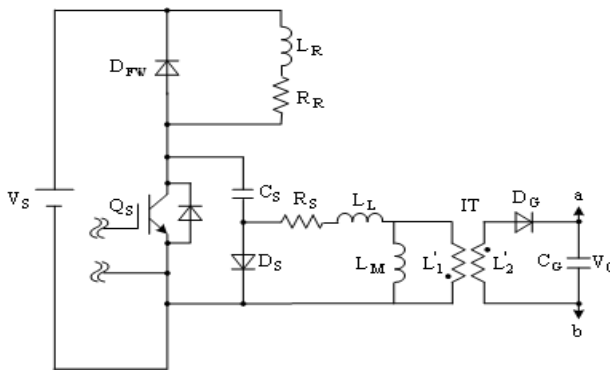
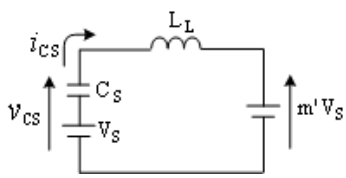


Fig. 9 Proposed capacitor energy recovery circuit

In order to solve this problem, the authors modified the secondary voltage source by changing the main dc source to the corresponding gate drive dc power source. In addition, previous work did not show the energy recovery



(a) Circuit configuration



(b) Equivalent circuit

Fig. 10 The proposed capacitor energy recovery circuit

ratio experimentally. Therefore we confirmed the practical energy recovery ratio thorough the experiments.

The quivalent circuit of the proposed energy recovery circuit is shown in Figs. 10(a) and (b). In Fig. 10(a), the current transformer is expressed by the magnetizing inductor, L_M, the leakage inductor, L_L, and the ideal transformer, IT. The voltage ratio of the ideal transformer is denoted by $m = \sqrt{L_1'/L_2'}$. The simplified equivalent circuit is shown as Fig. 10(b). The secondary voltage, V_G, which is assumed as the gate drive power supply voltage, is converted to the primary the side voltage, mV_G. When we define the voltage ratio, m', as

$$m' = \frac{mV_G}{V_S}, \ (0 < m' < 1). \tag{1}$$

where, V_S is the main dc voltage.

We can derive a differential equation as follows.

$$\frac{d^2 v_{CS}}{dt^2} + \frac{v_{CS}}{L_r C_S} = m' V_S . \tag{2}$$

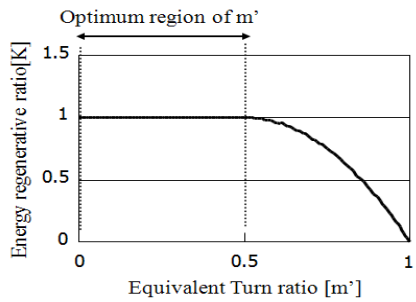


Fig. 11 Calculated results of the energy recovery ratio

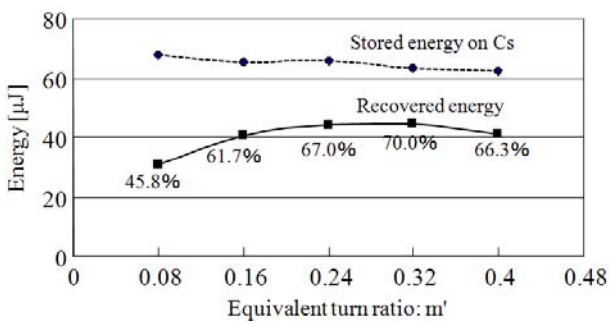


Fig. 12 Experimental results of the energy recovery ratio

The initial conditions of the voltage and the current of the capacitor, Cs, are given by $v_{CS}(t) = V_S$, and $i_{CS}(t) = 0$, respectively. For simplicity, we assume that the resistor component, R_S, is negligible and the magnetizing inductance, L_M, of the transformer is very large. The current, $i_{CS}(t)$, which flows into the voltage $m'V_S = mV_G$ yields,

$$i_{CS}(t) = \frac{V_S}{\sqrt{L_r / C_S}}(1 - m')\sin\frac{1}{\sqrt{L_r C_S}}t \ . \tag{3}$$

The energy regenerative ratio, K, is given from the

following equations.

In the case of $0 < m' < 0.5$,

$$K = 1 \tag{4}$$

In the case of $0.5 < m' < 1$,

$$K = \frac{\int_0^T (m' V_S i_{CS}(t))dt}{0.5 C_S V_S^2} = 4m'(1-m') \tag{5}$$

The calculated recovery ratio, K, is shown by Fig. 11. The results show that the voltage ratio, m', should be smaller than 0.5 in order to achieve high energy recovery. By taking the above results into consideration we measured the energy recovery ratio on the experimental setup. Figure 12 shows the measured results of the recovered energy, the stored energy on Cs, and the resultant energy recovery ratio. The highest energy recovery ratio is 70% which is given at m'=0.32. The ratio decreases, so that the value of m' keeps away from 0.32.

Figure 13 shows the measured loss distribution results of the energy recovery circuit. In the case of lower m' condition, peak current of i_{CS} increases as shown in eq.(3). Hence, turn-on loss of the IGBT increases because high peak current flows thorough the IGBT at its turn on duration. On the contrary, in the case of high m' condition, peak current of i_{CS} decreases and turn-on loss of the IGBT decreases. However, both the magnetizing current and the resultant magnetizing loss increases because the voltage, mV_g, which is induced to the magnetizing inductor, increases. Fortunately, the maximum energy recovery ratio given in the proposed circuit is almost same with that given in the referenced paper[3]. This means that the proposed method is also useful for efficient energy recovery.

5. Conclusions

A novel gate drive circuit for MOSFETs and IBGTs used for decreasing switching loss at high frequency operation is proposed. The experimental results in the buck-chopper circuit are shown and discussed for its effectiveness. On the MOSFETs, the proposed method is useful for reducing both the turn-on and the turn-off loss. On the contrary, on the IGBTs, the proposed method is useful only for reducing turn-off loss. The proposed circuit was modified in order to regenerate the capacitor energy while keeping the function of turn-off loss reduction. The energy recovery ratio on the modified circuit reaches 70%.

We can conclude that both the proposed gate drive circuit and the modified energy recovery circuit are effective methods for the reduction of switching loss on both the Power MOSFET and the IGBT.

References

[1] K.Takao, et.al, "Novel exact power loss design method for high output power density converter", Conference Record of IEEE PESC'06, pp.2651-2655, 2006.

[2] T.Shimizu, H.Kinjyo, K.Wada, "A Novel High-frequency Current Output Inverter based on an Immittance Conversion Element and a Hybrid MOSFET-SiC Diode Switch", Conference Record of IEEE PESC'03, pp.2003-2008, 2003.

[3] S.Finney, B.Williams, T.Green, "RCD Snubber Revised", *IEEE Trans. on Industry Applications*, Vol.32. No.1, pp.155-160, 1996.

[4] R.Chokhawala, J.Catt, B.Pelly, "Gate Drive Circuit for IGBT Module", *IEEE Trans. on Power Electronics*, Vol.31, No.3, pp.603-611, 1995.

[5] T.Shimizu, K.Wada, "A gate drive circuit of Power MOSFET and IGBT for low switching losses", The 7th International Conference on Power Electronics-ICPE'07, pp.857-860, 2007.

[6] Jun-Young Lee, "Dual Path Magnetic-Coupled AC-PDP Sustain Driver with Low Switching Loss", *Journal of Power Electronics*, Vol. 6, No. 3, pp.205-213, 2006.

[7] Amir Ostadi/Xing Gao/Gerry Moschopoulos, "Circuit Properties of Zero-Voltage-Transition PWM Converters", *Journal of Power Electronics*, Vol. 8, No. 1, pp.35-50, 2008.

Toshihisa Shimizu (M'93-SM'02) received his B.E., M.E. and Dr.Eng. in Electrical Engineering from Tokyo Metropolitan University in 1978, 1980, and 1991, respectively. In 1998, he was a visiting professor at VPEC, Virginia Polytechnic Institute and State University, Virginia. He joined Fuji Electric Corporate Research and Development, Ltd. in 1980. Since 1994, he has been with the Department of Electrical Engineering, Tokyo Metropolitan

University, Tokyo, Japan. Now he is a full professor in the same university. His research interests include power converters, high frequency inverters, photovoltaic power generations, high power density converter design, UPSs and EMI problems. Dr. Shimizu received a Transactions Paper Award from the Institute of Electrical Engineers of Japan in 1999. He is a senior member of IEEE, and a member of the Institute of Electrical Engineers of Japan (IEEJ), the Japan Society of Power Electronics.

Keiji Wada received his B.S. and M.S. degrees from Polytechnic University, Kanagawa, Japan, and his Ph. D. degree from Okayama University, Okayama, Japan in 1995, 1997, and 2000, respectively, all in Electrical Engineering. From 2000 to 2006, he was a Research Associate in Tokyo Metropolitan University and Tokyo Institute of Technology. Since 2006, he has been an Associate Professor with Tokyo Metropolitan University, Tokyo.