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Optimal Design Considerations of a Bus Converter for On-Board Distributed Power Systems

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ABSTRACT

The power supply systems, which require low-voltage / high-current output has been changing from the conventional centralized power system to a distributed power system. The distributed power system consists of a bus converter and POL. The most important factor is the system stability in bus architecture design. The overlap between the output impedance of a bus converter input impedance of POL causes system instability and has been an actual problem. By increasing the bus capacitor, the system stability can be easily improved. However, due to limited space on the system board, the increasing of bus capacitors is impractical. An urgent solution of this issue is strongly desired. This paper presents the output impedance design for on-board distributed power system by means of three control schemes of a bus converter. The output impedance peak of the bus converter and the input impedance of the POL are analyzed and then conformed experimentally for stability criterion. Furthermore, the design process of each control schemes for system stability is proposed.

Keywords: Distributed power system, Stability, Input impedance, Output impedance

1. Introduction

Various LSI is used in the telecommunication application equipments and the driving voltage also greatly varies. On the other hand, an increase of the load current is also remarkable by an advanced LSI function. Since the present LSI is designed in accordance with semiconductor manufacture technology, the tolerance level of the operating voltage is very narrow. Consequently, the voltage drop by the wiring impedance of power lines causes a malfunction of the LSI. In order to reduce the malfunction of the LSI by the voltage drop, it is proposed that the converter is arranged very close to the LSI. This converter is called POL. Thus, the power supply system which requires the low-voltage/high-current output has been changing from the conventional centralized power system to a distributed power system. The distributed power system consists of first-stage isolated DC-DC converter as a bus converter and second-stage non-isolated DC-DC converter as a POL.

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However, recently, the instability phenomenon in a distributed power system is posing a problem. This is an instability phenomenon resulting from the overlapping between the output impedance of a bus converter and the input impedance of a POL. By increasing the bus capacitor, the system stability can be easily improved.

However, due to limited space on the system board, the increasing of bus capacitors is impractical. An urgent solution of the issue is strongly desired, and various discussions of system stability has been reported[1-9]. Then, we have also reported the detailed discussion of system stability by control schemes of a bus converter (Un-regulated, Semi-regulated and Full-regulated)[10-15]. However, so far, the detailed discussion of the practical design of a bus converter about an on-board distributed power system has not been reported. This paper presents the optimal design of a bus converter for an on-board distributed power system by means of three control schemes of the bus converter.

2. Impedance analysis

The on-board distributed power system consists of a bus converter and a POL. The half-bridge converter with the most popular circuit of the power–stage is used as a bus converter, and the synchronous buck converter with the most popular circuit is used as a POL. Figure 1 and 2 show the circuit diagrams, respectively. Even if each converter has stable operations, the instability phenomenon may occur by connecting two converters in a series. The input and output impedance is greatly concerned to the system stability. From a previous report of reference15, it is necessary to set the peak value of the output impedance to smaller than the low-frequency value of the input impedance |Zin(0)| for system stability.

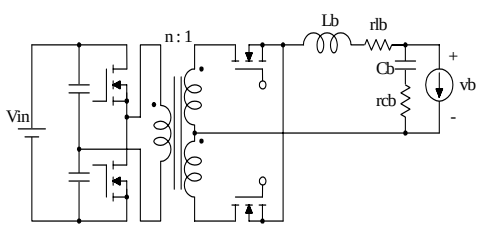

Fig. 1. Bus converter. (Half-bridge converter)

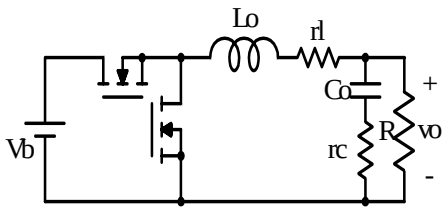

Fig. 2. POL. (buck converter)

$$\begin{cases} |Z_{in}(0)| \geq Z_{o\_peak} & : \ Stable \\ |Z_{in}(0)| < Z_{o\_peak} & : \ Unstable \end{cases} \tag{1}$$

In this section, the low frequency value of the input impedance and the peak value of the output impedance are analyzed.

2.1 Input impedance

At first, the low-frequency value |Zin(0)| of the input impedance is estimated. The input impedance of POL can be derived as the following equation[17-19].

$$\frac{1}{Z_{in}(s)} = \frac{1}{Z_N(s)} \cdot \frac{T_p(s)}{1+T_p(s)} + \frac{1}{Z_D(s)} \cdot \frac{1}{1+T_p(s)} \tag{2}$$

From Eq. (2), the low-frequency value of the input impedance |Zin(0)| is given by the following equation.

$$\left|Z_{in}(0)\right|_{(dB\Omega)} \approx 20\log\left(\frac{R+r_L}{D^2}\right) \quad (dB\Omega) \tag{3}$$

|Zin(0)| has minimum value at rated load, so the estimation of |Zin(0)| must be at rated load. Next, the output impedance is examined.

2.2 Output impedance

The output impedance of a bus converter can be derived.

Open loop case,

$$Z_o(s) = \frac{s^2 L_b C_b r_{c_b} + s\left(L_b + C_b r_{L_b} r_{c_b}\right) + r_{L_b}}{s^2 L_b C_b + s C_b \left(r_{L_b} + r_{c_b}\right) + 1} \tag{4}$$

Closed loop case,

$$Z_{oc}(s) = \frac{Z_o(s)}{1 + T_b(s)} \tag{5}$$

where,

$$T_b(s) = k \cdot PWM \cdot G_{dv_b}(s) \tag{6}$$

$$G_{dv_b}(s) = \frac{V_s}{P_b(s)}\left(sC_b r_{c_b} + 1\right) \quad \text{(Vs=Vin/2n)} \tag{7}$$

$$P_b(s) = s^2 L_b C_b + sC_b\left(r_{L_b} + r_{c_b}\right) + 1 \tag{8}$$

k : sense gain products error amp. gain.
PWM : gain of the comparator.

In an open loop case, the peak frequency is the same resonant frequency fp of the loop gain T(s) as shown in Fig. 3, and the peak value of the output impedance can be derived from Eq. (4).

$$Z_{o\_peak} = \frac{L_b}{C_b\left(r_{c_b} + r_{L_b}\right)} \tag{9}$$

In a closed loop case, the output impedance peak moves to crossover frequency fc as shown in Fig. 3. In this instant the peak value of the closed loop output impedance can be derived from the following equation,

$$Z_{oc\_peak} = \frac{L_b}{C_b\left\{(1+\alpha) r_{c_b} + r_{L_b}\right\}} \tag{10}$$

where,

$$\alpha = \left|T(0)\right| = k \cdot PWM \cdot V_s \tag{11}$$

Moreover, from the transfer function of loop gain, the crossover frequency fc is expressed as follows by means of peak frequency fp of the loop gain.

$$f_c = \sqrt{1+\alpha}\, f_p \tag{12}$$

From Eq. (10) (12), the peak value of a closed loop output impedance is expressed as follows.

$$Z_{oc\_peak} = \frac{L_b}{C_b\left\{\left(\frac{f_c}{f_p}\right)^2 r_{C_b} + r_{L_b}\right\}} \tag{13}$$

As shown in Eq. (13), if fc is equal to fp, it becomes the same as Eq(9). Therefore, the peak value of output impedance is calculable by means of Eq. (13).

3. Output impedance characteristics

The output impedance characteristic of each control shames (un-regulated, semi-regulated, and full-regulated) is different, and each bus converter has different operations. Therefore, the output impedance design suitable for the feature of each control method is required. From now on, the output impedance design for each control shames is considered.

3.1 Un-regulated

In an un-regulated case, the output impedance is the same as open-loop output impedance because this control method has no control loop. In order to reduce the peak value of output impedance, it is effective to make the inductance small or to enlarge the capacitance.

Generally, an un-regulated bus converter is operated at a maximum duty ratio. Therefore, the inductor of the bus converter can be reduced as small as possible to reduce the system instability. The peak value of the output impedance is reduced with the small inductor. Figure 4 shows the experimental result of the relationship between the output impedance and inductance. Moreover, Fig. 5 shows the analytical and experimental results of the relationship between the peak value of output impedance and inductance. Both results agreed well with each other.

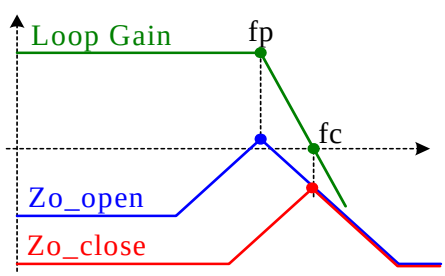

Fig. 3. Output impedance peak.

3.2 Semi-regulated

A semi-regulated bus converter has a control loop. However, regulation is related to a variation of input voltage, therefore the output impedance is the same as an un-regulated case. In this case, the duty ratio is changed, and the inductor of the bus converter cannot be reduced.

Therefore, a very large bus capacitor is needed to reduce the peak value of output impedance.

Figure 6 shows the experimental result of the relationship between the output impedance and capacitance. Moreover, Fig. 7 shows the analytical and experimental results of the relationship between the peak value of output impedance and capacitance. Both results agreed well with each other.

3.3 Full-regulated

A full-regulated bus converter has a feedback loop, so the output impedance characteristic is changed. Therefore, output impedance can be made small with a wide bandwidth. Figure 8 shows the experimental result of the relationship between the output impedance and bandwidth. Moreover, Fig. 9 shows the analytical and experimental results of the relationship between the peak value of output impedance and bandwidth. Both results agreed well with each other.

Next, the relationship between the capacitance and output impedance peak is examined in a closed loop case. In a closed loop case, if capacitance Cb changes to Cb+Cadd, the peak frequency fp of the loop gain is changed as follows.

$$f_p' = \frac{1}{2\pi\sqrt{L_b\left(C_b + C_{add}\right)}} \tag{14}$$

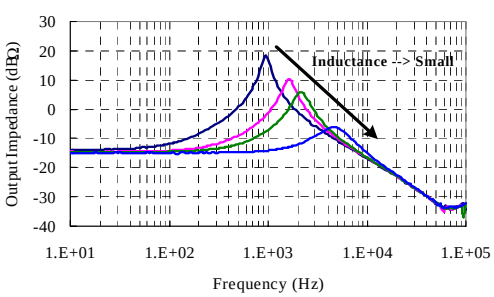

Fig. 4. Inductance and output impedance.

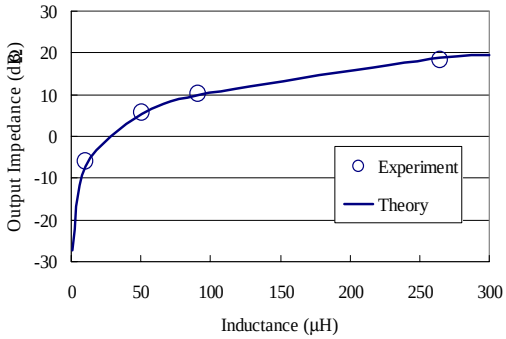

Fig. 5. Inductance and peak value of Zo.

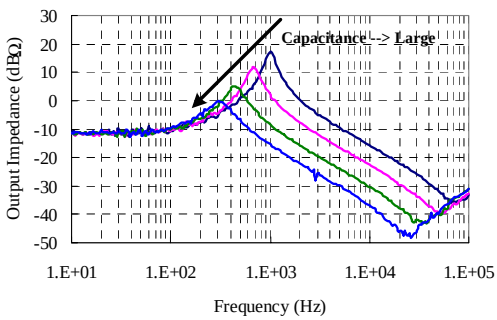

Fig. 6. Capacitance and output impedance.

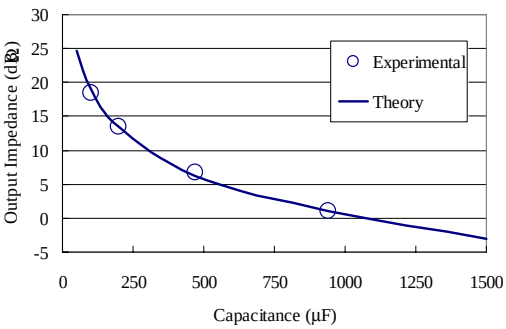

Fig. 7. Capacitance and peak value of Zo.

Therefore, the crossover frequency fc is changed as follows.

$$f_c' = \sqrt{1+\alpha}\, f_p' \tag{15}$$

Moreover, frequency ratio fc'/fp' is given as the following equation.

$$\frac{f_c'}{f_p'} = \frac{f_c}{f_p} \tag{16}$$

From these results, output impedance peak can be expressed as in the following equation.

$$Z_{oc\_peak}' = \frac{k_{esr} C_b}{(C_b + C_{add})} Z_{oc\_peak} \quad (17)$$

where,

$$k_{esr} = \frac{(1+\alpha) r_{cb} + r_{Lb}}{(1+\alpha) r_{cb}' + r_{Lb}} \quad (18)$$

Figure 10 shows the experimental result of the relationship between the output impedance and capacitance in a closed loop case. Moreover, Fig. 11 shows the analytical and experimental results of the relationship between the peak value of output impedance and capacitance in a closed loop case. Both results agreed well with each other. In this case, the total ESR is greatly changed by the additional capacitor.

Moreover, the total ESR is quite changed by the additional capacitor. Furthermore, in the case of the closed loop, ESR has a great influence to the output impedance peak. Therefore, estimation of ESR is very important.

4. Optimal design of bus converter

In order to evaluate the performance of this system, the experiment circuits are implemented using the specifications and parameters in Table 1.

Table 1 Circuit parameters

	Symbol	Description	Value
Bus Converter	Vin	Input Volotage	48V
	Vb	Bus Volotage	12V
	Lb	Output Inductor of Bus Converter	270μH
	Cb	Output Capacitor of Bus Converter	100μF
	rlb	Registance of Lb	300mΩ
	rcb	ESR of Cb	25mΩ
	kb	Feedback gain (with sence gain)	0.9
POL	Vo/Io	Output Condition	3.3V/5A
	Lo	Output inductor	2.8μH
	Co	Output capacitor	820μF
	rl	Registance of Lo	25mΩ
	rc	ESR of Co	10mΩ

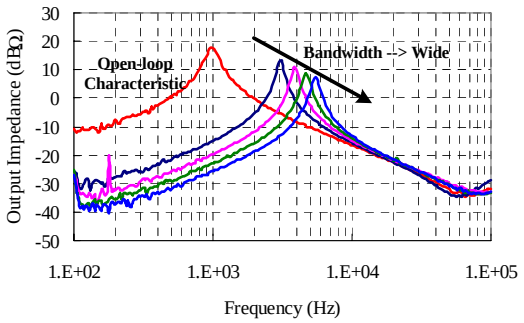

Fig. 8. Bandwidth and output impedance.

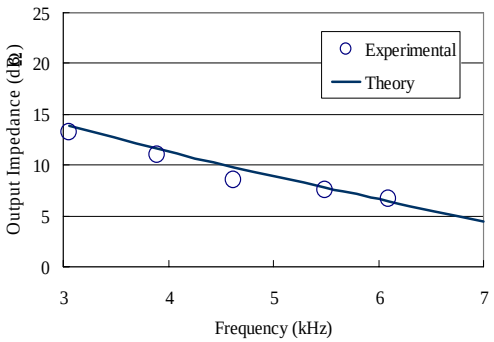

Fig. 9. Bandwidth and peak value of Zo.

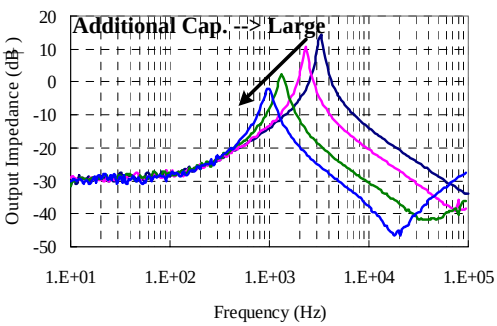

Fig. 10. Additional capacitance and output impedance.

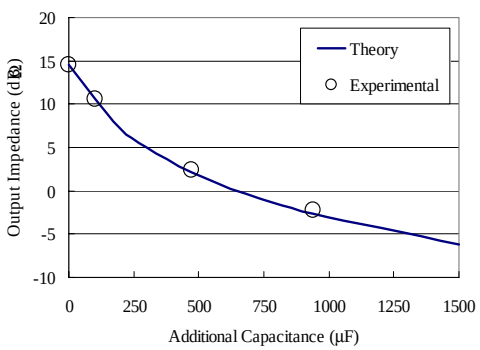

Fig. 11 . Additional capacitance and peak value of Zo.

Here, the case with two POLs is discussed as an actual example. The practical design process is shown below.

4.1 Input impedance estimation

The low-frequency value |Zin(0)| of input impedance is given by Eq. (3). The duty ratio is D=0.275 and output resistance is R=0.66(Ω) from the relational input and output. In this case, the |Zin(0)| is 20.6(dBΩ). When two POLs of the same condition are connecting in a parallel, |Zin(0)| is 14.6(dBΩ). Figure 14 shows the experimental result of the input impedance. The low-frequency value |Zin(0)| is around 15(dBΩ) as shown in Fig. 12. The experimental results and analytical results also compliment each other well. If the stability margin is set to 6(dBΩ), then the peak value of the output impedance must be set to around 9(dBΩ).

In an un-regulated case, the optimal inductance value is considered because the stability is improved by small inductance. From Eq. (13), the optimal inductance value can be derived as following equation.

$$L_{b\_optimal} = C_b \left(r_{C_b} + r_{L_b} \right) Z_{o\_peak} \tag{19}$$

where, the unit of |Zo_peak| is Ω.

Since the output impedance must be set to 9(dBΩ), the inductance value is set to around 87(μH) from Eq. (19). Figure 13 shows the experimental result of the output impedance with small inductance.

The inductance value is around 90 (μH), and the peak value of the output impedance is around 8.5 (dBΩ).

The experimental results and analytical results further agree well. Moreover, in an open loop case, since the rL is generally larger than the rc, the output impedance does not become smaller than rL as shown in Fig. 4.

Therefore, the inductance value has minimum value. From Eq. (19), the minimum value of the inductance is given by the following equation.

$$L_{b\_\min} = C_b \left(r_{C_b} + r_{L_b} \right) r_{L_b} \tag{20}$$

In this case, the minimum value of inductance is around 10 (μH).

In a semi-regulated case, the optimal capacitance value is considered because the stability is improved by large capacitance. From Eq. (13), the optimal capacitance value can be derived as in the following equation.

$$C_{b\_optimal} = \frac{L_b}{\left(r_{C_b} + r_{L_b} \right) Z_{o\_peak}} \tag{21}$$

where, the unit of |Zo_peak| is Ω. Since the output impedance must be set to 9(dBΩ), the capacitance value is set to around 300(μF) from Eq. (16). In this case, the influence of the ESR is considered because the ESR becomes small when the capacitor is connected in parallel.

Figure 14 shows the experimental result of the output impedance with a large capacitance. The capacitance value is 300 (μF), and the peak value of the output impedance is around 8 (dBΩ). The experimental results and analytical results agree well with each other.

Moreover, the output impedance does not become smaller than rL as shown in Fig. 6. Therefore, the capacitance value has maximum value. From Eq. (21), the maximum value of the capacitance is given by the following equation.

$$C_{b\_\max} = \frac{L_b}{\left(r_{C_b} + r_{L_b} \right) r_{L_b}} \tag{22}$$

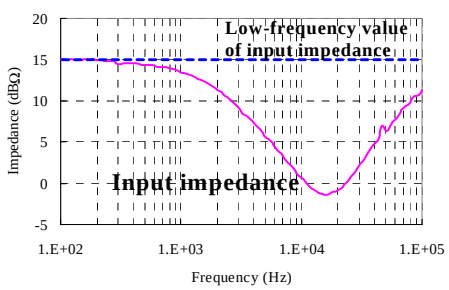

Fig. 12. Input impedance characteristic.

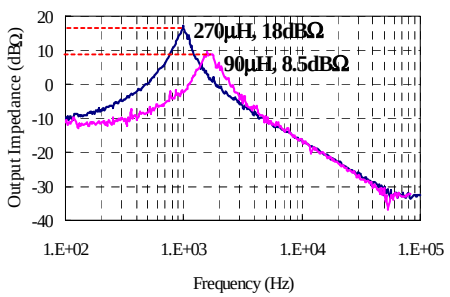

Fig. 13. Output impedance with small inductor.

In this case, the maximum value of the capacitance is around 2.8 (mF).

In a full-regulated case, the optimal bandwidth is considered because the stability is improved by wide bandwidth. From Eq. (13), the optimal bandwidth can be derived as in the following equation.

$$f_{c\_optimal} = f_p \sqrt{\frac{\frac{L_b}{C_b Z_{oc\_peak}} - r_{L_b}}{r_{C_b}}} \quad (23)$$

where, the unit of |Zo_peak| is Ω. Since the output impedance must be set to 9(dBΩ), the bandwidth is set to around 5.1kHz from Eq. (23). Figure 15 shows the experimental result of the output impedance with wide bandwidth. The bandwidth is around4.7kHz, and the peak value of output impedance is around 8.5 (dBΩ). The experimental results and analytical results soundly agree with each other.

Next, the optimal capacitance is considered in closed loop case. From Eq. (17), the optimal additional capacitance can be derived as in the following equation.

$$C_{add\_optimal} = \left(\frac{k_{esr} Z_{oc\_peak}}{Z_{oc\_peak}'} - 1 \right) C_b \quad (24)$$

In the basic parameters case, the closed loop output impedance peak is around 14.5(dBΩ). Since the output impedance must be set to 9(dBΩ), the additional capacitance is set to around 150μF from Eq. (24). Figure 16 shows the experimental result of the output impedance with additional capacitance. The capacitance is around 150μF, and the peak value of the output impedance is around 9 (dBΩ). The experimental results and analytical results agree well with each other.

5. Conclusions

This paper presents the output impedance design for an on-board distributed power system by means of three control methods of a bus converter. The output impedance peak of the bus converter and the input impedance of the POL were analyzed, and it was conformed experimentally for the stability criterion. As a result, the standard of the discrimination of stability on a frequency response of input and output impedance was clarified. Furthermore, the design process of each control method for system stability was proposed.

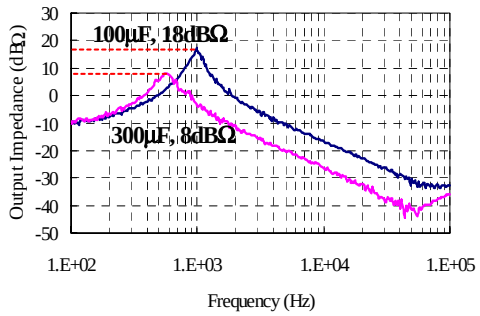

Fig. 14. Output impedance with large capacitor.

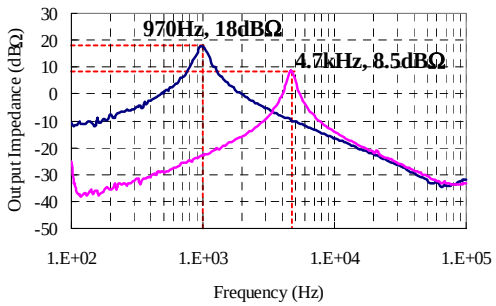

Fig. 15. Output impedance with wide bandwidth.

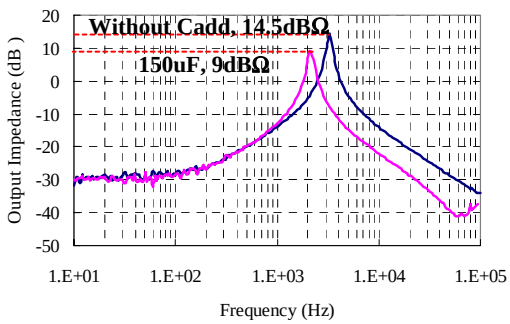

Fig. 16. Output impedance with additional capacitance.

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