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Verification of an Autonomous Decentralized UPS System with Fast Transient Response Using a FPGA-Based Hardware Controller

Tomoki Yokoyama†, Nobuaki Doi*, and Toshiya Ishioka*

†*Dept. of Computers and Systems Eng., Tokyo Denki University, Saitama, Japan

ABSTRACT

This paper proposes an autonomous decentralized control for a parallel connected uninterruptible power supply (UPS) system based on a fast power detection method using a FPGA based hardware controller for a single phase system. Each UPS unit detects only its output voltage and current without communications signal exchange and a quasi dq transformation method is applied to detect the phase and amplitude of the output voltage and the output current for the single phase system. Fast power detection can be achieved based on a quasi dq transformation, which results in a realization of very fast transient response under rapid load change. In the proposed method, the entire control system is implemented in one FPGA chip. Complicated calculations are assigned to hardware calculation logic, and the parallel processing circuit makes it possible to realize minimized calculation time. Also, an Nios II CPU core is implemented in the same FPGA chip, and the software can be applied for non-time critical calculations. Applying this control system, an autonomous decentralized UPS system with very fast transient response is realized. Feasibility and stable operation are confirmed by means of an experimental setup with three UPSs connected in parallel. Also, rapid load change is applied and excellent performance of the system is confirmed in terms of transient response and stability.

Keywords: UPS, FPGA, Autonomous decentralized control, Quasi dq transformation

1. Introduction

Information technology realizes the worldwide communication network and many social infrastructures have to work 24 hours per day, 365 days per year, to ensure communications reliability. Uninterruptible power supplies (UPSs) are employed because of the increasing importance of reliable power supplies for critical loads. Parallel operation of redundant UPS systems is widely used to achieve reliable power supply systems. Generally, a master-slave control [1] method has been adopted to realize stable operation of parallel UPS systems. In this method, one master controller detects the total load current, then calculates the current references for each UPS unit, then transfers them through an exclusive communication line. In this system, to increase the number of parallel UPS units, the master controller has to recognize the number of parallel UPS units and the communication line also has to be maintained. In the case of failure of the master controller, one of the slave controllers has to detect the loss of the master controller and change the slave function to the

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†Corresponding Author:yoko@k.dendai.ac.jp

Tel:+81 0492962911, Fax:+81 0492966185, Tokyo Denki Univ.

*Dept. of Computers and Systems Eng., Tokyo Denki Univ., Japan

master function by itself, so a very complicated sequence control has to be implemented in the controller.

On the other hand, an autonomous decentralized UPS system has been presented [2]-[5]. In this system, autonomous load share characteristics are realized without any communication line between each UPS unit, so the extension capability of the system is much improved compared with the master-slave control method, and the complicated sequence control is not necessary because no master controller exists in the system and each UPS unit operates independently.

In the case of a three phase system, using an $\alpha\beta$ transformation and a *dq* transformation, instantaneous phase and amplitude information of the target line voltage and current can be detected, then applying the droop control based on the detected output power, an autonomous decentralized control can be achieved [2]. On the other hand, in the case of a single phase system, it is difficult to detect the phase and amplitude of the line voltage and current as fast as with a three phase system.

In [5], by using a one cycle integration method for measuring current to detect the output power in a single phase system, an autonomous decentralized UPS system was realized. But this power detection method essentially involves a detection delay of the output power, so fast transient response cannot be expected. In [6]–[9], the authors proposed an autonomous decentralized UPS system based on a quasi *dq* transformation using a FPGA based hardware controller. A quasi *dq* transformation method can detect the phase and the amplitude for a single phase system with only three sampling data points, so instantaneous power detection can be achieved. Thus, fast transient response of the autonomous decentralized control can be realized even under rapid load change. In [9], the experimental result for parallel operation with two UPS units was shown and steady state characteristics were confirmed. But to confirm the proper operation of the autonomous decentralized UPS system, more than three units are required in the experimental system.

In this paper, the experimental result for three UPSs connected in parallel was determined and verified. Also, the transient response for rapid load change was also determined and stable operation of the proposed method was verified.

2. System Modeling and Control Method

In the case of the proposed autonomous decentralized control UPS system, there is no need to communicate with the other UPS units with an exclusive communication line, so an easy plug-in, plug-out secure power island can be realized as shown in Fig. 1. Each UPS unit treats the output power autonomously by itself, so the user can easily increase the number of units to increase the total system capability. Fig. 2 shows a basic parallel-connected UPS system where the voltage v_i is the output voltage for the ith UPS unit as $v_i = E_i \cos(\omega t + \phi_i)$. Each UPS is controlled independently with the same control law, and it is assumed that each UPS can observe only its output voltage and current.

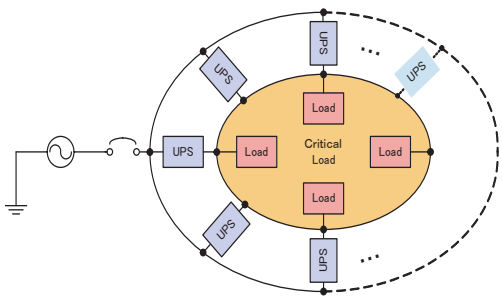

Fig. 1. Autonomous Decentralized Control UPS system.

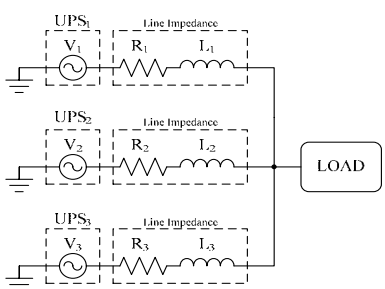

Fig. 2. Model of parallel-connected single-phase UPS system.

2.1 Droop Control

The phase and the voltage amplitude are controlled based on a droop characteristics in this system. The control factors for the output voltage are the phase ϕ_i and

the voltage amplitude E_i. The reference of the phase ϕ_i^* and the reference of the voltage amplitude E_i^* are determined according to the active power of the i th UPS P_i and the reactive power of the i th UPS Q_i. Fig. 3 shows how to decide the phase ϕ_i^* and the voltage amplitude E_i^* based on the droop characteristics. The active element and the reactive element of the output voltage, and the active element and the reactive element of the output current can be detected by a quasi *dq* transformation [12].

Equation (1) and (2) indicate how to decide the phase and the voltage amplitude from the active power and the reactive power. By differentiating the rated active power of the i th UPS P_{0i} and the active power of the i th UPS P_i, then multiplying by the droop characteristics gain m_i, and subtracting from the nominal phase ϕ_0, the desired phase reference ϕ_i^* is derived. Also, by differentiating the rated reactive power of the i th UPS Q_{0i} and the reactive power of the i th UPS Q_i, then multiplying by the droop characteristics gain n_i, and subtracting from the nominal voltage amplitude E_0, the desired voltage amplitude reference E_i^* is derived.

The share ratio of the output power can be determined by the selection of P_{0i} and Q_{0i} for each UPS unit. If two UPSs were connected to the load and P_{01} and P_{02}, Q_{01} and Q_{02} were settled equally, each UPS would supply the power equally to the load.

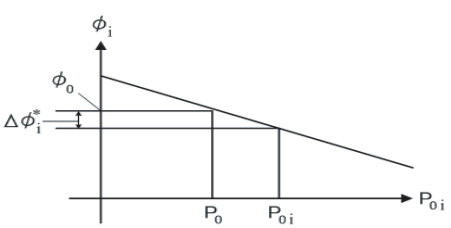

Fig. 3. Droop characteristics.

If the ratio of P_{01} and P_{02}, Q_{01} and Q_{02} were changed, the balance of the output power would vary according to the ratio of these parameters.

$$\phi_i^* = \phi_0 - m_i(P_{0i} - P_i) \tag{1}$$

$$E_i^* = E_0 - n_i(Q_{0i} - Q_i) \tag{2}$$

E_i^* : reference of voltage amplitude
E_0 : nominal voltage amplitude
ϕ_i^* : reference of phase
ϕ_0 : nominal phase
P_{0i} : rated active power for i th UPS
Q_{0i} : rated reactive power for i th UPS
n_i, m_i : droop characteristics gain
Vd_{01} : phase voltage for i th UPS
Id_{0i} : phase current for i th UPS
Iq_{0i} : phase current for i th UPS

2.2 Quasi *dq* Transformation

A quasi dq transformation was used to detect an instantaneous phase and the amplitude of a single phase voltage. The target waveform V_S is assumed as the normal line voltage, and is sampled in every sampling period T_S, so the present sampled data $V_S(k)$ can be described as equation (3). Also, pre-sampled data $V_S(k-1)$ and $V_S(k-2)$ can be expressed as (4) and (5). Here, V_L is the maximum peak value of V_S, and $V_S(k-1)$ is defined as V_α [11].

$$V_S = V_L \cos(\omega t) \tag{3}$$

$$V_S(k-1) = V_L \cos\{\omega(t - T_S)\} = V_\alpha \tag{4}$$

$$V_S(k-2) = V_L \cos\{\omega(t - 2T_S)\} \tag{5}$$

By differentiating (3) and (5) and adapting the formula of the trigonometric function, (6) can be derived.

$$\frac{V_S(k-2)-V_S(k)}{2\omega T_S}=\frac{V_L}{2T_S}\left[\cos\{\omega(t-2T_S)\}-\cos\omega t\right]$$

$$=\frac{V_L}{2T_S}\left[-2\sin(-T_S)\sin\{\omega(t-T_S)\}\right]$$

$$\cong V_L\sin\{\omega(t-T_S)\}=V_\beta \qquad (6)$$

Here, it is obvious that the phase of V_β delays $90°$ more than the phase of V_α, so using only three sampled data points of the single phase waveform, V_α and V_β form a rectangular coordinates system, and a dq transformation can be adopted to the single phase system. Therefore, the phase and the voltage amplitude can be detected from three sampling data points using a quasi dq transformation. In order to reduce the influence of the noise of the target waveform, three kinds of sampling frequencies are adopted for the implementation, which are 20[kHz], 10[kHz] and 6.7[kHz], respectively. Three parallel calculation circuit blocks are prepared and each block is driven by three different sampling frequencies. By averaging the calculated values of every circuit one can derive dq elements of the target waveform.

2.3 Control Block Diagram for Single Phase UPS System

Fig. 4 shows the proposed control block diagram of the single phase UPS system. ϕ_{V_i} is the phase of the output voltage for the i th UPS. The single phase UPS is controlled by the droop control and the PLL control based on the quasi dq transformation [12]. It is assumed that each UPS can observe only its output voltage and current. The phase and the voltage amplitude can be detected by the quasi dq transformation. The operation frequency is detected by the PLL control using the phase ϕ_{V_i} of the i th UPS output voltage.

Also, the active power of the i th UPS can be obtained by multiplying the voltage amplitude and the current amplitude, and the reactive power of the i th UPS can be obtained by multiplying the voltage amplitude and the phase of the output current, which is normalized to calculate the reactive power. The phase reference ϕ_i^* and the voltage amplitude reference E_i^* can be decided by applying the phase and the voltage amplitude control based on the droop characteristics using the active power P_{0i} and the reactive power Q_{0i} .Therefore, the voltage of each UPS can be controlled and each UPS supplies balanced power to the load.

3. Simulation

Simulations were carried out for the step response of the load change. The parameters for the simulations are shown in Table 1.

3.1 Load Variation

The load is changed from R_1 to R_2 at 0.5 seconds with two parallel-connected UPSs and each UPS is settled in the same rated output power references. Fig. 5 shows the active power, the reactive power, the output current of each UPS, and the load current, respectively. From this figure, it is confirmed that the active power and the reactive power of the load are supplied equally from the two

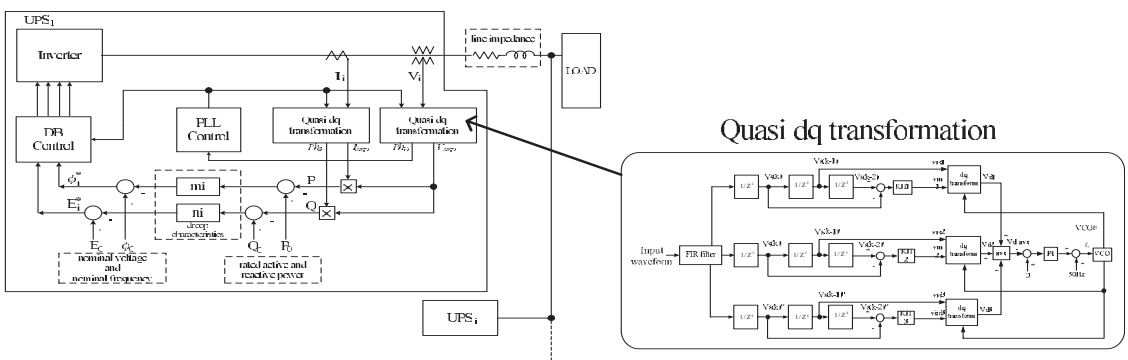

Fig. 4. Control block diagram for one single phase UPS system.

UPSs while the load is changed.

Table 1 Simulation Conditions

rated active power of i th UPS P_{0i}	1000 [W]
rated reactive power of i th UPS Q_{0i}	0 [Var]
nominal frequency f	50.0 [Hz]
sampling frequency	20.0 [kHz]
reference of voltage amplitude E_{0i}	100 $\sqrt{2}$ [V]
reference of phase difference ϕ_{0i}	0 [rad]
load R_1	10 [Ω]
load R_2	4 [Ω]

3.2 Rapid Load Change

The stability of the system is verified when rapid load change occurs ten times in one cycle.

Fig. 6 shows the load current and the output current of each UPS. Even under such conditions, each UPS supplies balanced current to the load because of the fast response of the power detection based on the quasi dq transformation.

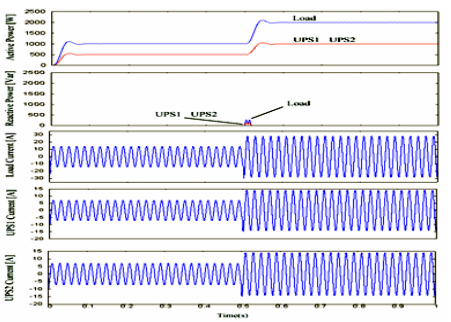

Fig. 5. Step response for the load change in two parallel connected UPSs.

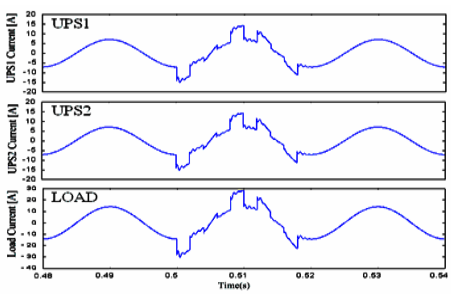

Fig. 6. Rapid load change in one cycle in two parallel connected UPSs.

4. Experiment

4.1 System Design

The parameters for the experimental setup are shown in Table 2. The proposed single phase UPS control system was implemented using a FPGA with a 32bit Nios II processor [14] as shown in Fig. 7. A StratixII EP2S60(ALTERA Corp.) is applied in this system. The Nios II CPU has a pipelined RISC architecture and reconfigurable features. In the experiments of the proposed single phase UPS system, a quasi dq transformation, PLL control and gate pulse generation block were implemented in FPGA logic. The operations such as droop control were implemented in Nios II CPU software.

Table 2 Experimental Conditions

Controller Board	Altera NiosII Development Kit
FPGA Device	Altera Stratix2 2S60
CPU Core	Altera NiosII CPU
rated active power of i th UPS P_{0i}	62.5 [W]
rated reactive power of i th UPS Q_{0i}	0 [Var]
Nominal frequency f	50.0 [Hz]
sampling frequency	20.0 [kHz]
reference of voltage amplitude E_{0i}	25$\sqrt{2}$ [V]
Reference of phase difference ϕ_{0i}	0 [rad]

4.2 Experimental System

Fig. 8 shows the module block diagram of the proposed single phase UPS system in the FPGA with a 32bit Nios II processor. The FPGA blocks are constructed with a quasi dq transformation block, PI control block and VCO block. In the Nios II CPU blocks, a power calculation block, droop control block and reference of output voltage calculation block are implemented. Two quasi dq transformation blocks are constructed in parallel, which calculates the different sampling frequency, and the phase difference and the amplitude are calculated for every control cycle. In the FPGA, the phase difference ϕ_{V_i}, ϕ_{I_i} and the voltage amplitude V_{amp_i}, I_{amp_i} can be calculated by the quasi dq transformation using the i th UPS output voltage and the i th UPS output current. Also, the

operation frequency f is detected by the PLL control using the phase difference of the i th UPS output voltage ϕ_{V_i}. These values (V_{amp_i}, I_{amp_i}, ϕ_{I_i}, f) are sent to the Nios II CPU. In the Nios II CPU, the reference of the output voltage is decided by the droop control.

Fig. 9 shows the circuit schematics of logic element(LE) wiring in the FPGA chip. The upper square area corresponds to the NiosII CPU.

Fig. 10 shows the timing chart of the FPGA based hardware controller. The A/D conversion and hardware calculation are finished in 1.18us(73clocks), the software calculation is finished in 12.3us, and all the calculations are finished in 13.6us.

A Stratix II (EP2S60), which has 60,440LE (logic elements), is used for the FPGA controller and 20% of the LE are used for the proposed control logic including the Nios II CPU core.

Fig. 11 shows the FPGA based hardware controller and Fig. 12 shows the experimental system for the parallel connected UPS.

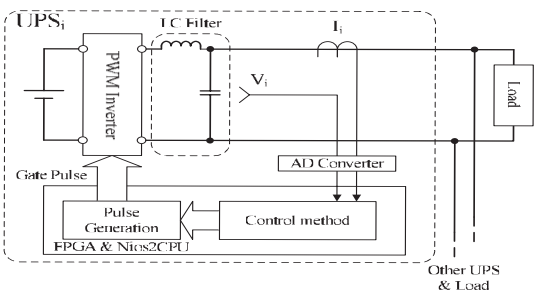

Fig. 7. FPGA Based Hardware Controller System configuration.

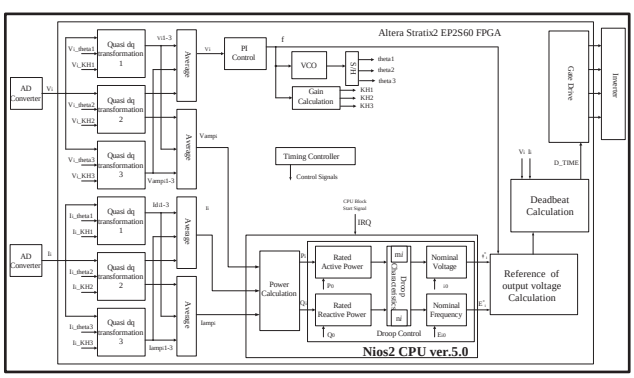

Fig. 8. Module block diagram of FPGA controller.

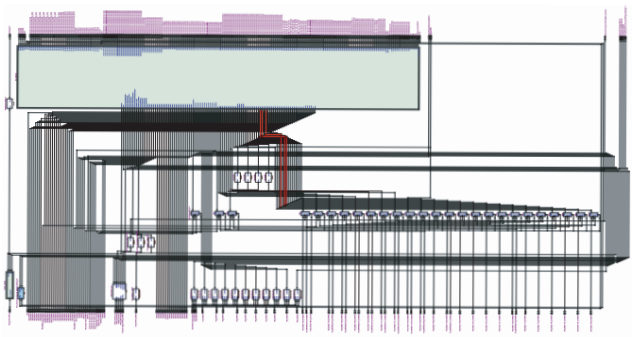

Fig. 9. Circuit schematics of logic element wiring in one FPGA Controller.

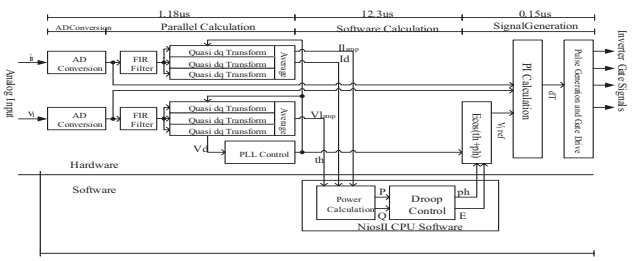

Fig. 10. Timing chart of the hardware logic and software.

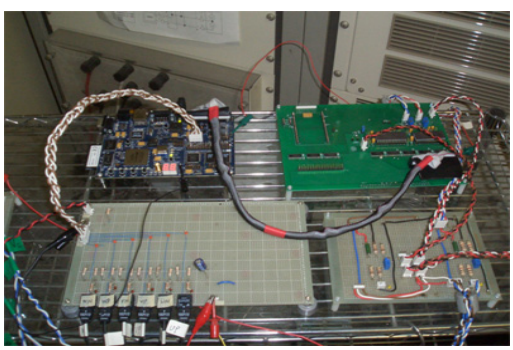

Fig. 11. Controller circuit.

Fig. 12. Overview of Experimental System.

4.2.1 Two parallel connected UPSs

In the experimental system, the two parallel connected UPS setup was verified. Under the condition that UPS_1 supplied the power to the load, UPS_2 was connected and disconnected to the load line. In the case of share ratio 1:1, P_{01} and P_{02} are settled equally to 62.5[W]. From Fig. 13 and Fig. 14, it is confirmed that the two UPSs shared the load current equally.

Fig. 15 and Fig. 16 show the experimental results when the share ratio is settled to 1:2. Table 3 shows the load share characteristics when the share ratio of P_{01} and P_{02} was changed. Fig. 17 shows power balance characteristics. It is confirmed that the load share balance can be controlled by the ratio of the rated power gain P_{01} and P_{02}.

Table 3 Load Share Characteristics

Share ratio (Setting)		P0i [W]	Q0i [Var]	P [W]	Q [Var]	Power Balance (Result)
1:0.5	UPS1	62.5	0.0	44.64	0.0	1.00:0.47
	UPS2	31.25	0.0	20.78	0.0	
1:0.75	UPS1	62.5	0.0	37.65	0.0	1.00:0.68
	UPS2	46.875	0.0	25.64	0.0	
1:1	UPS1	62.5	0.0	31.92	0.0	1.00:0.94
	UPS2	62.5	0.0	30.23	0.0	
1:1.5	UPS1	62.5	0.0	25.06	0.0	1.00:1.49
	UPS2	93.75	0.0	37.27	0.0	
1:2	UPS1	62.5	0.0	21.98	0.0	1.00:1.91
	UPS2	125.0	0.0	42.02	0.0	
1:2.5	UPS1	62.5	0.0	18.65	0.0	1.00:2.35
	UPS2	156.25	0.0	43.74	0.0	
1:3	UPS1	62.5	0.0	15.07	0.0	1.00:3.11
	UPS2	187.5	0.0	46.96	0.0	

4.2.2 Rapid load change

Experiments were carried out for the load fluctuate condition. Two UPS were connected to two different loads (R_1 and R_2) via a bidirectional switch and the load was rapidly changed. Fig. 18 shows the load current and the output current of each UPS. Even under such conditions, each UPS supplies balanced current to the load.

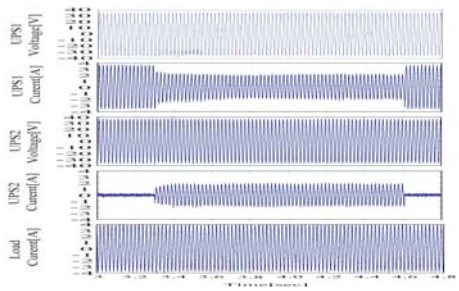

Fig. 13. Voltage and current waveforms for UPS_1 and UPS_2. (share ratio 1:1)

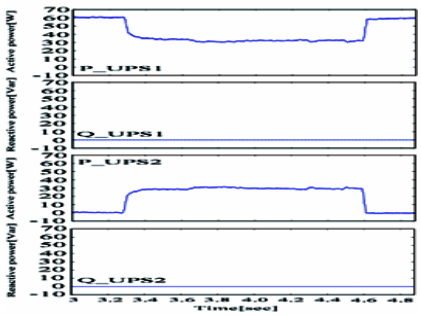

Fig. 14. Active Power and Reactive Power for UPS_1 and UPS_2. (share ratio 1:1)

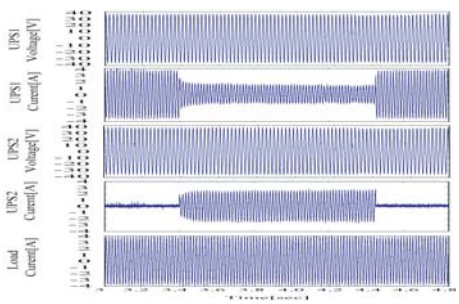

Fig. 15. Voltage and current waveforms for UPS_1 and UPS_2. (share ratio 1:2)

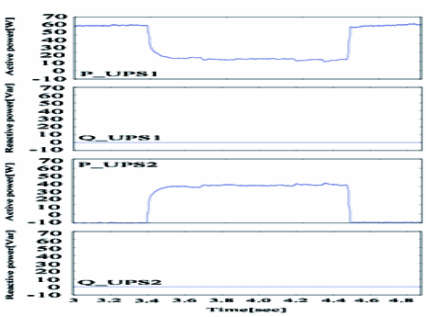

Fig. 16. Active Power and Reactive Power for UPS_1 and UPS_2. (share ratio 1:2)

4.2.3 Three parallel connected UPSs

The three parallel connected UPS setup was verified. Under the condition that UPS_1 and UPS_2 supplied the power to the load, UPS_3 was connected and disconnected to the load line. In the case where the share ratio is settled to 1:1:1, P_{01} and P_{02} and P_{03} supplied the power equally as shown in Table 4 and Fig. 20.

Table 4 Load Share Characteristics

Share ratio (Setting)		P0i [W]	Q0i [Var]	P [W]	Q [Var]	Power Balance (Result)
1:1:1	UPS1	62.5	0.0	21.53	0.0	1.00
	UPS2	62.5	0.0	20.50	0.0	0.95
	UPS3	62.5	0.0	19.87	0.0	0.92

5. Conclusions

In this paper, an autonomous decentralized control system for a single phase UPS inverter with a FPGA based hardware controller using a software CPU core is proposed. A quasi dq transformation method is applied to detect the phase and amplitude of the output voltage and the output current for the single phase system. Fast power detection is achieved, which results in a realization of very fast transient response during rapid load change. By applying the proposed method in a parallel-connected single phase UPS system, each UPS shares the power of the load equally when the power of the load changes or the number of the connected UPSs changes and an autonomous decentralized control for a single phase UPS system with very fast transient response is realized. When constructing the control system using a FPGA, a HW/SW co-design procedure was applied to determine the optimal control system. Through simulations and experiments, the proper operation of the proposed method was verified.

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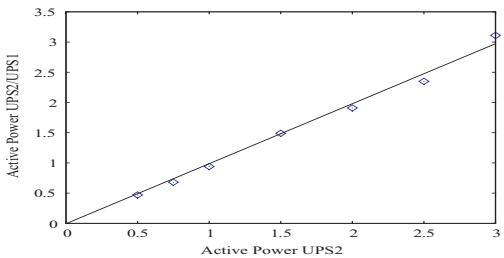

Fig. 17. Power balance characteristics.

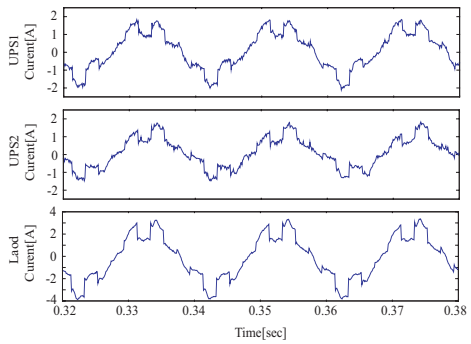

Fig. 18. Current Waveforms in Rapid Load Change.

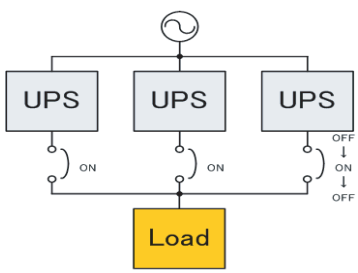

Fig. 19. Experimental setup of three parallel connected UPSs.

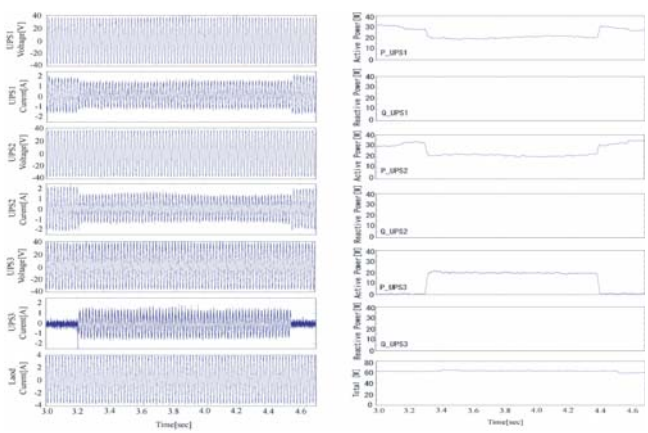

Fig. 20. Power Balance in three parallel UPSs operation.

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Tomoki Yokoyama was born in Hiroshima Prefecture, Japan in 1965. He received the B.S., M.S and Ph.D. degrees in Electrical Engineering from Yokohama National University, Kanagawa, Japan, in 1988 and 1994, respectively. In 1994, he joined Toshiba Corporation Japan. In 1998, he joined Tokyo Denki University. He is currently an associate professor. His research interests are in the areas of advanced control of power electronics. Prof. Yokoyama is a member of the Institute of Electrical Engineers of Japan.

Nobuaki Doi was born in Tokyo Prefecture, Japan in 1984. He received the B.S. degree in Electrical Engineering from Tokyo Denki University, Saitama, Japan, in 2007. His research interests are in the areas of advanced control of power electronics. Mr. Doi is a student member of the Institute of Electrical Engineers of Japan.

Toshiya Ishioka was born in Chiba was born in Chiba Prefecture, Japan in 1986. He received the B.S. degree in Electrical Engineering from Tokyo Denki University, Saitama, Japan, in 2008. His research interests are in the areas of advanced control of power electronics. Mr. Ishioka is a student member of the Institute of Electrical Engineers of Japan.