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Combined Dithered Sigma-Delta Modulation based Random PWM Switching Scheme

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ABSTRACT

The PWM (Pulse Width Modulation) control signals have a drawback in that their power spectrum tends to be concentrated around the switching frequency and the resulting harmonic spikes cause an EMI (Electromagnetic Interference) and switching losses in semiconductors, etc. The SDM (Sigma-Delta Modulation) is a type of switching modulation used to reduce these harmonic spikes, and several SDM schemes are investigated in this paper. In the DSDM (Dithered SDM), the SDSDM (Space-Dithered SDM) and TDSDM (Time-Dithered SDM), the signals are classified by the location of their random dither additions. In these schemes, the switching frequency is spread by a random dither generator placed on the input or the output parts. Experimental results are presented where the advantages of the new proposed CDSDM (Combined Dithered SDM) are confirmed by applying to a buck converter.

Keywords: Sigma-Delta Modulation, Random PWM, DC/DC converter

1. Introduction

Pulse Width Modulation (PWM) signals have been widely employed in power-electronic applications[1-2], but they have a drawback in that their power spectra tend to be concentrated around the switching frequency, causing a lot of harmonics. The harmonic spikes can have serious undesirable effects, such as acoustic noise, harmonic heating effects, mechanical vibration, switching losses in the semiconductor and electromagnetic interference[3]. Numerous soft switching techniques have been used to solve these problems, but there is a limit on reducing the current stresses and the electromagnetic interference. One method to alleviate these undesirable phenomena is to increase the switching frequency, which results in higher switching losses. Moreover, this solution has a disadvantage that it requires additional filters, and thus the use of supplementary equipments. Another solution is to use the Random PWM (RPWM) scheme, which spreads the switching frequency bandwidth by making the switching on the broad frequency bandwidth[4-6]. The problem with the RPWM is the means by which it is realized; that is, how the random numbers are generated

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and the switching frequency is varied, or how the duty ratio is changed in a random manner. Several random number generation methods have been developed, but normally some hardware is required, along with some complex software algorithms[7].

The Dithered Sigma-Delta Modulation (DSDM) scheme comprising the SDM and a random dither generator can be realized with simple hardware and software algorithms[8]. The SDM is a type of switching modulation and it makes switching pulse waveforms without additional on/off calculation. This means that the output switching frequency can be randomly varied under a constant sampling frequency. In addition, the SDM has an advantage of harmonic-spreading effects, reducing the low-frequency noise so that the harmonics in the switching frequency bandwidth caused by the PWM scheme are also reduced [9]. For this reason, SDM has been used in the converter. However, the SDM has some harmonic spikes, in case of a DC input with a low modulation index. In order to reduce these harmonic spikes, the random dither generator is placed at the input side of the quantizer in the SDM to reduce the harmonic spikes; this scheme is called the Space-Dither SDM (SDSDM). And the random dither generator can be placed at the output side of the quantizer in the SDM, and when this is done, the scheme is called the Time-Dither SDM (TDSDM).

In order to confirm the degree of the harmonic-spreading, we use the standard deviation for the sampling number per switching cycle. In this paper, the CDSDM is explained and improved through an experimental demonstration by an application to a buck converter.

2. SDM (Sigma-Delta Modulation) Scheme

2.1 Conventional PWM and SDM Schemes

So far, many PWM schemes have been developed and implemented successfully for different applications; typical methods are Sinusoidal PWM (SPWM), SDM and RPWM schemes. The SPWM scheme simply generates the switching pulse pattern by comparing a desired reference signal and a triangular carrier waveform. The SDM utilizes a quantizer to generate the switching pulse pattern and consists of an integrator and a two-level quantizer within a feedback loop. The various RPWM schemes randomize the pulse pattern using a random number generator, which causes the harmonic spikes to be greatly reduced.

The most standard PWM scheme is the SPWM, which, as already stated, generates its signal by comparing a reference signal and a high-frequency triangular carrier waveform. Since the switching frequency in the SPWM scheme is always fixed, the switching pulse is easily generated by a Digital Signal Processor (DSP) operating with a constant sampling frequency. In other words, the harmonic power spectrum of the switching pulse waveform is concentrated around the switching frequency and its multiples. These harmonic spikes cause undesirable effects, such as excessive acoustic noise, harmonic heating effects, mechanical vibration, switching losses of the semiconductor and electromagnetic interference.

The SDM has generally been used in A/D conversions together with the over sampling scheme as well as shaping the quantizer noise into the desired high-frequency bandwidth rather than into uniform white noise.

2.2 Fundamental of SDM

The SDM consists of an integrator and a quantizer in a feedback loop, as shown in Fig. 1. The quantizer considered here is a two-level type which the output is either +1 or -1, and its input is the integral of the difference between the input and the quantized output. That is, the quantization error. As an effect of the feedback loop, the average value at the integrator input is brought to zero. An equivalent discrete time model for the SDM can be obtained by using the following difference equation:

$$\begin{aligned} u\big((n+1)T\big) &= x(nT) - y(nT) + u(nT) \\ y(nT) &= +1 \ (if \ u(nT) \ge 0) \\ &= -1 \ (if \ u(nT) < 0) \end{aligned} \tag{1}$$

where $x(nT)$, $u(nT)$, and $y(nT)$ denote the input signal, the integrator state, and the output of the quantizer, respectively.

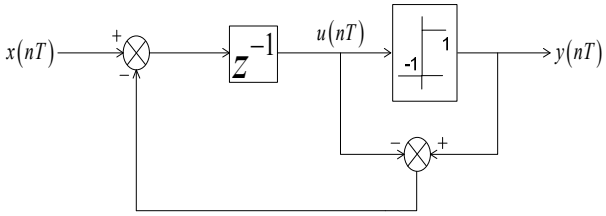


Fig. 1. Block diagram of the SDM.

$$e(nT) = y(nT) - u(nT) \tag{2}$$

With the equation (1) and (2), the output equation can be obtained as

$$y((n+1)T) = x(nT) + e((n+1)T) - e(nT) \tag{3}$$

The output equation in (3) can be rewritten by z-transform as

$$y(z) = z^{-1}x(z) + e(z)(1 - z^{-1}) \tag{4}$$

Using the equation (4), the discrete-time linear system model of the SDM is obtained.

Fig. 2 shows the discrete-time linear system model for a SDM. Using this model, we can derive *x(z)* and *y(z)* as the z-transforms of the input and output sequences respectively**.** The quantizer error is represented as a white, uniform noise process, *N(z)*. Based on Fig. 1 and 2, two transfer functions can be defined; the first is the signal transfer function that shows how the output depends on the input, and the second is the noise transfer function that describes the manner in which the added noise *N(z)* contributes to the output.

$$signal\ transfer\ function = \frac{Y(z)}{X(z)} = z^{-1} \tag{5}$$

$$Noise\ transfer\ function = \frac{Y(z)}{N(z)} = 1 - z^{-1} \tag{6}$$

In order to observe the frequency characteristics of the SDM, z in Equation (6) is replaced with $z = e^{j\omega T_s}$ and

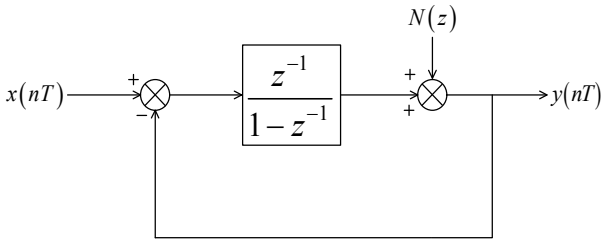


Fig. 2. Discrete-time linear system model of the SDM.

thus, the magnitude of the noise function is obtained as follows:

$$\left|\frac{Y(e^{j\omega T_s})}{N(e^{j\omega T_s})}\right| = 2\left|\sin\frac{\pi \cdot f}{f_s}\right| \tag{7}$$

where T_s denotes the sampling time ($1/f_s$).

Fig. 3 shows that the in-band noise is further decreased and the out-band noise is increased due to the sigma-delta noise shaping. It includes the in-band and out-band noise. On one hand, the in-band noise shows low frequency components, such as DC components and signal bands. On the other hand, the out-band noise shows high frequency components, such as harmonics. By virtue of the above frequency characteristics of the SDM, various kinds of Sigma-Delta Modulation have been used to generate the switching pattern for the switching converters, such as the DC/DC converter [11], resonant converter [12], and the DC/AC converter [13]. However, even the SDM has some harmonic spikes, in case of a DC input with a low modulation index.

2.3 Sampling Number and Switching Period

In order to study the mechanism of the harmonic spikes in the SDM, it is useful to examine the variation of the output's switching periods. If the sampling frequency f_s of the SDM is much larger than the input signal frequency, the switching frequency ratio of the SDM to SPWM can be theoretically calculated under the condition that f_s is equal to the carrier frequency of the SPWM. With a DC input signal, the switching frequency ratio is obtained

$$R = \frac{1}{2} - \frac{1}{2}m \tag{8}$$

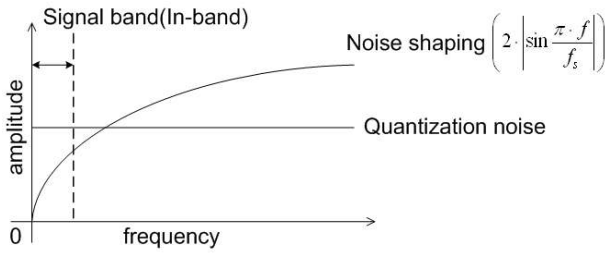


Fig. 3. Frequency characteristics of the SDM.

where m is the modulation index. Unlike the DC input, the magnitude of AC sinusoidal inputs varies in $m\sin(\omega t)$, and thus the equation for the switching frequency ratio is the mean value of $m\sin(\omega t)$. This value can be given as follows:

$$R=\frac{1}{2}-\frac{1}{2}\left(\frac{1}{\pi}\int_0^{\pi} m\sin(\omega t)d\omega t\right)=\frac{1}{2}-\frac{1}{\pi}m \tag{9}$$

Fig. 4 shows the relationship between R and m. As the modulation index increases, the switching frequency ratio decreases, and this results an increase in the number of samplings per cycle of the output pulse.

In order to investigate the variation in the output switching periods, we introduce the sampling number per switching cycle. From Equation (8), we obtain the most probable value of the sampling number n_s as follows:

$$\tilde{n}_s=\left\langle\frac{2}{1-|x|}\right\rangle \tag{10}$$

where $\tilde{n}_s$ denotes the most probable value of n_s, $\langle a\rangle$ represents the nearest integer to a, and x is the input at the starting instant of the switching cycle. The mean of n_s is theoretically equal to $1/R$. Fig. 5 shows the waveform where the sampling numbers are 2 and 3. When the magnitude of the input signal is 0, the value of n_s is equal to 2. As the magnitude of the input signal becomes larger, the value of n_s grows and thus the period of the switching pulse becomes longer. Since the control performance of

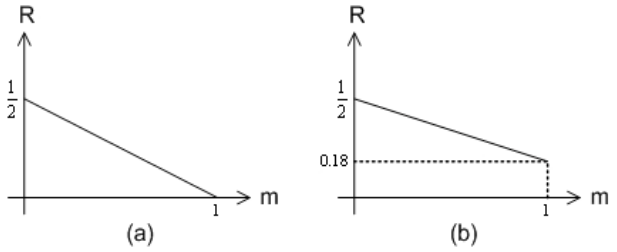


Fig. 4. Relationship between the switching frequency ratio and the modulation index in SDM for (a) DC inputs, (b) AC inputs.

the modulator deteriorates with a decrease in the switching frequency, a value of $\bar{n}_s$ above 10 is not desirable. In other words, in case of DC inputs, a modulation index below 0.8 is the most efficacious.

3. Proposed CDSDM (Combined DSDM) Scheme

The main strategy of DSDM is to apply a random dither somewhere in the SDM to produce perturbations that reduce the problems, while maintaining the required average properties - the switching frequency and the duty ratio - of the modulator. To reduce the harmonic spikes in the SDM, the DSDM method has various structures for determining the additional random dither generator; these methods can be classified into Space-Dithered SDM and Time-Dithered SDM in consideration of the location of the random dither additions.

3.1 Space-Dithered SDM

Fig. 6 shows the block diagram of the SDSDM where x denotes the input value, y denotes the two-leveled modulated output, d_s denotes the value of the space-dither and K_s denotes the magnitude adjustment parameter for the space-dither. In this scheme, the space-dither has a random magnitude and behaves like noise. The SDSDM can easily be implemented in a microprocessor and can be operated under a constant sampling frequency. However, there remains a problem with the signal-to-noise ratio (SNR). Too much power in the space-dither will cause the SNR of the output pulse to deteriorate. The parameter K_s is employed to control this and the degree of scattering can be adjusted accordingly. The SDSDM makes the

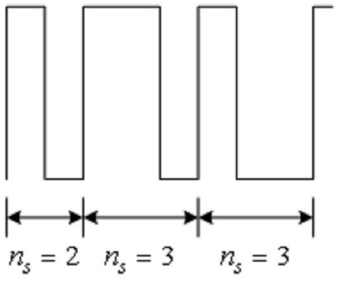


Fig. 5. Sampling numbers for the output pulse pattern of SDM.

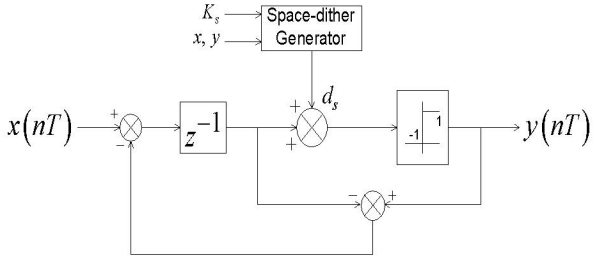


Fig. 6. Block diagram of SDSDM.

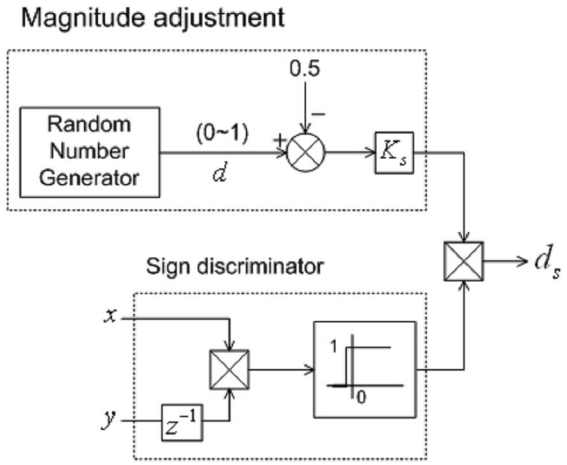


Fig. 7. Schematic of the space-dither generator.

switching in the broad frequency bandwidth, so some harmonic spikes in the SDM are redistributed.

Fig. 7 shows the schematics of a space-dither generator, that comprises a magnitude adjustment section and a sign discriminator. A random number between 0 and 1 is generated at every sampling instance, and subtracting 0.5 removes its bias. When the signs of the input and output are different from each other for large values of x, the dither should not be applied. This is to prevent excessive reduction of the switching frequency.

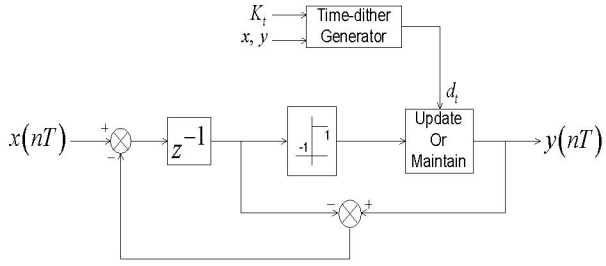


Fig. 8. Block diagram of the TDSDM.

3.2 Time-Dithered SDM

Fig. 8 shows the configuration of another method, that utilizes the random dither in time; here, a random dither is used as a control signal to make the update-or-maintain changes to its state and thus to decide the switching instants. This method is called the "Time-Dithered SDM" and the parameter K_t controls the distribution of the value of time-dither d_t.

Unlike the SDSDM, the output of the time-dither is a binary signal, that is, either 0 or 1. On one hand, when it is 0, the update-or-maintain block is in the "update" state and the TDSDM behaves like a SDM. On the other hand, when the value of the time-dither is 1, the update-or-maintain block is changed to the "maintain" state, and the output value of the Time-Dithered SDM remains unchanged. In consequence, the switching instants of Time-Dithered SDM are displaced in a random manner according to the time-dithered outputs.

Like the SDSDM, the TDSDM algorithm can also be implemented easily in a microprocessor, and can be operated under a constant sampling frequency. It should be noted that too many 1's in the value of the time-dither will cause the SNR of the output pulses to deteriorate, and the parameter K_t is employed to manage this so that the degree of scattering can be adjusted.

The time-dither generator shown in Fig. 9 is divided into a distribution adjustment section and a sign discriminator. First, a random sequence of numbers between 0 and 1 is produced as it did in the space-dither generator. Second, this is changed into a binary signal while K_t controls the probability for the occurrence of the 1's. Finally, the sign discriminator decides the period during which the binary signal is to be passed to the dither output. Increasing the value of K_t increases the probability of 1 occurring in the dither output and thus, increases the

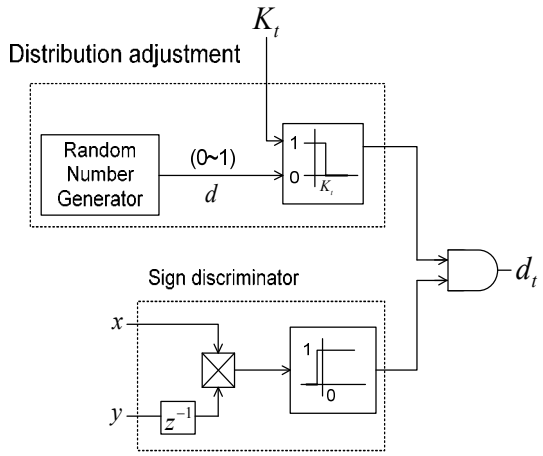


Fig. 9. Schematic of the time-dither generator.

value of n_s. As a result, the harmonic spikes are weakened, but the low-frequency spectrum grows as K_t approaches 1.

3.3 The Standard Deviation of the Sampling Number

In order to verify the degree of the harmonic-spreading, the standard deviation of n_s is used. The standard deviation σ is expressed as

$$\sigma = \sqrt{\frac{1}{N-1}\sum\left(n_s - \bar{n}_s\right)^2} \tag{11}$$

where N is the number of output pulses during several periods of the input signal and $\bar{n}_s$ is the mean of n_s. The variation of n_s directly affects the switching pattern of the output pulses. As the magnitude of the space-dither increases and the probability of 1 occurring at the time-dither increases, the value of n_s varies to a larger extent. This causes the standard deviation σ to increase accordingly and the harmonic spikes to migrate.

3.4 Proposed CDSDM

Fig. 10 shows the standard deviation of n_s vs. the modulation index. In the SDM scheme, σ is generally below 0.5, which means that n_s becomes one of the two adjacent integers. The SDSDM scheme makes σ increase gradually with the increase of m, and results in good performances throughout the whole range. In the

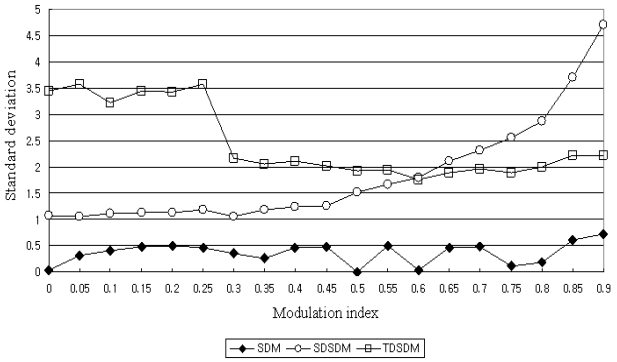


Fig. 10. Standard deviation of n_s vs. m for the SDM, SDSDM, and TDSDM methods.

TDSDM method, an increase in σ does not follow that of m, that is, there is no accommodation for a large $\bar{n}_s$.

The SDSDM and TDSDM methods reduce the harmonic spikes caused by the PWM. However, the two methods have a different performance according to the modulation index. The standard deviation of the sampling number represents the performance difference between the SDSDM and TDSDM.

If the modulation index is lower than 0.6, the SDSDM scheme gives outputs that are higher than those from the TDSDM method. If the modulation index is higher than 0.6, TDSDM gives higher values than the SDSDM. This means that the SDSDM has better performances in modulation indices lower than 0.6 and the TDSDM has better performances in modulation indices higher than 0.6. The modulation index varies within the output voltage, and hence the scheme chosen to be implemented varies as the modulation index goes from lower to higher than 0.6 and vice versa. The SDSDM scheme is applied in modulation indices lower than 0.6 and the TDSDM scheme is applied in modulation indices higher than 0.6 (see Fig. 11).

To achieve an effective reduction of harmonic spikes, the proposed CDSDM applied the SDSDM and TDSDM based on the modulation index of 0.6. The SDSDM was applied in the modulation index lower than 0.6 and the TDSDM was applied in the modulation index higher than 0.6. This means that only one method was chosen according to the modulation index (not at the same). There is no need to use an additional hardware to apply the proposed algorithm.

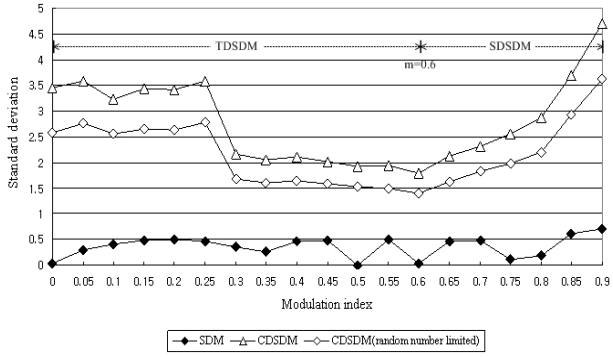


Fig. 11. Standard deviation of n_s vs. m for the SDM, CDSDM and CDSDM(random number limited) schemes.

4. Inductor Current and Switching loss

4.1 Peak Inductor Current

The maximum and minimum values of inductor current can be determined as

$$I_{\max} = I_o + V_i \cdot \frac{D(1-D)}{2L} \cdot T$$
$$I_{\min} = I_o - V_i \cdot \frac{D(1-D)}{2L} \cdot T \quad (12)$$

where I_o, V_i, D, and T denote the output current, the input voltage, the duty ratio, and the switching period respectively. The PWM method has a fixed switching frequency so that the inductor current doesn't vary at every switching instant. However, the proposed method has a variable switching frequency at every switching instant with a random dither.

The inductor current of the proposed method can have a variable maximum and minimum value under the variation of T. The sampling number in Section 2.3 determined the switching period of the proposed method. Being proportionate to T, the maximum value of inductor current can be estimated by the sampling number.

The distribution of sampling number and switching state of SDM are shown in Fig. 12. Fig. 13 and Fig. 14 show that the same contents for 0.2 and 0.7 of modulation index about the CDSDM, respectively. The sampling numbers of SDM are 2 and 3. With the random dither generator, the CDSDM has larger sampling numbers than the SDM. This means that the peak inductor current of the

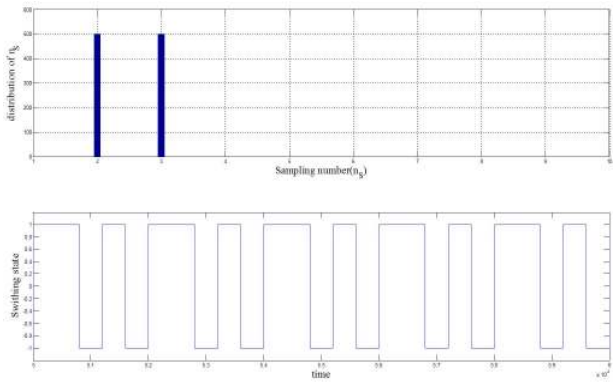
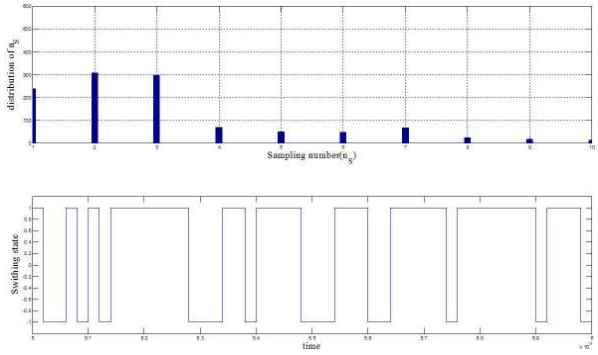
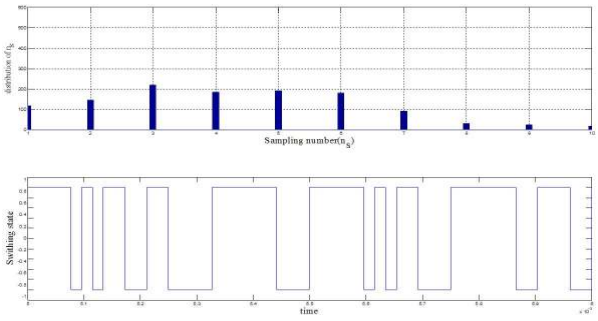


Fig. 12. The Distribution of ns and switching state for m=0.2 of SDM.



(a)



(b)

Fig. 13. The Distribution of ns and switching state for m=0.2 (a) of SDSDM (b) of TDSDM.

CDSDM is larger than that of the SDM.

In the proposed method, a random characteristic makes a random switching frequency so that it causes an increase in the peak inductor current. To reduce the harmonic spikes and the peak inductor current, the maximum period where random numbers are distributed should be limited to 90%.

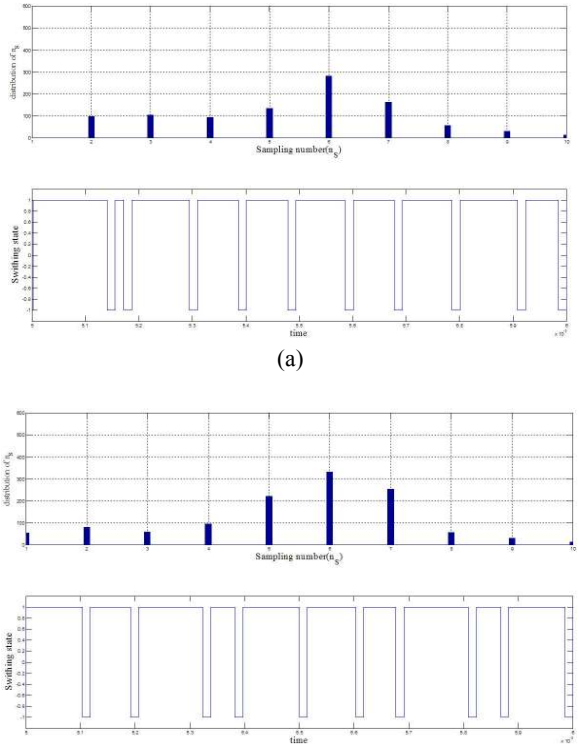


Fig. 14. The Distribution of ns and switching state for m=0.7 (a) of SDSDM (b) of TDSDM.

4.2 Switching loss

The switching device has losses that affect its temperature and switching efficiency. The switching operation includes four behaviors: turn-on time (T_1), on-state time (T_2), turn-off time (T_3) and off-state time (T_4). The total time of the four behaviors is equal to the switching period, and in turn, it is equal to $1/f_{sw}$ where f_{sw} is the switching frequency.

The instant voltage, or the current of the four intervals of the switching operation, can be seen as Fig. 15. During stage T_1, the instantaneous voltage across the switch is V_1, and the instantaneous current is I_1. The average power P_1 is obtained by the product of V_1 and I_1. The energy dissipated during this stage is $P_1 \cdot T_1$.

$$L_{sw} = P_1 T_1 f_{sw} + V_T I_T D + P_3 T_3 f_{sw} \quad (13)$$

In equation (13), the switching loss is determined. The switching loss of the PWM and proposed CDSDM method can be compared by the switching frequency. On average,

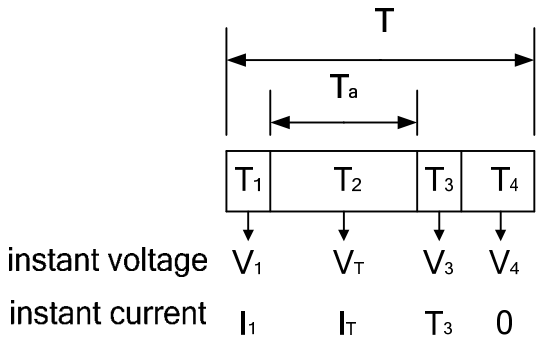


Fig. 15. Four stages of a switching operation.

the proposed method has the same switching frequency as the PWM. The switching loss of the both method is almost the same.

5. Experimental Results

Experiments have been performed to confirm the performance improvement of a buck converter by applying the proposed CDSDM scheme. The DC input voltage of the converter is 50[V], the rated power is 100[W] and the sampling frequency is 25[kHz]. Fig. 16 shows the schematic of a Buck converter using the CDSDM. Fig. 17 shows the Experimental FFT waveforms of the switching signal using the SPWM and SDM schemes. Fig. 18 and 19 show the Experimental FFT waveforms of the switching signals for modulation indexes 0.2 and 0.7.

The proposed CDSDM has different performance on the base of modulation index 0.6. The difference between the two methods is shown in the experimental result. In Fig 17, the differential performance at the modulation index of lower than 0.6 is shown. In Fig. 18, the differential performance at modulation index higher than 0.6 is shown.

The harmonic spikes in the conventional SPWM are concentrated at the switching frequency and its multiple frequencies, but the harmonic spikes in the SDM are reduced to some extent. The harmonic spikes in the SDSDM and TDSDM are spread on a broad frequency bandwidth.

For modulation index value of 0.2, the harmonic spikes obtained by using the SDSDM are more spread than those obtained by the TDSDM method. For modulation

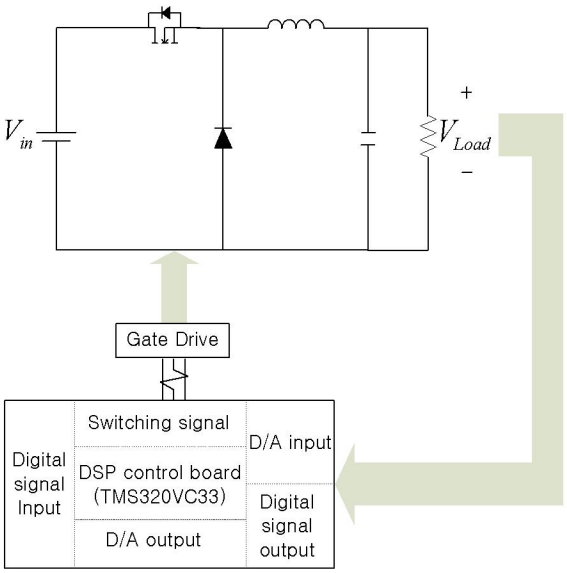


Fig. 16. Schematic of a Buck converter using the CDSDM scheme.

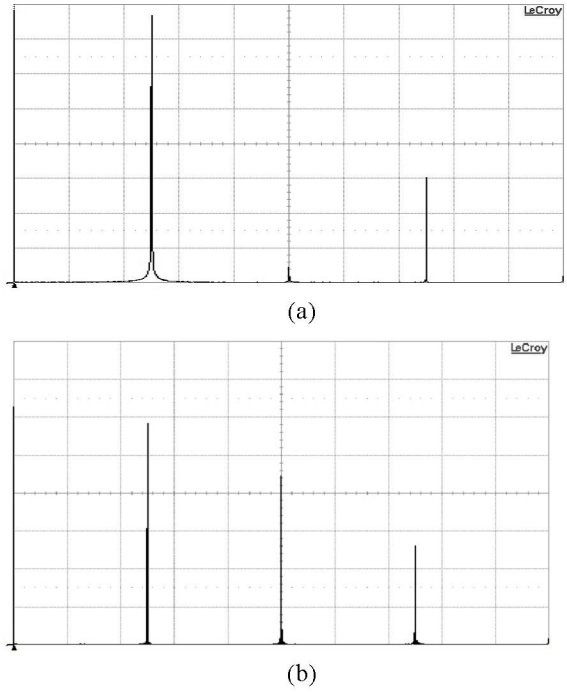


Fig. 17. Experimental FFT waveforms of the switching signal using (a) the SPWM and (b) SDM schemes (x-axis: 2[kHz /div], y-axis: 1[V/div]).

index value of 0.7, the harmonic spikes for the TDSDM are more spread than the SDSDM scheme. The modulation index varies with the output voltage, and the scheme adopted is changed when the modulation index increases from below 0.6 to above it and vice versa. Fig. 20 shows the changes in the modulation index with the variation of the output voltage, and Fig. 21 shows how the output voltage and error vary when the input voltage is fixed at 50[V] and the reference voltage is changed to the following values from 40[V] to 30[V], from 30[V] to 20[V], and again back to 30[V]. The output voltage is seen to track the reference voltage with respect to the changes in the reference voltage.

The random characteristic in the CDSDM causes the increase in a current ripple in the inductor. To complement the increase in a current ripple, the maximum period where random numbers are distributed should be limited to 90%. In Fig. 22, current ripples using the SPWM, TDSDM, and SDSDM are shown. The current ripple using the TDSDM is measured at modulation index 0.3 and the current ripple using the SDSDM is measured at modulation index 0.7, and the output voltage using the SPWM, TDSDM, and SDSDM is 35[V], 15[V], and 35[V], respectively. The rms value for the AC component

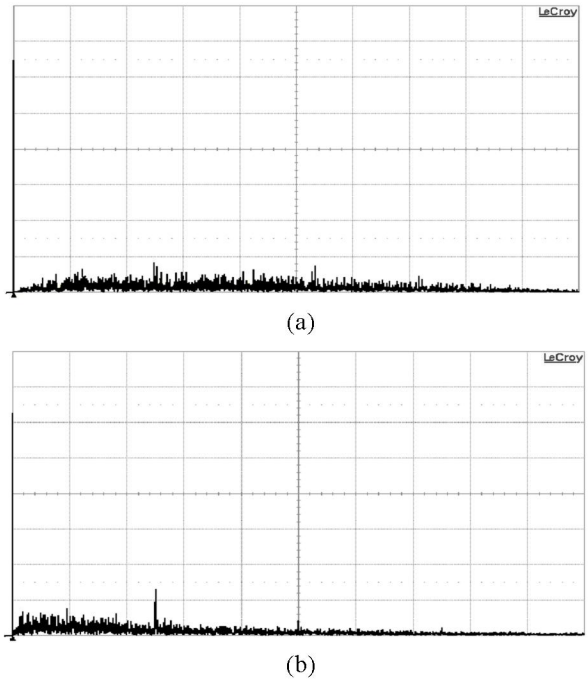
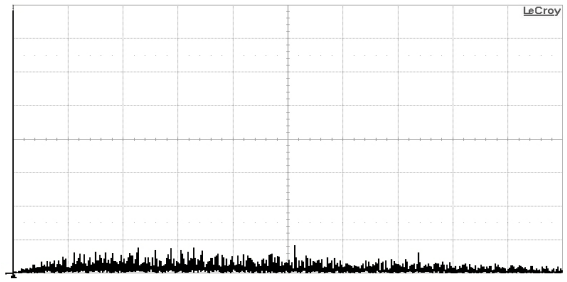
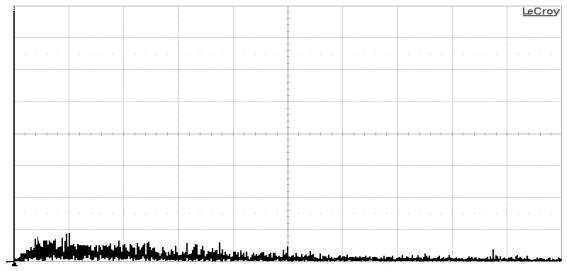


Fig. 18. Experimental FFT waveforms of the switching signal for a modulation index value of 0.2 using (a) the SDSDM and (b) the TDSDM (x-axis: 2[kHz /div], y-axis: 1[V/div]).



(a)



(b)

Fig. 19. Experimental FFT waveforms of the switching signal for a modulation index value of 0.7 using (a) the SDSDM and (b) TDSDM (x-axis: 2[kHz /div], y-axis: 1[V/div]).

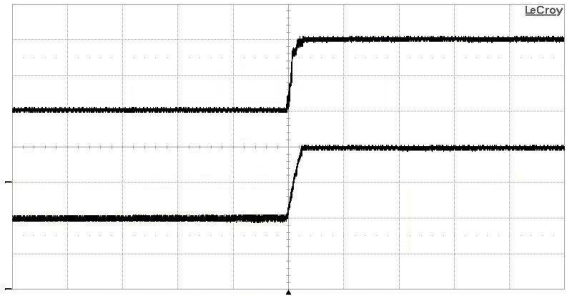


Fig. 20. Output voltage (upper) and modulation index (lower) changes (x-axis: 10[ms/div], y-axis: 10[V/div]).

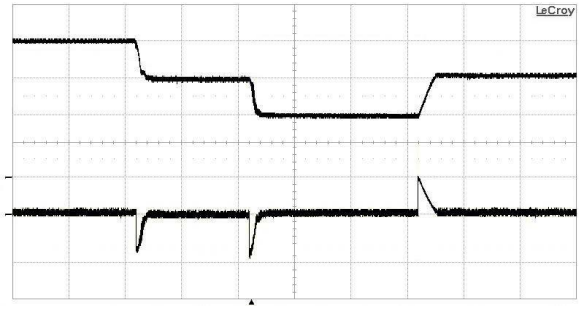
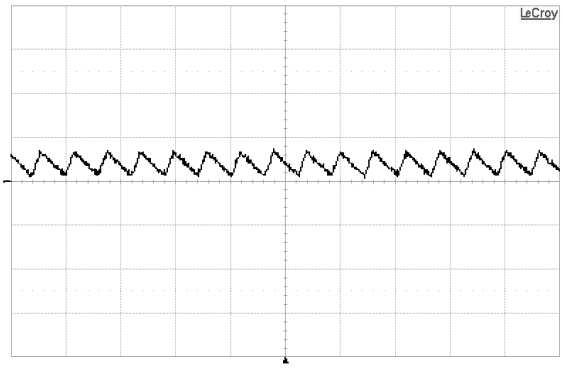
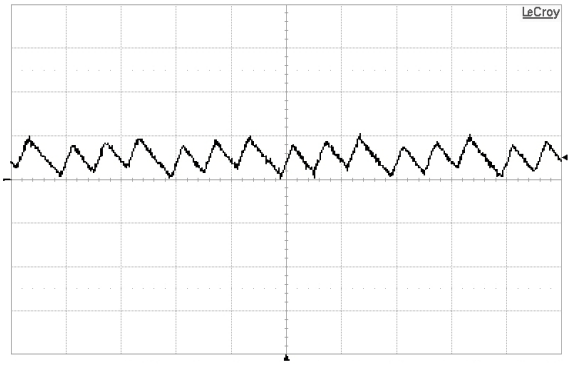


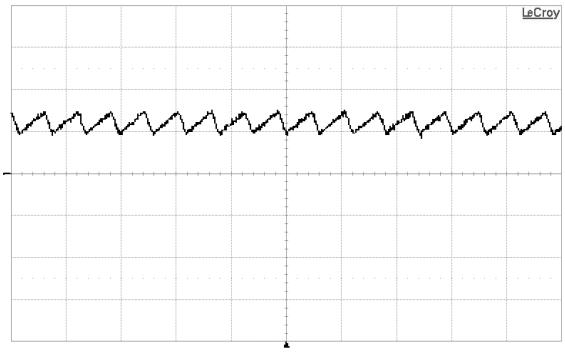
Fig. 21. V_{ref} change in the buck converter with using the CDSDM scheme (x-axis: 10[ms/div], y-axis: 10[V/div]).



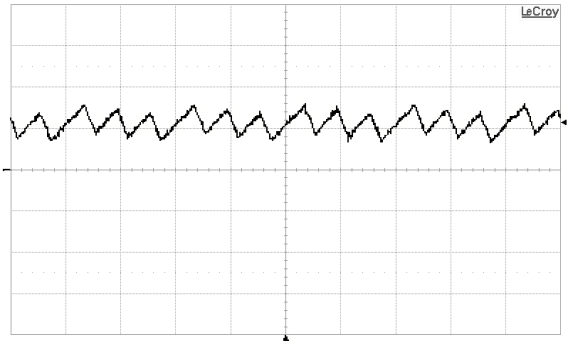
(a) SPWM (duty ratio = 0.3)



(b) TDSDM (m=0.3)



(c) SPWM (duty ratio = 0.7)



(d) SDSDM (m=0.7)

Fig. 22. Comparison of inductor current applied by the SPWM and CDSDM (x-axis: 500[μs /div], y-axis: 1[A/div]).

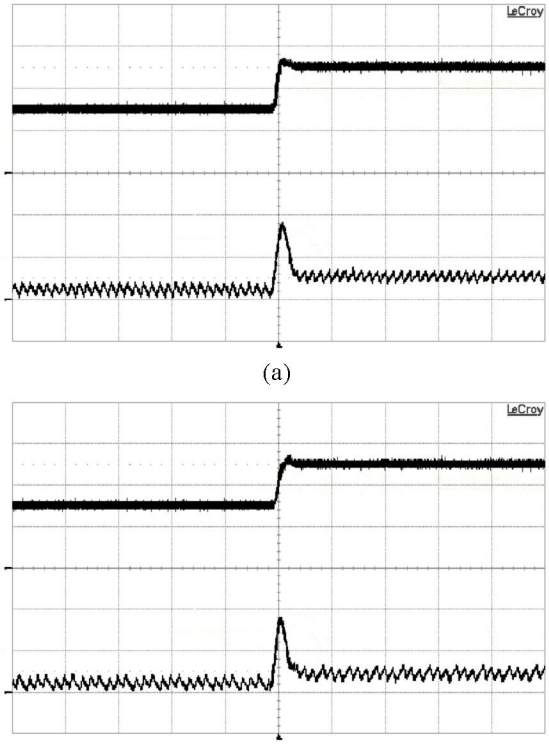


Fig. 23. Variation of inductor current with output voltage using (a) the SPWM and (b) the CDSDM (x-axis: 2[ms/div], y-axis: 20[V/div](upper), 2.5[A/div](lower)).

of current is measured for 200[mA] using the SPWM scheme, 217[mA] using the TDSDM, and 211[mA] using the SDSDM. Despite the increase of the standard deviation, it is observed that the current ripple using the TDSDM and SDSDM is almost same as the conventional SPWM scheme. As the output voltage varies from 15[V] to 35[V], the inductor current is shown in Fig. 23. The CDSDM has a correct transient response, and it is observed that the current ripple doesn't increase on the whole compared to the SPWM.

6. Conclusions

The CDSDM scheme was proposed for improving the performance of a PWM converter in this paper. In order to reduce the harmonic spikes, the SDM, SDSDM and TDSDM schemes were explained and the degree of the harmonic-spreading for the CDSDM was quantitatively confirmed by investigating the standard deviation of the sampling number per switching cycle. Experimental FFT analyses were also presented, and thus verified that the proposed CDSDM scheme had a much better performance than the SPWM, SDM, SDSDM, and TDSDM methods.

Acknowledgment

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