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A New Soft Switching Step-Down/Up Converter with Inherent PFC Performance

Masoud Jabbari[†] and Hosein Farzanehfard[*]

[†*]Dept. of Electrical and Computer Eng., Isfahan University of Technology (IUT), Isfahan, Iran

ABSTRACT

In this paper a new buck-boost type DC-DC converter is presented. Its voltage gain is positive, all active elements operate under soft-switching condition independent of loading, magnetic isolation and self output short-circuit protection exist, and very fast dynamic operation is achievable by a simple bang-bang controller. This converter also exhibits appropriate PFC characteristics since its input current is inherently proportional to the source voltage. When the voltage source is off-line, it is sufficient to add an inductor after the rectifier, then near unity power factor is achievable. All essential guidelines to design the converter as a DC-DC and a PFC regulator are presented. Simulation and experimental results verify the developed theoretical analysis.

Keywords: DC-DC converter, PFC, Resonant converters, Soft switching

1. Introduction

Soft switching techniques are mainly developed to reduce switching losses. Under soft switching condition, switching frequency can be increased and thereby converter size can be reduced as well. These converters are often obtained by modifying hard switching topologies or sometimes by presenting novel circuits. Soft switching condition is commonly attained by switching under zero voltage (ZV) or zero current (ZC) condition[1-3].

PFC converters are presented to reduce line current harmonics and are classified as single-stage and two-stage topologies [4-6]. Single-stage topologies are more economical for low power applications[4-9]. Two-stage topologies are formed by a PFC preregulator which is followed by a DC-DC converter. The preregulator which is often a boost converter, enhances the input power factor and the second stage provides tight output voltage regulation with a fast dynamic response. However, number of elements is increased, efficiency is decreased, and two control loops are required. Among various presented topologies, only a few are soft switched[7-13]. To have a universal voltage gain or to decrease power processing, PFC (pre-) regulators based on buck-boost, SEPIC and Cuk converter are also developed[14-24].

A new soft-switching step down/up converter is presented in this paper. The converter is resonant type, has a positive voltage gain, and exhibits inherent PFC characteristics. Its topology is derived from our previous work, switch-resonator converters[25]. For DC-DC purposes, the proposed converter can be attractive as a soft-switched alternative for SEPIC or Cuk converter.

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[†]Corresponding Author: Jabbari.Masoud@Gmail.com
Tel: +98-913-314-8874, Isfahan Univ. of Tech.
[*]Dept. of Electrical and Computer Eng., Isfahan Univ. of Tech.

Similar to SEPIC, magnetic isolation also exists. Furthermore, a bang-bang controller can be employed easily and thereby a much faster dynamic response can be attained with respect to the common PWM-based controllers. For PFC applications, since the converter input current is inherently proportional to the source voltage, it is sufficient to place an inductor after the input full-bridge rectifier to obtain a near unity power factor.

This paper pays special attention to achieve the highest input power factor along with minimizing the input filter size of the proposed converter. All required design guidelines are prepared based on mathematical relations. The presented simulation and experimental results verify the theoretical analysis.

2. Proposed DC-DC Converter

Consider the proposed circuit presented in Fig. 1 where all switches are unidirectional, and Q_2 and Q_r are gated simultaneously as shown by the dashed-line. Also the resonance capacitor C_r provides magnetic isolation between the load and source. To simplify the analysis, assume that all the circuit elements are ideal and the output capacitor is large enough so that the output voltage is almost constant. The equivalent circuit of each operating mode and important waveforms are shown in Fig. 2 and Fig. 3 respectively. Following relations are defined for the circuit of Fig. 1:

$$\omega_r = 1/\sqrt{L_r \cdot C_r}\ , \quad f_r = T_r^{-1} = \omega_r/(2\pi) \tag{1}$$

$$Z_r = \sqrt{L_r/C_r} \tag{2}$$

$$r = R/Z_r \tag{3}$$

$$\mu = C/(2C_r) \tag{4}$$

Assume that prior to Mode I, the resonance current i_r is zero, the resonance voltage v_r is $-V_O$, and all switches are off. The circuit operates in four modes as follows:

Mode I ($t_1 - t_2$): At t_1, Q_1 is turned on at ZC and C_r is charged through a resonance with L_r. At t_2, i_r reaches zero and Q_1 is turned off at ZC consequently. At this time v_r has reached $2V_S+V_O$.

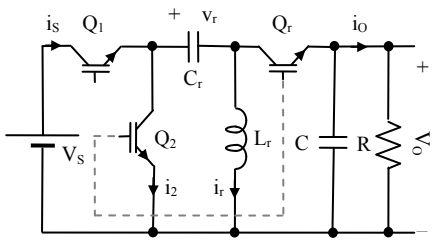

Fig. 1. Proposed converter topology.

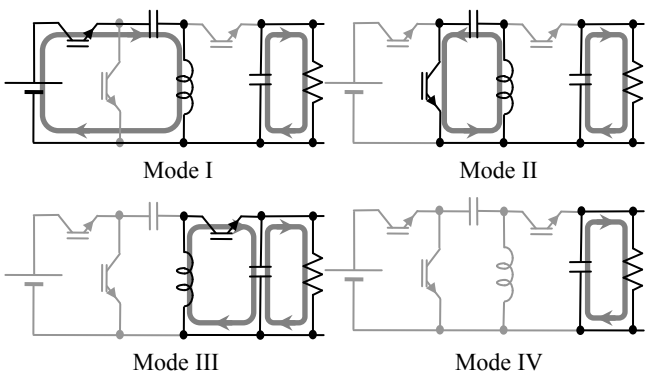

Fig. 2. Equivalent circuit of each operating mode.

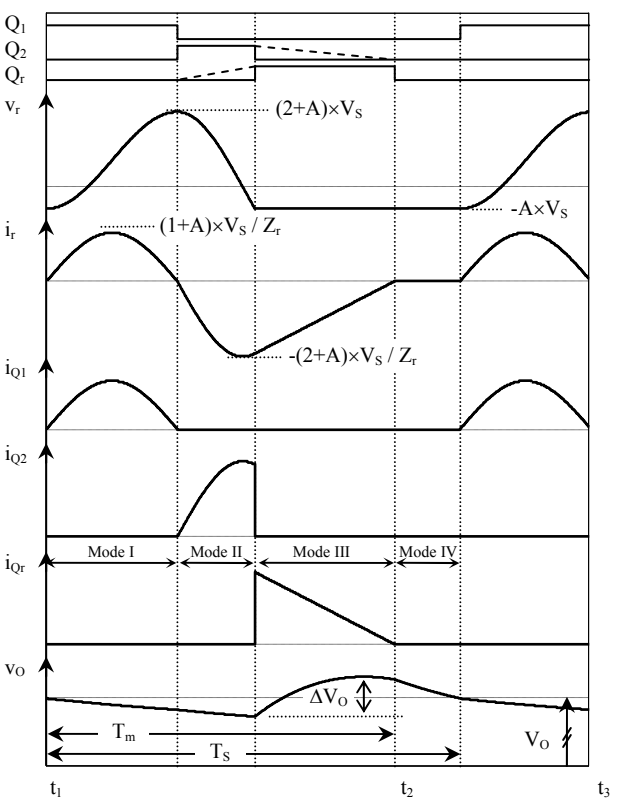

Fig. 3. Steady-state key waveforms.

$$v_r(t) = V_S - (V_S + V_O)\cos(\omega_r \cdot (t - t_1)) \quad (5)$$

$$Z_r \times i_r(t) = (V_S + V_O)\sin(\omega_r \cdot (t - t_1)) \quad (6)$$

$$t_2 - t_1 = T_r/2 \quad (7)$$

Mode II ($t_2 - t_3$): At t_2, Q_2 is turned on at ZC and a resonance starts between L_r and C_r. The resonance current is sinusoidal and the resonance voltage reduces to zero and goes negative until it reaches $-V_O$. Q_r should be gated during this mode (or simultaneously with Q_2), but it does not conduct since its collector-emitter voltage is negative. Thus, Q_r turn on is at zero-voltage zero-current condition.

$$v_r(t) = (2V_S + V_O)\cos(\omega_r \cdot (t - t_2)) \quad (8)$$

$$Z_r \times i_r(t) = -(2V_S + V_O)\sin(\omega_r (t - t_2)) \quad (9)$$

$$t_3 - t_2 = \frac{1}{\omega_r}\left[\pi - \cos^{-1}\frac{V_O}{2V_S + V_O}\right] \quad (10)$$

$$Z_r \times i_r(t_3) = -2\sqrt{V_S(V_S + V_O)} \quad (11)$$

Mode III ($t_3 - t_4$): When v_r reaches $-V_O$, collector-emitter voltage of Q_r becomes positive and thus it starts conducting. Since C is much larger than C_r, the current of L_r is diverted to Q_r, and Q_2 current becomes zero. During this mode the energy stored in L_r is delivered to the load and Q_2 can be turned off at ZC. The magnitude of i_r decreases linearly until at t_4 it reaches zero. At this time Q_r turns off at ZC. The entire energy absorbed by C_r in Mode I is now delivered to the load.

$$i_r(t) = i_r(t_3) + V_O/L_r \times (t - t_3) \quad (12)$$

$$v_r(t) = -V_O \quad (13)$$

$$t_4 - t_3 = \frac{2}{\omega_r} \cdot \frac{\sqrt{V_S(V_S + V_O)}}{V_O} \quad (14)$$

Mode IV ($t_4 - t_5$): In this mode, all switches are off and the load is supplied by the output capacitor. Duration of this interval is determined by the controller so that proper voltage gain is attained (dead-time control).

3. Transient and Steady-State Equations

The converter dynamic operation can be represented using difference equations in discrete time-domain. Within the n*th* and (n+1)*th* switching cycle, the converter input energy is $\varepsilon_{in}(n)$ and the energy consumed by the load is $\varepsilon_{out}(n)$ as (15) and (16) where $T_S = f_S^{-1}$ is the switching period. Also, the output capacitor energy variation in this interval, $\Delta\varepsilon_C(n)$, is as (17).

$$\varepsilon_{in}(n) = \int_{t1}^{t2} V_S\, i_r\, dt = 2C_r V_S^2 + 2C_r V_S V_O(n) \quad (15)$$

$$\varepsilon_{out}(n) = \int_{TS} \frac{v_O^2}{R}\, dt \cong \frac{V_O^2(n) + V_O^2(n+1)}{2R f_S} \quad (16)$$

$$\Delta\varepsilon_C(n) = \varepsilon_{in} - \varepsilon_{out} = \frac{1}{2}CV_O^2(n+1) - \frac{1}{2}CV_O^2(n) \quad (17)$$

Instantaneous average voltage gain a(n) and parameter S are defined as follows:

$$a(n) = V_O(n)/V_S(n) \quad (18)$$

$$S = 2RC_r f_S = \frac{r}{\pi} \cdot \frac{f_S}{f_r} \quad (19)$$

By using (15)-(19), the converter dynamic equation is attained as (20).

$$(1 + \mu S)a^2(n+1) + (1 - \mu S)a^2(n) = 2S[1 + a(n)] \quad (20)$$

By substituting A=a(n)=a(n+1) in (20), voltage gain at steady-state, A, is attained as (21). Also it can be proven that the peak-to-peak output voltage ripple ΔV_O is approximately given by (22).

$$S = A^2/(1 + A) \quad (21)$$

$$\Delta V_O/V_O \cong \left[\sqrt{1 + A}/A - 1/2r\right]^2/\mu \quad (22)$$

4. Maximum Power Delivery Condition

In absence of dead-time, the converter operates at its maximum power handling capability where the switching frequency is also at maximum. This state is named Maximum Power Delivery Condition. Subscript 'm' is used to denote the quantities at this condition. The interval from t_1 to t_4 is defined as T_m. By using (7), (10) and (14)

the following relation is obtained.

$$\frac{T_m}{T_r}=1+\frac{1}{2\pi}\left[\frac{2\sqrt{1+A}}{A}-\cos^{-1}\frac{A}{2+A}\right] \tag{23}$$

By substituting $f_S=T_m^{-1}$ in (19), (24) is attained. This equation is required for converter design. For example, for $R=Z_r/2$ ($r=0.5$), A_m is obtained equal to 0.338 which shows maximum attainable voltage gain in this case. Lower voltage gain can be achieved by adjusting switching frequency (inserting dead time).

$$r=\frac{A_m^2}{1+A_m}\cdot\left[\pi+\frac{\sqrt{1+A_m}}{A_m}-\frac{1}{2}\cos^{-1}\frac{A_m}{2+A_m}\right] \tag{24}$$

According to (23), T_m is infinite for output short-circuited ($A=0$). Thus power transferring is automatically stopped at output short-circuited (self short-circuit protection).

5. General Equations and Modeling

In this section, the proposed converter is analyzed at steady state when the source voltage is alternative and positive (e.g. rectified AC voltage). The voltage source period is defined as T_0, and averaging operator $\langle x\rangle$ is defined as below:

$$\langle x\rangle_T=\frac{1}{T}\int_T x\cdot dt \tag{25}$$

Equation (20) still describes the converter dynamic operation. By applying averaging operator on both sides of this equation, and assuming that the switching frequency is at least two times greater than the maximum frequency of the source voltage spectrum (Nyquist rate), (26) is obtained. This equation is the general form of (21).

$$S=\left\langle v_O^2\right\rangle_{T_0}\Big/\left[\langle v_O\cdot v_S\rangle_{T_0}+\left\langle v_S^2\right\rangle_{T_0}\right] \tag{26}$$

This equation is still unusable since the cross term $\langle v_O\cdot v_S\rangle$ cannot be calculated directly. Let's assume $\langle v_O\cdot v_S\rangle\cong V_O\cdot\langle v_S\rangle$ because it is desired to have a constant DC output voltage, then:

$$S\cong V_O^2\Big/\left[V_O\cdot\langle v_S\rangle_{T_0}+\left\langle v_S^2\right\rangle_{T_0}\right] \tag{27}$$

According to (6), the amplitude of source current during t_1 to t_2 is $(v_S+V_O)/Z_r$ and is zero during the rest of switching period. Thus, the source current during its non-zero interval contains two terms; the first term is proportional to v_S (inherent PFC characteristic) but the second term is independent from v_S. Therefore, the converter input behavior can be modeled as a resistor R_f in parallel with an independent DC current source I_{DC} which is described by (28). In view of this model, the total energy absorbed by the converter is as (29). By applying (27), R_f is obtained as (30).

$$I_{DC}=\left\langle i_r\big|_{v_S=0}\right\rangle_{TS}=\frac{V_O}{Z_r}\cdot\frac{1}{\pi}\frac{T_r}{T_S}=\frac{V_O}{R/S} \tag{28}$$

$$\sum_{T_0}\varepsilon_{in}(n)=\frac{\left\langle v_S^2\right\rangle_{T_0}}{R_f}T_0+\langle v_S\rangle_{T_0}I_{DC}T_0 \tag{29}$$

$$R_f=R/S=1/(2C_rf_S) \tag{30}$$

6. PFC Circuit

Generally the input source of power supplies is off-line. Since most of the existing converters are DC-DC, a (full-bridge) rectifier followed by a filtering capacitor is usually used to prepare the required input DC voltage. In order to have an acceptable DC voltage, capacity of the filter is relatively high since the line frequency is low 50/60Hz. But, on the other hand, a large capacitor leads to a low input power factor. There is a tradeoff between the power factor and the ripple of the produced DC voltage.

The proposed topology has two features; it is a buck-boost converter and its input current is a sinusoidal pulse whose amplitude is proportional to the input voltage. Thus, a much smaller filtering capacitor can be chosen since the converter is able to compensate a higher input voltage ripple. But, by decreasing the size of filter

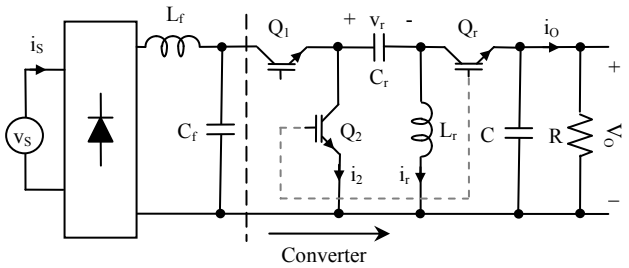

Fig. 4. Proposed PFC converter.

capacitor, the high-frequency harmonics created due to switching operation appear in the source current. Consequently, an inductor should be placed between the rectifier and the filtering capacitor. In other words, the previous large filtering capacitor is now replaced with a small capacitor and an inductor. Thereby, the input power factor is enhanced. This scenario, of course, is employed for other buck-boost type converters like SEPIC in discontinuous conduction mode [14-19]. But there are some improvements. Firstly, the proposed converter operates at soft-switching condition. Thus, switching losses are eliminated and the switching frequency can be increased. As a result, the employed LC filter becomes smaller. Secondly, the proposed converter input current waveform is a smooth sinusoidal pulse comparing to the sharp triangular current waveform of the conventional buck-boost type converters. Thus the produced switching harmonics are also smaller. Thirdly, in PWM controllers with the purpose of achieving current pulses proportional to the source voltage, complicated controllers are often employed[23-24]. The proposed converter has this feature inherently.

According to the aforementioned discussion, schematic of Fig. 4 is proposed where power factor is enhanced passively using a low-pass filter L_f and C_f. In fact, when the source is off-line, it is sufficient to place a small capacitor and an inductor after the rectifier and no additional control loop is required.

Consider the proposed system of Fig. 4 and assume that L_f and C_f do not exist. Thus the converter input voltage is a truly rectified sinusoidal. By defining $A_P=V_O/V_{S,peak}$, according to (27) the relation of A_P and S is obtained as (31). In the same manner used for obtaining (23), A_P at the maximum power delivery condition, A_{Pm}, is attained as (32).

$$S = \frac{A_P^2}{\frac{1}{2}+\frac{2}{\pi}A_P} \tag{31}$$

$$r = \frac{A_{Pm}^2}{\frac{1}{2}+\frac{2}{\pi}A_{Pm}} \cdot \left[\pi + \frac{\sqrt{1+A_{Pm}}}{A_{Pm}} - \frac{1}{2}\cos^{-1}\frac{A_{Pm}}{2+A_{Pm}}\right] \tag{32}$$

The equivalent circuit of the proposed PFC converter is shown in Fig. 5. In this figure, the diode D is used instead of the full-bridge rectifier, but the absolute value of the source voltage is applied. R_f and I_{DC} represent the converter averaging model, and i_h models the high-frequency harmonics of switching operation. After lengthy calculations, analytical relation of power factor is approximately obtained as (33) [26].

$$PF = \frac{\sqrt{2}\cdot\left[\frac{2}{\pi}\cdot\frac{A_P}{r_f}+\sum_{n=-\infty}^{\infty} g_n^2 f_n\right]}{\sqrt{\delta^2+\frac{A_P\left(A_P+4/\pi\right)}{r_f^2}+\sum_{n=-\infty}^{\infty}\left|g_n f_n\right|^2}} \tag{33}$$

$$g_n = \frac{2}{\pi}\frac{(-1)^{n+1}}{4n^2-1} \qquad f_n = \frac{1/r_f + j\,2n\lambda}{1-(2n\lambda)^2 + j\,\frac{2n\lambda}{r_f}} \tag{34}$$

$$\omega_f = \frac{1}{\sqrt{L_f\cdot C_f}} \qquad Z_f = \sqrt{L_f/C_f} \qquad r_f = R_f/Z_f \qquad \lambda = \omega_0/\omega_f \tag{35}$$

$$\delta^2 = \left(\frac{Z_f\,\omega_f}{2Z_r\omega_r}\right)^4\left(r_f - \frac{\pi Z_r}{2Z_f}\right)^2\left(1+\frac{8}{\pi}A_P+2A_P^2\right) \tag{36}$$

7. Control Scheme

One switching pattern includes gate signals which are used to commutate the switches. According to Fig. 3, to have a correct operation, the switching pattern is as follows. First Q_1 is turned on and remains on unless the

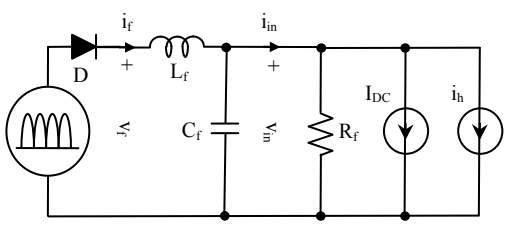

Fig. 5. Equivalent circuit of the PFC converter.

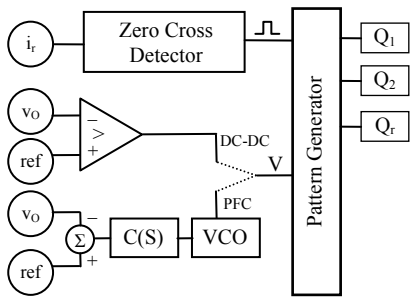

Fig. 6. Controller block diagram.

falling-edge of the resonance current crosses zero. Then it is turned off, and practically after a guard-time, Q_2 is turned on. By detecting the rising-edge zero crossing of the resonance current, Q_2 is turned off. The switch Q_r can be gated with Q_2 simultaneously. To realize this algorithm, pattern generator, it is sufficient to detect the zero crossing instances of the resonance current.

To regulate the output voltage, consider a control signal V so that while V=1 the pattern generator provides the required gate signals repetitively, and when V=0, after finishing the in progress cycle, the converter goes to the dead time mode. The block that provides the signal V is in fact the converter voltage controller.

For DC-DC purposes, the voltage controller is simply a voltage comparator as shown in Fig. 6 where the output voltage is directly compared with the reference voltage. During startup, V is continuously high since the output voltage is much lower than the reference voltage. Hence the controller does not insert dead-time within the switching pattern. Thus the converter operates at the maximum power delivery condition, and then the lowest settling time is achieved. When the output voltage reaches the reference voltage, V goes low and the switching operation is stopped immediately. Therefore, no voltage overshoot occurs. At steady-state, when the output voltage becomes lower than the reference voltage, one switching cycle is carried out which increases the output voltage to above the reference voltage. After that, the converter remains in dead-time until the output voltage becomes less than the reference voltage and the cycle repeats again. This control mechanism is a bang-bang controller and yields very fast dynamic performance.

For PFC applications, a simple bang-bang controller is unusable since the switching frequency should not have substantial variations with respect to the line voltage frequency. Otherwise, proper PFC performance is not attained. Thus the well-known VCO based controllers ought to be used as shown in Fig. 6.

8. Design Procedure

Consider a design with the following requirements.

- Source voltage: AC, 220±10% V_{RMS}, 50Hz
- Output voltage: DC, 25V
- Output power: maximum 100W, minimum 10W
- High frequency term of output voltage ripple < 0.2%
  Input power factor > 95% at 25W

Step I) determining Z_r:

$$A_{Pm} \geq \frac{Max\{V_O\}}{Min\{V_{S,peak}\}} = 89.3\times10^{-3} \xrightarrow{Eq.32} r \geq 0.201$$

$$Z_r \leq \frac{Min\{R\}}{0.201} = 31.1\Omega \xrightarrow{10\%\ overdesign} Z_r = 28.3\Omega$$

Step II) determining C/C_r: C is used to suppress the high-frequency term of output voltage ripple. According to (22), the high-frequency term of output voltage ripple is at its maximum, when r is at its maximum and A is at its minimum.

$$\left.\begin{aligned} A_{P,\min} &= \frac{Min\{V_O\}}{Max\{V_{S,peak}\}} = 0.073 \\ r_{\max} &= \frac{Max\{R\}}{Z_r} = 2.208 \end{aligned}\right\} \xrightarrow{Eq.22} \frac{C_H}{C_r} = 194500$$

Step III) Ascertaining resonance frequency: Equation (7) denotes that the on time duration of Q_1 is $T_r/2$. Thus, the resonance frequency should be ascertained considering the speed of employed switches. By applying $T_r/2=1\mu s$ in the above equations, $L_r=9\mu H$, $C_r=11.1nF$, and $C=2160\mu F$ are attained.

Step IV) Ascertaining Z_f and ω_f: Considering (33), power factor depends on seven parameters: A_P, r_f, ω_0, ω_f, ω_r, Z_f and Z_r. Among these parameters ω_0, ω_r and Z_r are known, A_P and r_f vary but their ranges are certain.

However, ω_f and Z_f are fixed but yet undetermined. Hence, a constrained optimization problem with one degree of freedom is produced. Encountering this problem is situational and depends on designer viewpoints. The concern of this paper is to achieve desired power factor analogous to a criterion, minimax [27], in which the minimum of power factor is wished to be maximum. In other words, 1-PF (one minus PF) should be minimized at the worst case (25W). This optimization is subjected to a constraint in which L_f is desired to be minimum too. By solving this problem, L_f=2.2mH, C_f=380nF are obtained.

9. Experimental Results

First consider the designed system as a DC-DC converter where only a very large capacitor is placed after the rectifier. Fig. 7 shows the soft-switching performance where for every switch, gate-emitter voltage, collector current and collector-emitter voltage are presented. These waveforms do not depend on the converter output power. The employed switches are IXRP15N120 and the control circuit is implemented by standard discrete HCMOS chips. Dynamic operation of the converter is shown in Fig. 8. The top waveform shows the output voltage at startup for 25W output power. As shown by this waveform, a very low settling time without voltage overshoot is attained. In most PWM converters, light load leads to voltage overshoot. The middle and bottom waveforms of Fig. 8 show the converter dynamic response to load variations. The middle waveform shows the converter output current where the load resistance is changed instantaneously from 30Ω (20W) to 6.3Ω (100W) and vice versa at 2.5KHz. Simultaneously the bottom waveform shows the output voltage ripple. Again no voltage overshoot/undershoot occurs. The converter efficiency is presented in Fig. 9. At full-load, the losses segregation is 11% for Q_1, 15% for Q_2, 65% for Q_r, and 9% for other losses. As a PFC converter, Fig. 10 shows simulation results of the source current at 80W output power. At this condition switching frequency is 68KHz and power factor is 99.7%. Experimental result of the converter source current is shown in Fig. 11. The theoretical (eq. (33)) and the attained experimental values of power factor are presented in Fig. 12. For load variations between 35W to 100W, the experimental results show an almost unity PF.

10. Conclusions

A new soft-switching step down/up converter with positive voltage gain is presented in this paper. The turn on and turn off transition of all switches are performed under soft switching conditions. Its soft-switching performance does not depend on loading. Furthermore, magnetic isolation and self output short-circuit protection exist, and very fast dynamic operation is achievable by a simple bang-bang controller. The presented converter is attractive for DC-DC purposes as SEPIC alternative. This converter also exhibits appropriate PFC characteristics

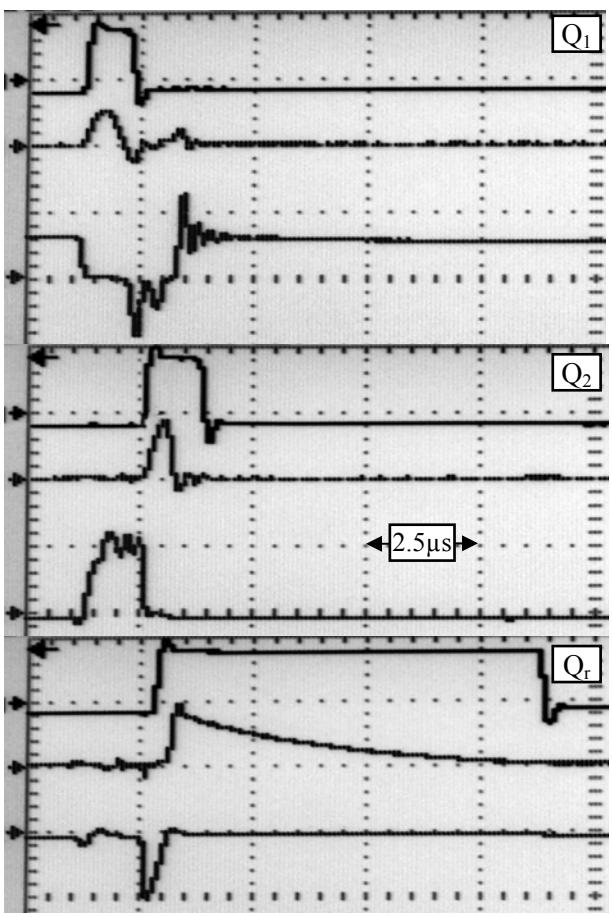

Fig. 7. Soft-switching performance for Q_1, Q_2, and Q_r (2.5µs/div). For each switch, waveforms of gate-emitter voltage (20V/div), collector current (20A/div), and collector-emitter voltage (500V/div) are shown respectively from the top.

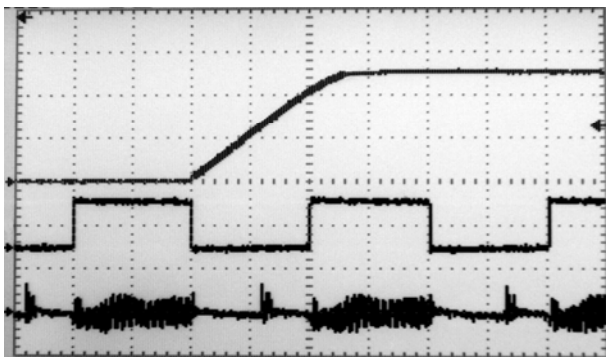

Fig. 8. Dynamic operation, respectively from top: output voltage at startup (5ms/div, 10V/div), output current (100μs/div), and output voltage ripple (1V/div).

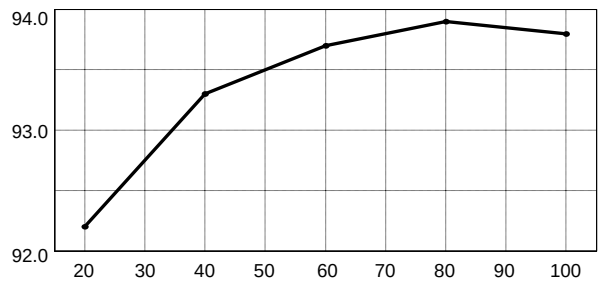

Fig. 9. Efficiency vs. output power.

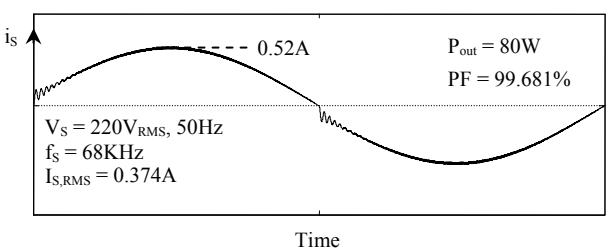

Fig. 10. Simulation results, source current at P_{out} = 80W.

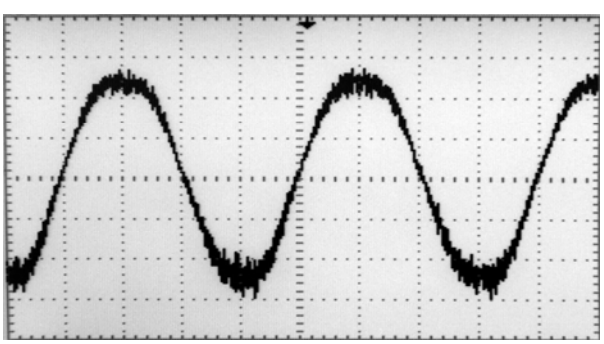

Fig. 11. Source current (0.25A/div), V_S=220V and P_{out}=80W.

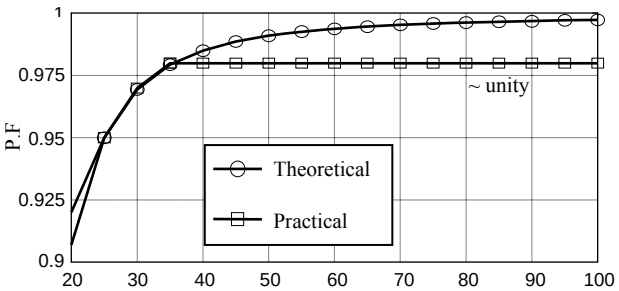

Fig. 12. PF vs. output power - theoretical and practical results.

since its input current is inherently proportional to the source voltage. When the voltage source is off-line, it is sufficient to add an inductor after the rectifier, then near unity power factor is achievable. No additional control loop is required, however VCO based controllers should be used. All essential relations based on mathematical equations are presented in this paper. Power factor relation versus values of the circuit elements is also presented and thereby optimization can be performed. Simulation and experimental results verify the theoretical analysis.

References

[1] K. H. Liu and F. C. Lee, "Zero-voltage switching technique in DC/DC converters," *IEEE Trans. Power Electron.*, Vol. 5, pp. 293–304, July 1990.

[2] Y. Xi and P. Jain, "A forward converter topology employing a resonant auxiliary circuit to achieve soft switching and power transformer resetting," *IEEE Trans. Ind. Electron.*, Vol. 50, No. 1, pp. 132–140, Feb. 2003.

[3] V. M. Pacheco, A.J. Nascimento Jr, V. J. Farias, L. C. de Freitas, and J. B. Vieira Jr., "A quadratic buck converter with lossless commutation," *IEEE Trans. Ind. Electron.*, Vol. 47, No. 2, pp. 264–272, Apr. 2000.

[4] O. García, J. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: a survey," *IEEE Trans. Power Electron.*, Vol. 18, No. 3, May 2003.

[5] B.H. Lee, C.-E. Kim, K.-B. Park and G.-W. Moon, "A new single-stage PFC AC/DC converter with low link-capacitor voltage," *Journal of Power Electronics*, p338-335, Vol. 7, No. 4, 2007.

[6] J. A. Villarejo, J. Sebastian, F. Soto, and D. J. Esther, "Optimizing the design of single-stage power-factor correctors," *IEEE Trans. Ind. Electron.*, 54, (3), pp. 1472–1482, 2007.

[7] J. J. Lee, J. M. Kwon, E. H. Kim, W. Y. Choi, and B. H.

Kwon, "Single-stage single-switch PFC flyback converter using a synchronous rectifier," *IEEE Trans. Ind. Electron.*, 55, (3), pp. 1352–1365, 2008.

[8] D.L. O'Sullivan, M.G. Egan, and M.J. Willers, "A family of single-stage resonant AC/DC converters with PFC," *IEEE Trans. on Power Electron.*, Vol. 24 (2), pp. 398-408, Feb. 2009.

[9] C. M. Wang, "A novel ZCS-PWM power-factor preregulator with reduced conduction losses," *IEEE Trans. Ind. Electron.*, 52, (3), pp. 689–700, 2005.

[10] F. S. Kang, S. J. Park, and C. U. Kim, "ZVZCS single-stage PFC AC-to-DC half-bridge converter," *IEEE Trans. Ind. Electron.*, 49, (1), pp. 206–216, 2002.

[11] Y. Kawaguchi, E. Hiraki, T. Tanaka, and M. Nakaoka, "Basic study of a phase-shifted soft switching high-frequency inverter with boost PFC converter for induction heating," *Journal of Power electronics*, Vol. 8, No. 2, 2008.

[12] I. D. Kim, E. C. Nho, S. H. Choi, J. S. Lai, "A simple ZVT PWM single-phase rectifier with reduced conduction loss and unity power factor," *Journal of Power Electronics*, Vol. 7, No. 1, pp. 55 - 63, 2007.

[13] M. A. Chaudhari, H. M. Suryawanshi, A. K. Kulwal and M. K. Mishra, "Three-phase AC-to-DC resonant converter operating in high power factor mode in high-voltage applications," *Journal of Power Electronics*, Vol. 8, No. 1, pp.60-73, Jan. 2008.

[14] B. T. Lin, and Y. S. Lee, "Power-factor correction using Cuk converters in discontinuous-capacitor-voltage mode operation," *IEEE Trans. Ind. Electron.*, 44, (5), pp. 648–653, 1997

[15] N. Jayaram, and D. Maksimovic, "Power factor correctors based on coupled inductor SEPIC and Cuk converters with nonlinear-carrier Control," *Proc. IEEE APEC*, pp. 468–474, 1998.

[16] G. Spiazzi, and P. Mattavelli, "Design criteria for power factor preregulators based on SEPIC and Cuk converters in continuous conduction mode," *Proc. IEEE IAS Conf*, pp. 1084–1089, 1994.

[17] C. Jingquan, and C. Chin, "Analysis and design of SEPIC converter in boundary conduction mode for universal-line power factor correction applications," *Proc. IEEE PESC*, pp. 742–747, 2001.

[18] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode SEPIC and Cuk power factor preregulators: analysis and design," *IEEE Trans. Ind. Electron.*, 44, pp. 630–637, 1997.

[19] L. Petersen, and R. W. Erickson, "Reduction of voltage stresses in buck-boost type power factor correctors operating in boundary conduction mode," *Proc. IEEE APEC*, pp. 664–670, 2003.

[20] E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Buck–Boost-Type Unity Power Factor Rectifier With Extended Voltage Conversion Ratio," *IEEE Trans. Ind. Electron.*, 55, (3), pp. 1123–1132, 2008.

[21] C. J. Tseng, and C. L. Chen, "A novel ZVT PWM Cuk power-factor corrector," *IEEE Trans. Ind. Electron.*, 46, (4), pp. 780–787, 1999.

[22] J. Chen, D. Maksimovic, and R. W. Erickson, "Analysis and design of a low-stress buck-boost converter in universal-input PFC applications," *IEEE Trans. Power Electron.*, 21, (2), pp. 320–329, 2006.

[23] W. Zhang, G. Feng, Y. F. Liu, and B. Wu, "New digital control method for power factor correction," *IEEE Trans. Ind. Electron.*, 53, (3), pp. 987-990, 2006.

[24] G. K. Andersen, and F. Blaabjerg, "Current programmed control of a single-phase two-switch buck-boost power factor correction circuit," *IEEE Trans. Ind. Electron.*, 53, (1), pp. 263–271, 2006.

[25] M. Jabbari, and H. Farzanehfard, "Family of Soft Switching Resonant DC-DC converters," *IET Power Electron.*, Vol. 2, Iss. 2, pp. 113–124, 2009.

[26] M. Jabbari, "A new family of soft-switching DC-DC converters," PhD. Dissertation, Isfahan University of Technology, Iran, summer, 2009.

[27] K. Madsen, and H. Schjaer-Jacobsen, "Algorithms for Worst Case Tolerance Optimization," *IEEE Trans. of Circuits and Systems*, Vol. CAS-26, Sep. 1979.

Masoud Jabbari was born in Isfahan, Iran, in 1979. He received the B.S. degree in electrical engineering in 2001 from Kashan University, Iran and the M.S. degree in electrical engineering in 2003 from Isfahan University of Technology (IUT), Iran. He is currently working on the Ph.D. electrical engineering at IUT. His research interests include soft-switching techniques in high-frequency high-power dc-dc and dc-ac converters, power factor corrections, and active power filters.

Hosein Farzanehfard was born in Isfahan, Iran, in 1961. He received the B.S. and M.S. degrees in electrical engineering from the University of Missouri, Columbia, MO, in 1983 and 1985, respectively, and the Ph.D. from Virginia Tech., Blacksburg, VA, in 1992. Since 1993, he has been a faculty member in the Department of Electrical and Computer Engineering, Isfahan

University of Technology, Isfahan, Iran, where he is currently an Associate Professor and the President of the Information and Communication Technology Institute. His current research interests include high-frequency soft switching converters, pulse power applications, power factor correction, active power filters, and high-frequency electronic ballasts. He is the author or coauthor of more than 70 technical papers published in journals and conference proceedings.