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An Address Voltage Stabilization Circuit for the Single-Side Driving Method of AC Plasma Display Panels

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ABSTRACT

An address voltage stabilization circuit for the single-side driving (SSD) method for AC plasma display panels (PDP) is proposed. The single-side driving method, which eliminates a common sustaining driver, uses only two electrodes in a three electrode AC PDP structure. The high-impedance (Hi-Z) mode operation of the data drive ICs during the sustaining period is needed for surface gas-discharge without misfiring in the SSD method but it produces the problem that the address voltage increases up to the breakdown voltage. The proposed circuit based on a flyback converter can stabilize the address voltage under the breakdown voltage and provide better surface gas-discharge performance without any misfiring in the SSD scheme.

Keywords: Plasma display panel, Single-side driving, Addressing

1. Introduction

PDP is one of the promising display devices in the aspects of thinness, wide screen area, dynamic contrast ratio and good image quality[1]. However, since cost competitiveness has recently become the most important issue in the display market, more advanced technologies to reduce the cost of PDP should be developed to compete with other display devices[2]. Fig. 1(a) shows the structure of a surface discharge type AC PDP composed of three

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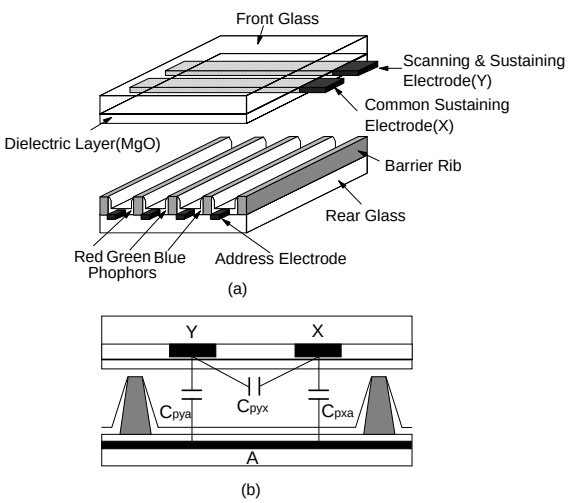

Fig. 1. Structure of three-electrode surface discharge AC PDP(a) and its equivalent capacitor model(b).

electrodes and its equivalent capacitor model is shown in Fig. 1(b)[3]. In an address display separation (ADS) scheme, the driving waveform is composed of three periods. These are the reset, addressing, and sustaining periods. Cells of the plasma display panel are initialized in the reset period and they are selected according to the image data in the addressing period. Gray scales of the image are expressed as the number of surface gas-discharges in the sustaining period[4]. To drive an AC PDP, it requires three driving boards, a ***Y*** board for scanning and sustaining, an ***X*** board for common sustaining and an ***A*** board for addressing. In the driving circuits, the costly parts are on the ***Y*** and ***X*** boards because they are composed of many semiconductor switching devices that have high electrical ratings[5]. To reduce the circuit cost by eliminating a common sustaining circuit (***X***), a single-side driving method (SSD) has been suggested[6]. There are no driving circuits except for simple bias circuitry at the ***X*** electrodes because sustaining the voltage to obtain surface gas-discharges is applied only to the ***Y*** electrodes. Unfortunately, to stabilize the gas discharge, data drive ICs must be operated in high-impedance (Hi-Z) mode which causes the address voltage to increase.

In this paper, we analyze the phenomenon of addressing the voltage increases in Hi-Z mode operation and derive the amount of power transferred from the ***Y*** electrodes during the sustaining period. Based on the analysis, a new SSD scheme, which has a DC/DC converter, is proposed to prevent an address voltage increase. Even with Hi-Z mode operation, it is possible to get stabilization of the data drive ICs, along with stable surface gas-discharges in the sustaining period.

2. Waveforms of conventional and single-side driving

A conventional PDP driving waveform is shown in Fig. 2. The sustaining voltage V_s is applied to the ***Y*** electrodes and zero voltage is applied to the ***X*** electrodes simultaneously. Accordingly, the voltage difference between the ***Y*** and ***X*** electrodes V_{yx} is $+V_s$. If some cells are selected in the addressing period, surface gas-discharges occur by the voltage difference during the

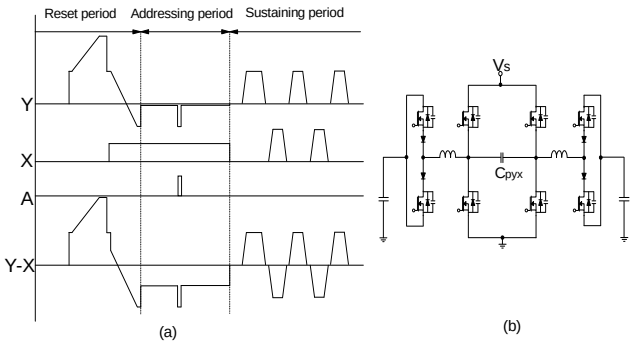

Fig. 2. Conventional PDP driving waveform in ADS driving method(a) and its sustaining circuit(b).

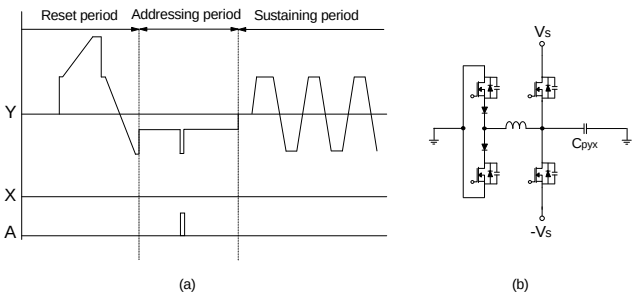

Fig. 3. Single-side driving(SSD) waveform(a) and its sustaining circuit(b).

sustaining period. After the half cycle, the sustaining voltage is applied to the ***X*** electrodes and zero voltage is applied to the ***Y*** electrodes simultaneously. The applied voltage is $-V_s$. The surface gas-discharges occur again in the cells that had gas-discharge during the previous half cycle. PDP circuits for driving the ***Y*** and ***X*** electrodes are implemented with a full bridge inverter with energy recovery circuits as shown in Fig. 2(b)[7]. The single-side driving waveform is modified from the ***Y–X*** waveform and the circuit for the SSD as shown in Fig. 3. The ***X*** electrodes are always at zero voltage and the bipolar sustaining voltages ($+V_s$ and $-V_s$) are applied to the ***Y*** electrodes in the sustaining period. The sustaining waveform is different from a conventional sustaining waveform but the voltage difference between the ***Y*** and ***X*** electrodes is the same as that of a conventional driving waveform. In the SSD, address electrodes need positive pulses to prevent the gas-discharges between the ***A*** and ***Y*** electrodes and these pulses should be synchronized with the sustaining pulses of the ***Y*** electrodes[8-12]. In the case of applying zero voltage at the address electrodes during the

sustaining period, gas-discharges occur between the ***A*** and ***Y*** electrodes, which causes surface gas-discharge between the ***Y*** and ***X*** electrodes to be unstable. To obtain pulses synchronized with sustaining pulses, data drive ICs must be operated in high-impedance (Hi-Z) mode. However, in Hi-Z mode operation of data drive ICs, the address voltage increases to the breakdown voltage of the data drive ICs and they fail in the end.

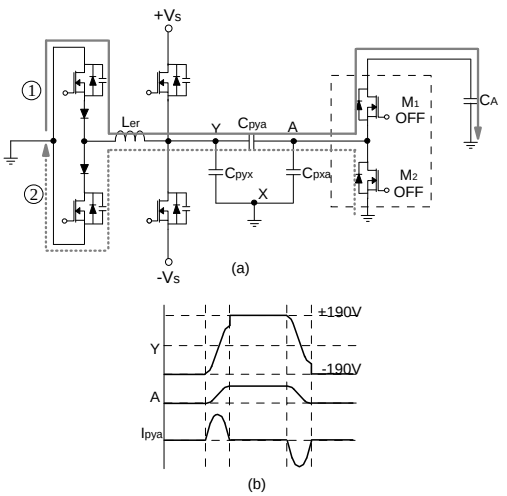

Fig. 4. Current path during rising and falling periods of sustaining pulse(a) and voltage waveforms of ***Y*** and ***A*** electrodes and current through C_{ypa}(b).

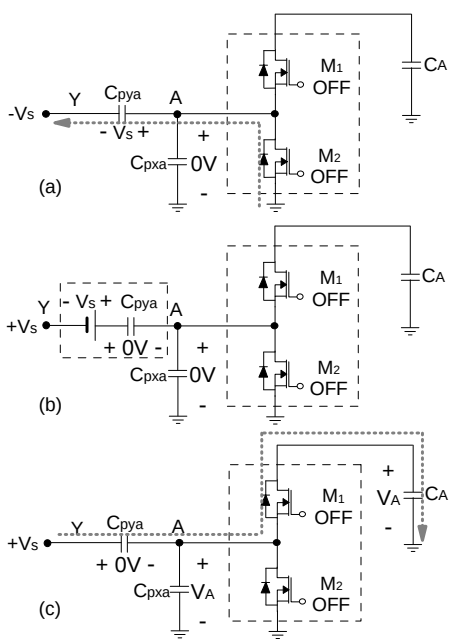

Fig. 5. Charging current path to C_A in address circuit.

3. Analysis of address voltage increase in Hi-Z mode

3.1 Analysis

In the case where data drive ICs operate in the Hi-Z mode, switches inside the data drive ICs are in the off-state and only the body diodes in the data drive ICs form conducting paths as shown in Fig. 4(a). When the data drive ICs operate in Hi-Z mode in the SSD scheme, the pulse at the ***A*** electrodes (node ***A*** in Fig. 4(a)) is applied to a rectangular waveform as shown in Fig. 4(b), which is synchronized with the bipolar sustaining pulses ($+V_s$ and $-V_s$) of the ***Y*** electrodes. In Fig. 4(b), when the sustaining pulse rises from negative sustaining voltage to positive sustaining voltage, the current path occurs through path ① in Fig. 4 (a). In this case, the current flows to the electrolytic aluminum capacitor C_A of the address circuit through the equivalent capacitor between the ***Y*** and ***A*** electrodes and the body diode of the M_1 switch inside the data drive ICs. When the sustaining pulse falls down from positive sustaining voltage to negative sustaining voltage, the current flows through path ② in Fig. 4 (a). In this case, the current flows to the energy recovery circuit (ERC) of the ***Y*** electrodes through the body diode of the M_2 switch inside the data drive ICs and the equivalent capacitor between the ***Y*** and ***A*** electrodes. Different current paths formed during the rising and falling periods of the sustaining pulses produce unbalanced charging and discharging in the electrolytic aluminum capacitor of the address circuit. As a result, repetitive sustaining pulses cause a voltage increase in the address voltage, which induces the breakdown of the data drive ICs. The charging mechanism of an electrolytic aluminum capacitor is analyzed in detail as shown in Fig. 5. Referring to Fig. 5(a), when $-V_s$ is applied to the ***Y*** electrode, the voltage across C_{pya} becomes V_s because the ***A*** electrode voltage is clamped by 0V. Fig. 5(b) is the equivalent circuit at the moment that the voltage applied to the ***Y*** electrode is changed from $-V_s$ to $+V_s$. The effectively applied voltage is $2V_s$ so that the ***A*** electrode voltage can be written as:

$$V_A = \frac{2V_S \times C_{pxa}}{C_{pya} + C_{pxa}} \tag{1}$$

and the address voltage of C_A follows this voltage as a result as shown in Fig. 5(c).

3.2 Simulation

Fig. 6 shows the simulation results of the charging voltage of C_A when bipolar sustaining pulses with +/-190V are applied to the ***Y*** electrodes. The simulation is performed only in the sustaining period. The panel capacitances listed in table 1 are the values measured from a 42-in XGA panel (column: 1024X3 (R, G, B), row: 768). Fig. 6(a) is the simulated waveform of Y_OUT which is the sustaining pulses at the ***Y*** electrodes. Fig. 6(b) is A_OUT which is the addressing pulses at the ***A*** electrodes, induced by the ***Y*** electrode pulses. Fig. 6(c) is a graph of V_CAP which is the voltage to be charged at the capacitor C_A in the address circuit. As the sustaining pulses at the ***Y*** electrodes are repeated, V_CAP is increased to the sustaining voltage of 190V. This voltage is expected from eq. (1). Fig. 6(d) and (e) are Y_OUT and A_OUT respectively, expanded in time scale.

3.3 Measurement in real PDP driving

Fig. 7 shows the measurement results from a 42-in diagonal XGA panel. Its address voltage is induced by sustaining pulses at the ***Y*** electrodes. The data drive ICs being used in PDP TVs have a breakdown voltage of 80V. The charged voltage at the electrolytic aluminum capacitor in the address circuit is 78V at 90V of sustaining voltage. 90V means that the total swing voltage of the sustaining pulse is 180V. If 100V of sustaining voltage is applied, the data drive ICs would fail. The operating sustaining voltage in a normal PDP is about 190V. It means 380V of applying sustaining voltage in the SSD, from -190V to +190V. However, from the measurement results, the sustaining voltage cannot be applied over 100V because of the breakdown of the data drive ICs. As a result, the address voltage needs to be prevented from increasing to the breakdown voltage under Hi-Z mode operation in the single-side driving method.

4. Proposed single-side driving circuit with flyback converter

Increasing address voltage is caused because the

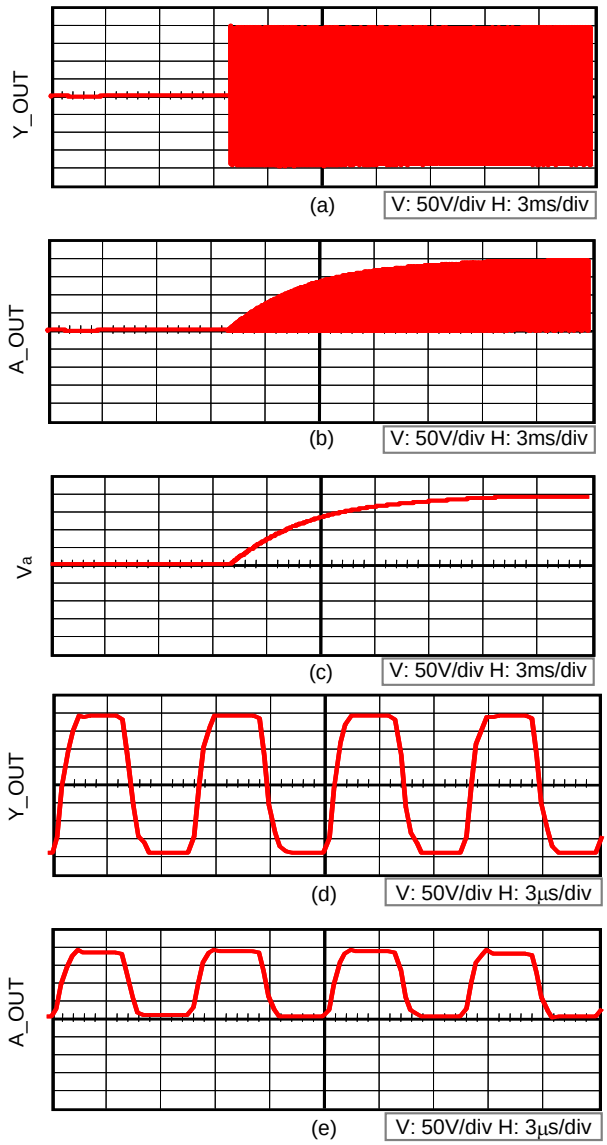

Fig. 6. Simulation results about increasing address voltage in Hi-Z mode.

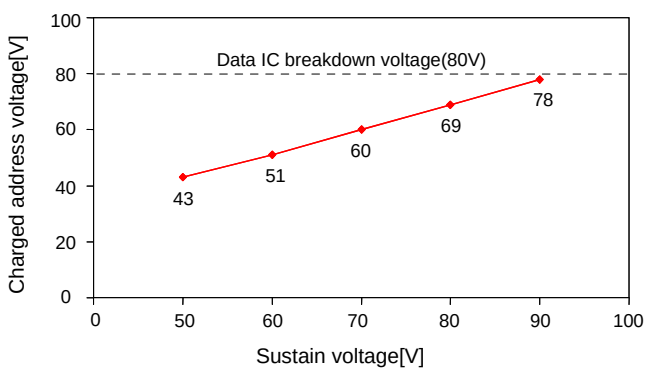

Fig. 7. Measurement of the charged address voltage under sustain voltage changes.

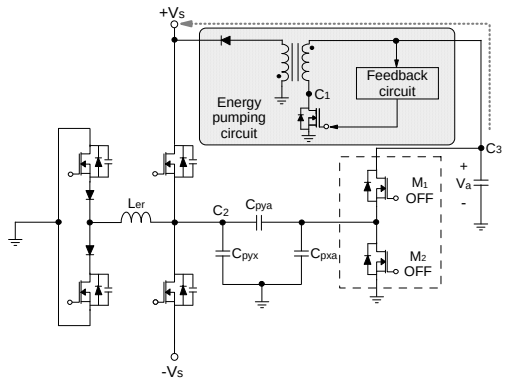

Fig. 8. Proposed single sustain driving circuit with flyback converter for regulating address voltage.

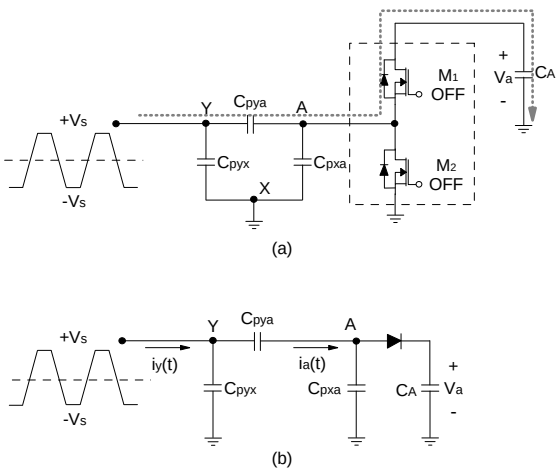

Fig. 9. Charging path to the capacitor C_A(a) and its equivalent circuit(b).

charging and discharging between the ***Y*** and ***A*** electrodes are not in balance. It is possible to prevent the address voltage from increasing by transferring the energy from the increasing address circuit, which is from the ***Y*** electrodes, to the ***Y*** sustaining circuit. A DC-DC converter is a good choice for this energy transfer. To do this, we propose new single-side driving circuit with a DC-DC converter based on a flyback converter as shown in Fig. 8. The primary side of the flyback converter is connected to the electrolytic aluminum capacitor in the address circuit and the secondary side is connected to the sustaining voltage source of the ***Y*** electrodes. To design a flyback converter, we need to calculate the power which is transferred to the address circuit by the ***Y*** sustaining pulses. Fig. 9 is the charging path to the capacitor C_A and its equivalent circuit. Before calculating the power, it is assume that the voltage of C_A is charged as V_a and that C_A is large enough to be a constant voltage source. Referring to Fig. 9, the current flowing to the ***Y*** electrode $i_y(t)$ is the resonant current formed by C_{pyx}, C_{pya}, and L_{er} and it is distributed by C_{pyx} and C_{pya}. Thus, the resonant current $i_a(t)$ which flows through C_{pya} is as follows:

$$i_a(t) = \frac{(V_s - V_a)}{Z} \sin \omega t \times \frac{C_{pya}}{C_{pya} + C_{pyx}} \tag{2}$$

where $\omega = 1/\sqrt{L_{er}(C_{pya}+C_{pyx})}$ and $Z = \sqrt{L_{er}/(C_{pya}+C_{pyx})}$.

The average current charging to C_A during one sustaining period is:

$$I_{avg} = \frac{1}{\omega T_s}\int_0^{\pi} i_a(t)\, d\omega t = \frac{2}{T_s}(V_s - V_a)C_{pya} \tag{3}$$

Therefore, the power stored in C_A during one TV filed period can be written as follows:

$$P_a = V_a I_{avg} \times \frac{N_p T_s}{T_{TV\_field}} = 2V_a(V_s - V_a)C_{pya} \times \frac{N_p}{T_{TV\_field}} \tag{4}$$

where N_p is the sustaining pulse number and T_{TV_filed} is one TV field period in seconds. In the case of NTSC, T_{TV_filed} is 16.67ms. From eq. (4), the maximum P_a in NTSC is calculated as 41.1W using V_s=190V, V_a=60V, N_p=800, and C_{pya}=55nF, which are the parameters of a 42-in diagonal XGA panel. The flyback converter can be designed based on this power.

5. Experimental results

The proposed method has been tested with a 42-in XGA panel. The transformer of the flyback converter has been implemented with EER3024 (20turns:100turns). A 5MR0380, which is the power switch integrated into the PWM controller, and two UF4007's have been used for the main switch and the output diode respectively. Fig. 10 shows the address voltage after turn-on. The applied sustaining voltage is 80V. Fig. 10(a) is the case where the flyback converter does not operate and it shows that the

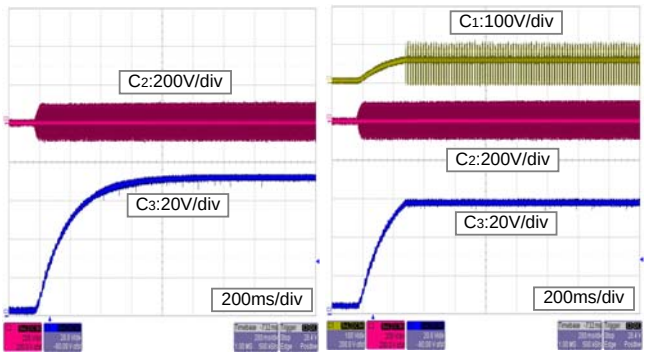

Fig. 10. Address voltage without flyback converter(a) and with flyback converter(b).

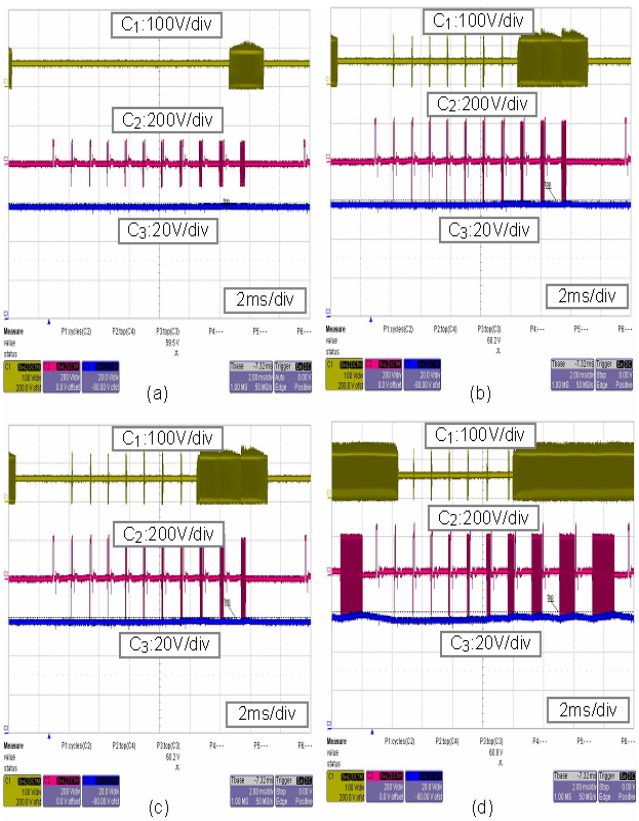

Fig. 11. Operation of flyback converter under sustain voltage(a,b) and sustain number(c,d) changes.

address voltage increases to 70V. This excessive increase of address voltage can be stabilized by 60V through an energy transfer using the converter, which is shown in Fig. 10(b). The operation of the flyback converter according to the sustaining voltage and the number changes is shown in Fig. 11. This figure shows that the switching operation of the flyback converter is increased as the sustaining voltage

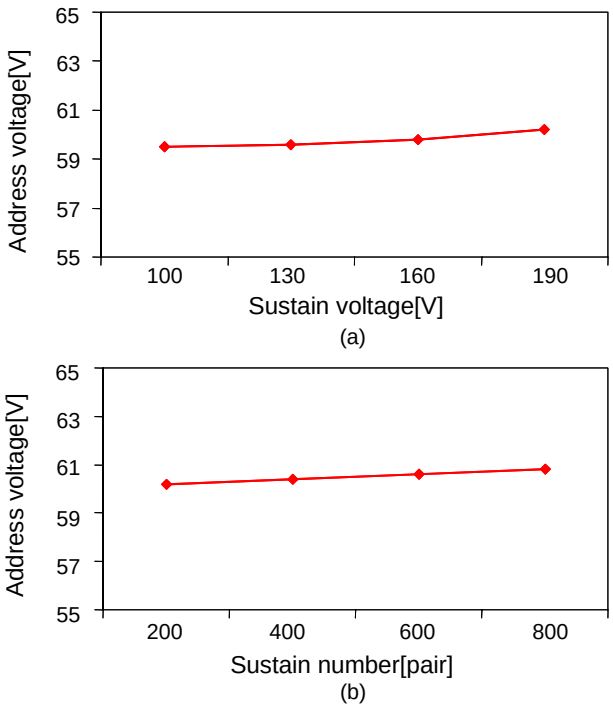

Fig. 12. Regulated address voltage under sustain voltage(a) and sustain number(b) changes.

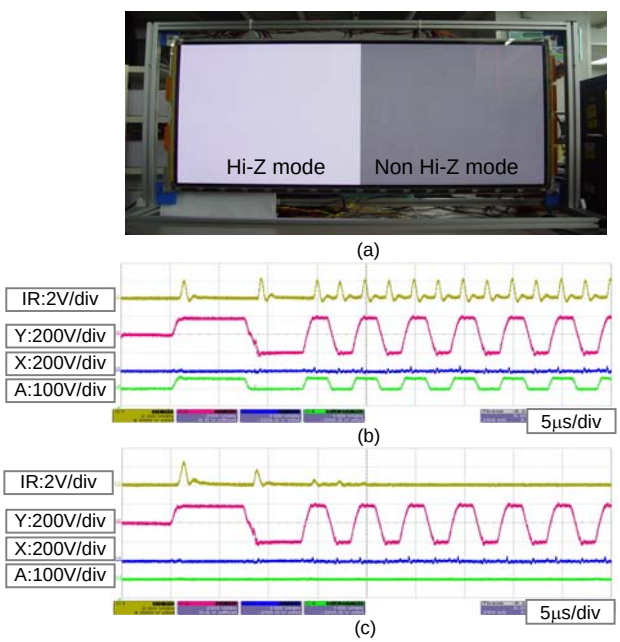

Fig. 13. Displayed image(a) and infrared waveforms with Hi-Z mode(b) and non-Hi-Z mode (c).

and the number are increased. Accordingly, as the load of the flyback converter increases, the switching operation of the flyback converter also increases so that the address

voltage is regulated with 60V. In Figs. 10 and 11, C_1, C_2, and C_3 are the drain-to-source voltage of the switch in the flyback converter, the sustaining pulse at the ***Y*** electrodes, and the address voltage respectively. These nodes are marked in Fig. 8. Fig. 12 shows that the address voltage regulated by the flyback converter increased the sustaining voltage from 100V to 190V and the sustaining number from 200 pairs to 800 pairs. One pair includes one positive sustaining pulse and one negative sustaining pulse. The ripple voltage of the address is controlled under 1V as the sustaining voltage and sustaining number increase. It is very stable compared with prior SSDs. A result of adopting the proposed single-side driving is indicated in Fig. 13(a). The displayed image shows two types of modes, Hi-Z mode and non-Hi-Z mode. The left side of Fig. 13(a) is an image driven by Hi-Z mode and the right side is by non-Hi-Z mode. The infrared (IR, 828nm) waveforms that are produced by a surface gas-discharge were measured in the sustaining periods. The measured waveforms IR and each electrode are (b) and (c) in Fig. 13 according to the operational modes of the data drive ICs. The left side, which displays a good full white image, has stable gas-discharges as shown Fig. 13(b). The IR waveforms are stable in all sustaining pulses. On the other hand, the right side, which displays a bad full white image, has unstable gas-discharges as shown in Fig. 13(c). The IR waveforms gradually disappear as the sustaining pulses are applied. Accordingly, the proposed single-side driving offers stable gas-discharge in Hi-Z mode and stabilization of the address circuit by regulating address voltage with a flyback converter.

6. Conclusions

In this paper, a new single side-driving circuit is proposed to stabilize address voltage and get stable surface gas-discharge in Hi-Z mode operation. The misfiring phenomenon between the sustaining electrode and the address electrode can be solved using Hi-Z mode operation of the data drive ICs during the sustaining period in the SSD. Hi-Z mode operation produces a serious problem. The problem is that the address voltage is increased over the breakdown voltage of the data drive ICs due to the energy induced by the sustaining pulses. This problem can be solved by a simple DC/DC converter such as flyback converter which delivers excessive address power to the sustaining voltage source. The mechanism of the address voltage increase has been analyzed and the amount of the induced power is calculated for the converter design. The proposed method is designed and verified with a 42-in XGA PDP panel with SSD. The experimental results show that it offers better surface gas-discharge performance without any misfiring in the single-side driving scheme. It also prevents the addressing data drive ICs from overvoltage failure. In addition to the sustaining voltage source, any DC voltage sources can be used as a target voltage source for energy transfer.

References

[1] Sobel, "Plasma displays," *IEEE Trans. Plasma Sci.*, Vol. 19, No. 6, pp. 1032–1047, Dec. 1991.

[2] T. Shinoda and K. Awamoto, "Plasma display technologies for large area screen and cost reduction," *IEEE Trans. Plasma Sci.*, Vol. 34, No. 2, pp. 279–286, Apr. 2006.

[3] H. B. Hsu, C. L. Chen, S. Y. Lin, and K. M. Lee, "A novel energy-recovery sustaining driver for plasma display panel," *IEEE Trans. Ind. Electron*., Vol. 47, No. 5, pp. 1118–1125, Oct. 2000.

[4] K. Yoshikawa, Y. Kanazawa, M. Wakitani, T. Shinoda, and A. Ohtsuka, "A full color AC plasma display with 256 gray scale," in *Proc. Japan Display Conf.*, pp. 605–608, 1992.

[5] J. Y. Lee, J. S. Kim, N. S. Jung, and B. H. Cho, "The current injection method for ac plasma display panel (PDP) sustainer," *IEEE Trans. Ind. Electron*., Vol. 51, No. 3, pp. 615–624, June 2004.

[6] J. Y. Lee and D. Y. Lee, "Driving device and method for plasma display device and panel," *KR. Patent*, 10–2005–0041716, May 4, 2005.

[7] L. F. Weber, K. W. Warren, and M. B. Wood, "Power efficient sustain drivers and address drivers for plasma panel," *US Patent* No. 4 866 349, Sep. 12, 1989.

[8] S. H. Kang, K. D. Cho, M. S. Kim, J. H. Ryu, and K. S. Hong, "New driving method and circuits for low cost AC plasma display panel," *IEEE Trans. Consum. Electron*., Vol. 51, No. 1, pp. 179–182, Feb. 2005.

[9] K. Ito, B. G. Cho, M. K. Lee, J. W. Song, S. C. Kim, H. S. Tae, N. S. Jung, and K. S. Lee, " New two stage recovery (TSR) driving method for low cost AC plasma display

panel," in *Proc. IDW Dig.*, pp. 461–464, 2005.
[10] K. Sakita, K. Takayama, K. Awamoto, and Y. Hashimoto, "High–speed address driving waveform analysis using wall voltage transfer function for three terminals and V_t close curve in three–electrode surface–discharge AC–PDPs," in *Proc. SID Dig.*, pp. 1022–1025, 2001.
[11] K. Sakita, K. Takayama, K. Awamoto, and Y. Hashimoto, "Ramp setup design technique in three–electrode surface–discharge AC–PDPs," in *Proc. SID Dig*., pp. 948–951, 2002.
[12] B. G. Cho, H. S. Tae, K. Ito, N. S. Jung, and K. S. Lee, "Study on discharge stability of cost–effective driving method based on Vt close–curve analysis in AC plasma display panel," *IEEE Trans. Electron Devices*, Vol. 53, No. 5, pp. 1112–1119, May 2006.

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