JPE 10-1-5

A High Frequency-Link Bidirectional DC-DC Converter for Super Capacitor-Based Automotive Auxiliary Electric Power Systems

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Abstract

This paper presents a bidirectional DC-DC converter suitable for low-voltage super capacitor-based electric energy storage systems. The DC-DC converter presented here consists of a full-bridge circuit and a current-fed push-pull circuit with a high frequency (HF) transformer-link. In order to reduce the device-conduction losses due to the large current of the super capacitor as well as unnecessary ringing, synchronous rectification is employed in the super capacitor-charging mode. A wide range of voltage regulation between the battery and the super capacitor can be realized by employing a Phase-Shifting (PS) Pulse Width Modulation (PWM) scheme in the full-bridge circuit for the super capacitor charging mode as well as the overlapping PWM scheme of the gate signals to the active power devices in the push-pull circuit for the super capacitor discharging mode. Essential performance of the bidirectional DC-DC converter is demonstrated with simulation and experiment results, and the practical effectiveness of the DC-DC converter is discussed.

Key Words: Bidirectional DC-DC converter, High Frequency (HF)-link, Push-pull circuit, S.C. charging mode, S.C. discharging mode, Super Capacitor (S.C.), Synchronous rectification

I. INTRODUCTION

Researches on high performance bidirectional DC-DC converters have been gaining momentum in industry, residential and aerospace environments [1]–[4]. In particular, for advanced and next generation vehicles such as Electric Vehicles (EVs) and Hybrid Vehicles (HEVs), this type of DC-DC converter is playing a key role for establishing an efficient power conversion and supplying system [5].

Nowadays, demands for the dual DC-voltage power systems as illustrated in Fig. 1 are surging for EVs, HEVs and other low CO2-emission vehicles. They are even being utilized in a conventional combustion engine car named More Electric Vehicles (MEVs) [1].

In the electric power architecture illustrated in Fig. 1, the high voltage battery, e.g. 42V or 288V, is employed as the main DC bus-line to supply more power to the loads as well as to reduce the volume of the electric wire harness [1], [2]. In this scheme, an auxiliary energy storage device such as a super capacitor (S.C.) is regarded as a key device for assisting the operation of the main battery against the repetitive charging/discharging operation and abrupt energy demands from the loads.

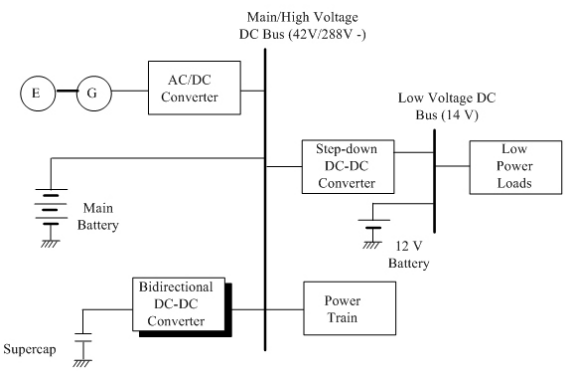

Fig. 1. Dual DC bus-voltage architecture in advanced electric vehicles (EVs, HEVs).

The bidirectional DC-DC converters developed for S.C. interfacing circuits up to the present time have been mainly non-isolated bidirectional DC-DC converters (current reversible DC choppers) [6], [7]. The non-isolated type circuit topology generally has some advantages such as a simple and light circuit configuration due to the transformer-free circuit topology. Since the tolerable and operating voltage of a S.C. cell is relatively low, e.g. 2.7 V, it is typical that a large

Manuscript received Aug. 20, 2009; revised Dec. 6, 2009
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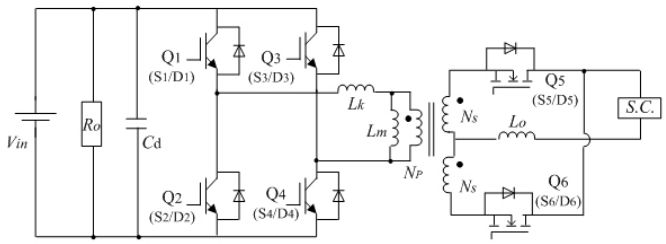


Fig. 2. Proposed HF-link bidirectional DC-DC converter for super capacitor interface.

volume of S.C. cells are connected in series in order to boost the terminal voltage of the S.C.-bank so that no large voltage difference between the two power sources takes place. The series connection of many S.C. cells may trigger some drawbacks such as an increase in ESR (Equivalent Series Resistance) and a decrease in the capacitance of the total S.C. bank. Moreover, installation of additional voltage-balancing circuits is required in parallel with the S.C. cells, and this inherently causes power losses in the total power conversion scheme as well as increase in the S.C. bank size. This leads to deterioration in the energy utilization of the S.C. cells.

Several bidirectional DC-DC converter topologies for low voltage/large current power conversion have been presented so far for power supplies in industry, communication and information facilities etc [2]–[4], [7], [9]. However, there are few proposals that are specified for a S.C. interface power converter under the low voltage condition.

As a new approach for creating a simple and versatile power converter for a S.C. interfacing circuit suitable for the low voltage condition, a HF transformer isolation-type bidirectional DC-DC converter topology is newly developed and its performance is evaluated in this research.

This paper is organized as follows: First, the circuit configuration is introduced. Then the operation principle of the proposed bidirectional DC-DC converter is explained. Next, the operations and the performance characteristics of the proposed bidirectional DC-DC converter are investigated by computer simulations. Finally, the validity of the converter topology is demonstrated with experiments using a prototype of the proposed DC-DC converter.

II. Circuit Topology and Operation Principle

A. Circuit configuration

The proposed bidirectional DC-DC converter topology is shown in Fig. 2.

The primary power source (main battery or DC bus line) V_{in} supplies power to the load R_o in the normal condition. In the case of a fault in V_{in} and the upsurge of power demand from R_o, the stored energy in the S.C. is delivered to the primary side.

In the S.C. charging mode, the full bridge circuit in the primary side operates as an inverter, and the push-pull circuit rectifies and delivers power to the S.C. by synchronous rectification of S_5 of Q_5 and S_6 of Q_6.

In the S.C. discharging mode, the push-pull circuit operates as an inverter, and the full bridge circuit works as a rectifier.

The motivations for employing a push-pull circuit can be validated by the following: (i) The S.C. is well suited to a current source type power converter. As a result, no bulky smoothing capacitor exists for the output side in the proposed bidirectional DC-DC converter. (ii) Since the operating frequency of the current through the output smoothing inductor L_o can naturally double the converter operating frequency, the size and volume of the output smoothing inductor L_o can be reduced effectively.

In the full bridge circuit configuration in the primary-side power stage, Phase-Shifted Pulse Width Modulation (PS-PWM) can be applied to the active switches Q_1-Q_4. Thus, the output voltage and output power regulation are performed by the PS-PWM scheme in Q_1-Q_4 for the S.C. charging mode.

In the S.C. discharging mode, the shortcut period of the secondary windings of the HF transformer is adjusted by changing the overlapping ON-term of S_5 and S_6. In the gate pulse sequence applied in the bidirectional DC-DC converter, the ON duty-cycles of S_5 and S_6 should be larger than 50%.

B. S.C. charging mode operation

The converter operating waveforms in the S.C. charging mode are schematically illustrated in Fig. 3 without consideration for the dead time in the full bridge circuit. In the S.C. charging mode, the output power, i.e. the S.C. charging current is controlled by the PS-PWM of the gate signals for S_1-S_4 in the full bridge circuit.

The operation mode is divided into four steps as follow:

$[t_0 - t_1]$: S_4 of Q_4 is turned-on at t_0 while S_1 of Q_1 is in the on-state. Accordingly, the power from V_{in} is delivered to the loads R_o via the HF transformer, and the current thorough the output inductor L_o rises linearly.

$[t_1 - t_2]$: S_1 of Q_1 is turned off at t_1 while S_4 remains in the on-state. At the same time, S_6 of Q_6 in the push-pull circuit is turned on, while S_5 of Q_5 remains in the on-state. In this interval, the zero voltage duration across the primary winding of the HF transformer appears, and no power is transferred to the output terminal. In the secondary side, the energy stored on L_o freewheels through S_5 and S_6, and i_{Lo} linearly decreases.

$[t_2 - t_3]$: At t_2, S_4 of Q_4 is turned off, and S_3 of Q_3 turns-on in the complementary way. At the same time, S_5 of Q_5 is turned off while S_6 of Q_6 remains in the on-state. The converter operation during this interval is similar to the one in the interval of $t_1 - t_2$ except that the primary winding of the HF transformer is reversely polarized.

$[t_3 - t_4]$: At t_3, S_2 is turned-off, and S_1 is turned on in the complementary way. In addition, S_5 is turned on while S_6 remains on. The operation in this stage is similar to the one in $t_1 - t_2$, so the stored energy in L_o freewheels through S_5 and S_6 with the secondary winding of the HF transformer shorted, consequently i_{Lo} linearly decays. After S_6 is turned off, the next cycle begins while S_5 remains in the on-state at t_4.

In the S.C. charge mode, the operation manner of the current-fed push pull converter is similar to the step-down converter, as follow:

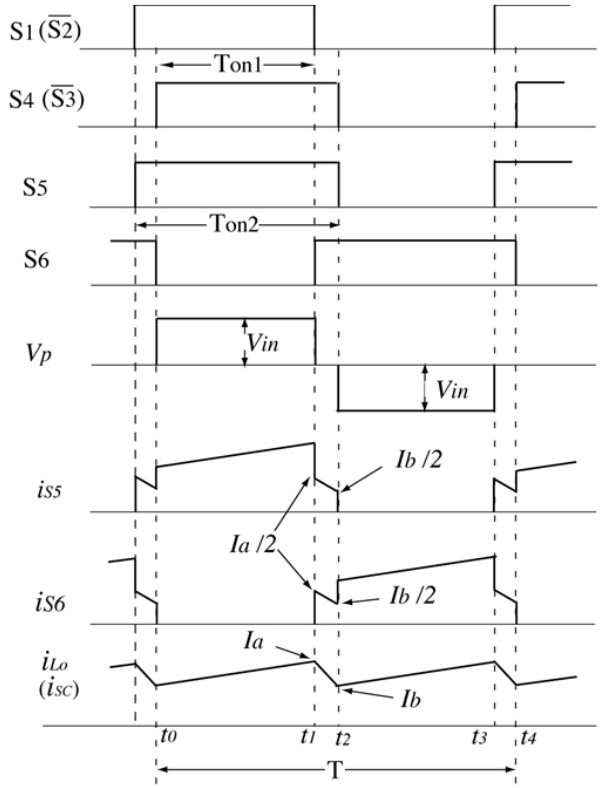


Fig. 3. Relevant voltage and current waveforms in S.C. charging mode.

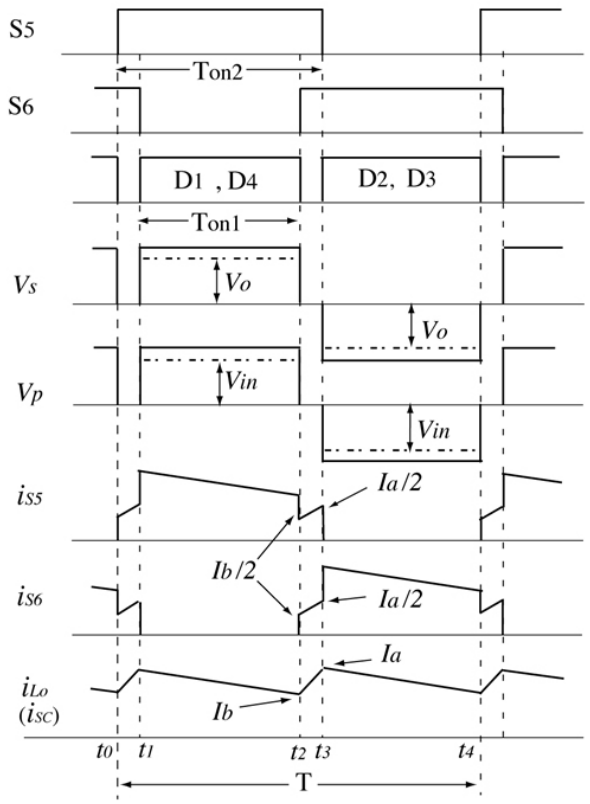


Fig. 4. Relevant voltage and current waveforms in S.C. discharging mode.

$$V_{sc} = \frac{2N_s}{N_p} \cdot DV_{in}, \quad D < 0.5 \tag{1}$$

where D is defined by T_{on1}/T in Fig. 3.

C. S.C. discharging mode operation

In the S.C. discharging mode, one-switching period is divided into the four stages as depicted in Fig. 4. Similar to the aforementioned description, the dead time of each switch-leg as well as the diode reverse-recovery currents are not taken into consideration in the following explanation.

$[t_0 - t_1]$: At t_0, S_5 is turned-on while S_6 remains in the on-state. At the same time, D_3 of Q_3 and D_4 of Q_4 are reversely biased. Since the HF transformer winding of the push-pull circuit is shorted, the inductor L_o stores energy and the current i_{Lo} linearly increases. Thus, the current is equally shared by S_5 and S_6, and no power is delivered to the primary-side power source V_{in} and the load R_o.

$[t_1 - t_2]$: At t_1, S_6 is turned-off while S_5 is in the on-state. At the same time, D_1 of Q_1 and D_4 of Q_4 are forward-biased. In this interval, the energy stored in L_O during the previous interval, is delivered to V_{in} and R_o. As a result, i_{Lo} through L_o rises linearly during this interval.

$[t_2 - t_3]$: At t_2, S_6 is turned-on while S_5 remains in the on-state. At the same time, D_1 of Q_1 and D_4 of Q_4 are reversely biased. The circuit operation in the interval is similar to that in $t_0 - t_1$. Thus, i_{Lo} increases linearly due to the stored energy in L_o, and no power is transferred to V_{in} and R_o.

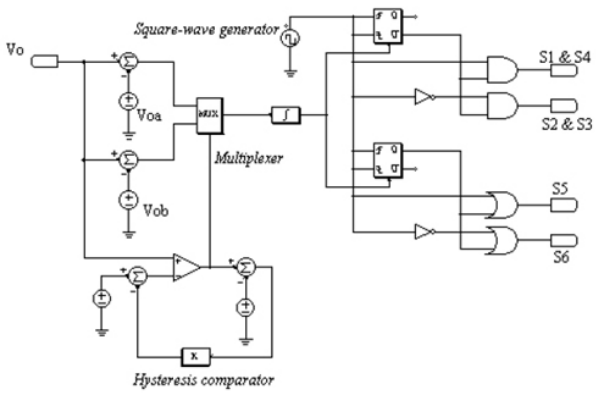


Fig. 5. Circuit diagram of the S.C. charge/discharge mode controller.

$[t_3 - t_4]$: At t_3, S_5 is turned off while S_6 is in the on-state. At the same time, D_2 of Q_2 and D_3 of Q_3 are forward biased. In this stage, the energy stored in L_o during the previous interval is delivered to V_{in} and R_o. Thus, the circuit operation in this interval is similar to that in $t_1 - t_2$. After S_5 is turned-on while S_6 remains in the on-state at t_4, the next cycle begins.

In the S.C. discharging mode, the operation manner of the push pull circuit is similar to the step-up converter, as given by:

$$V_{sc} = \frac{N_s}{N_p} \cdot \frac{V_0}{2(1 - D')}, \quad D' > 0.5 \tag{2}$$

where D' is defined by T_{on2}/T in Fig. 4. Therefore, the discharging current from the S.C. is regulated by controlling

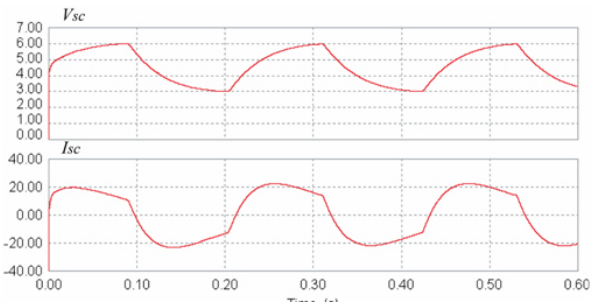


Fig. 6. Simulated operating waveforms for S.C. charging/discharging mode cycle.

the overlapping pulse widths for S_5 and S_6.

III. Control Scheme for S.C Charging/Discharging Mode Selection

TABLE I
Circuit Parameters of Experimental Prototype

Parameter	Symbol	Value & Unit
Capacitance of S.C	C_{sc}	450[F] (four-cells series)
ESR of S.C.	R_{sc}	$4.5[m\Omega]$
Main Battery	V_{in}	50 [V]
S.C. Maximum Voltage	V_{omax}	10.8 [V] (2.7 [V]/cell)
HF Transformer Turn Ratio	$N_T(=N_P/N_S)$	5
Link Inductor	L_o	60 $[\mu H]$
Switching Frequency	f_s	60 [kHz]

TABLE II
Specification of S.C. Cell

Parameter	Value & Unit
Rated Capacitance	1350 [F]
Rated Voltage (DC)	2.7 [V]
Normalized ESR (DC)	$1.5[m\Omega]$
Specific Energy Density	6.5 Wh/kg
Specific Power Density	5.5 kW/kg(@2.7[V])
Continuous Charge-Discharge Current	60 [A]
Volume	0.15 $[l]$

The S.C. charging and discharging cyclic operation of the proposed bidirectional converter are evaluated by simulations. The schematic diagram of the S.C. charging/discharging mode selector is illustrated in Fig. 5.

The principle parameters in the simulation circuit model are: Csc = 450[F], Rsc (ESR of S.C.) = 4.5[mΩ], $V_{sc(max)}$ = 10.8[V], V_{in} = 42[V], $L_o = 50[\mu H]$, $C_o = 500[\mu F]$, NT(Np/Ns) = 5 and the switching frequency fs = 60[kHz]. The parameters of the S.C. cell are modeled on the actual product (high power electric double layer capacitors for EV applications PSLF-1350, produced by Power Systems Co. LTD.), which is used for the experimental verifications as discussed later.

In this simulation, the S.C. operating voltage is limited from $V_{OL} = 3[V]$ to $V_{OH} = 6[V]$ in order to shorten the calculation time.

The simulation waveforms are shown in Fig. 6. The simulation waveforms indicate that the mode-exchanging of the

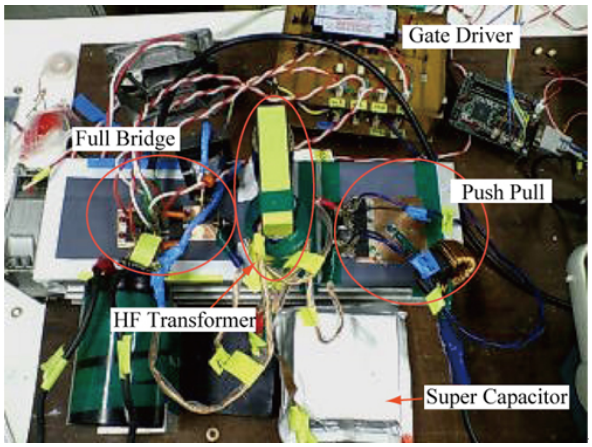


Fig. 7. Laboratory prototype and experimental setup.

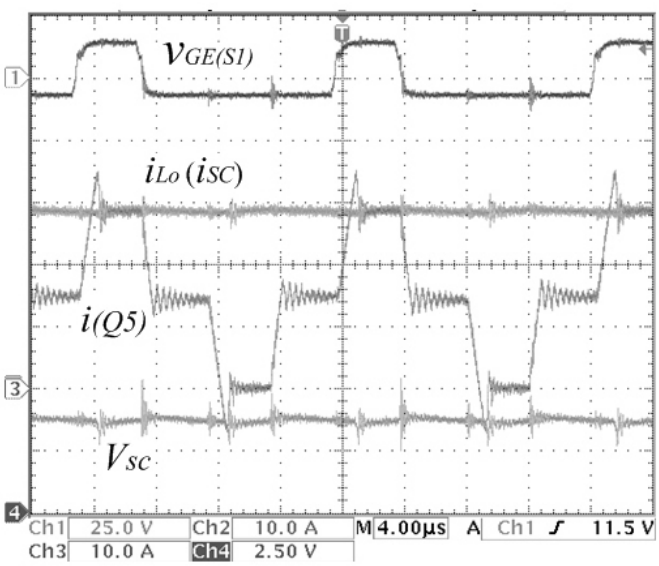


Fig. 8. Measured repetitive circuit operation waveforms in S.C. charging mode.

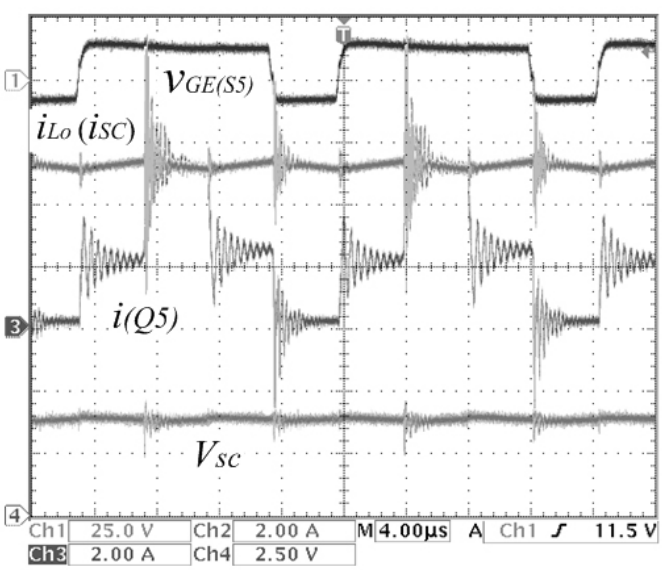
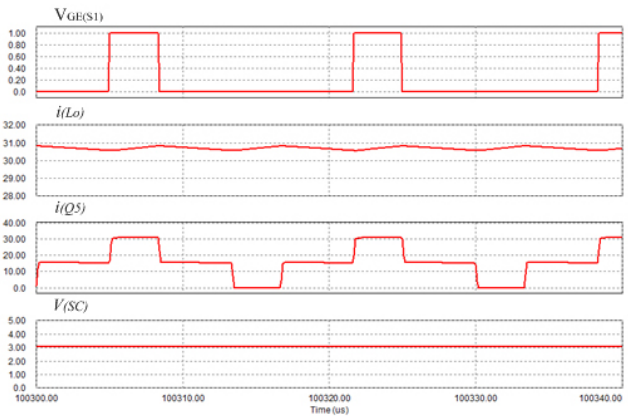
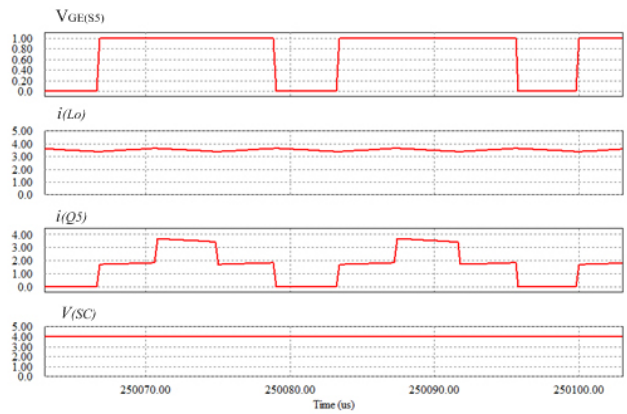


Fig. 9. Measured repetitive circuit operation waveforms in S.C. discharge mode.



(a) Charging mode



(b) Discharging mode

Fig. 10. Simulated waveforms.

charging and discharging can be determined from the S.C. voltage as well as the battery power conditions. It is also proven that the current fed push-pull circuit topology is useful for the repetitive charging and discharging cycle of the main battery.

IV. Experimental Results

A. Specification of experimental prototype

The performance of the proposed bidirectional DC-DC converter for a S.C. interfacing power conditioner is evaluated in an experiment with a 1.2[kW]-60[kHz] prototype. The exterior appearance of the laboratory prototype is depicted in Fig. 7. The specifications of the experimental set-up are indicated in Table 1. In the experiment, the S.C. cells developed for EVs are used, the specifications of which are indicated in Table 2.

In this laboratory prototype, two-in-one IGBT modules (Mitsubishi CM100DU-12F) are employed for the primary-side full bridge circuit. And, the bidirectional active switches Q_5 and Q_6 in the push-pull circuit are constructed by two-paralleled MOSFETs (Infineon Technologies BUZ341, $R_{DS(ON)} = 60[m\Omega]$), respectively.

B. S.C. charging/discharging operation

Fig. 8 shows the operating waveforms of the push-pull circuit with the gate-emitter voltage of the controlled switch Q_1 in the S.C. charging mode. The inductor current i_{Lo}, i.e. the super capacitor-charging current i_{sc} is well regulated, and no significant current ripple is observable in the inductor current. In this mode, the reverse-recover current in the rectifier diodes D_5 of S_5 and D_6 of S_6 causes voltage spikes in the S.C. voltage V_{SC}. Those unnecessary voltage spikes, however, can easily be reduced by introducing synchronous rectification as described in the next subsection.

The steady-state operating waveforms of the push-pull circuit in the S.C. discharging mode along with the gate-emitter voltage of the controlled switch Q_1 are shown in Fig. 9. There are current surges observed due to the hard-switching mode turn-off commutation in Q_5 and Q_6. These current spikes can be suppressed by a RCD snubber employed to Q_5 and Q_6 as mentioned later.

The simulated waveforms for the charging and discharging modes are additionally provided in Fig. 10 under the same circuit conditions as those of the experimental prototype. From the results of Figs. 8-10, the circuit operations theoretically described in Fig. 3 and 4 are practically verified.

As mentioned previously and depicted in Fig. 11(a), there are voltage and current surges generated due to the hard-switching mode turn-off operations in Q_5 and Q_6, which are inherent in the push-pull circuit operating by inverter mode [3]. As a solution, a RCD snubber is employed in the prototype DC-DC converter, and the operating waveforms with the passive snubber are shown in Fig. 11(b). The voltage peak stress is reduced by one-third with the aid of the snubber circuit.

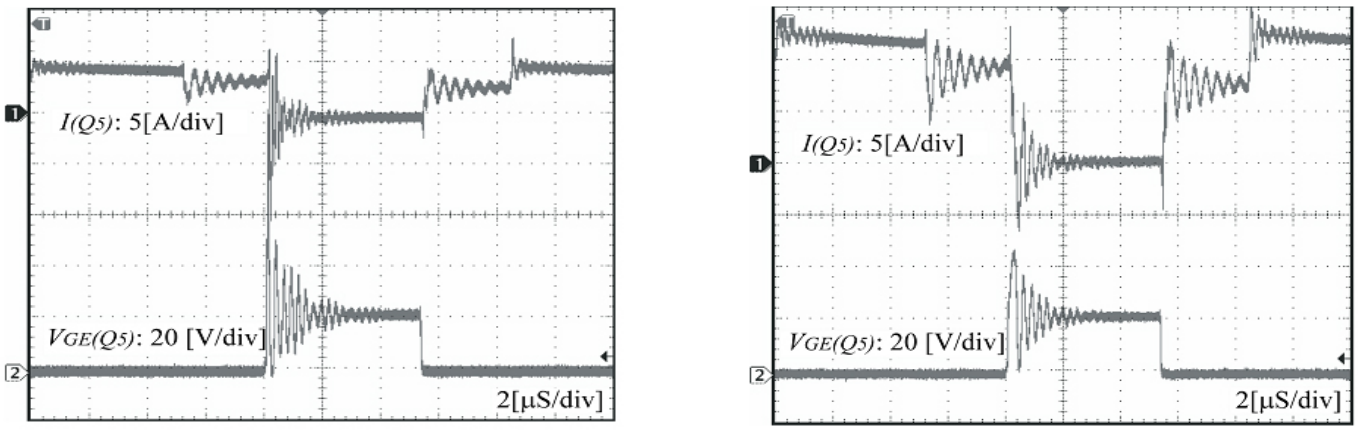
Employment of soft switching lossless cells is a more effective solution from the view point of converter efficiency [10], [11].

C. Effect of synchronous rectification

The large charging/discharging currents in the S.C. have a significant impact on the conversion efficiency in the DC-DC converter. Figs. 12(a) and 12(c) show the upscale current waveforms of Q_5 in the S.C. charging mode when the push-pull circuit operates with the diode rectifiers (D_5 and D_6). The current surges observed in the waveform of I_{Q5} are due to the reverse recovery of the diode D_6 in the opposite-side active switch Q_6. On the other hand, the current waveforms with the synchronous rectifications of S_5 and S_6 are depicted in Figs. 12(b) and 12(d), where no significant current surge occurs. Thus, the reverse recovery-related current surges as well as the ringing currents due to the parasitic capacitance of the MOFET switches can be suppressed effectively by introducing synchronous rectification in Q_5 and Q_6.

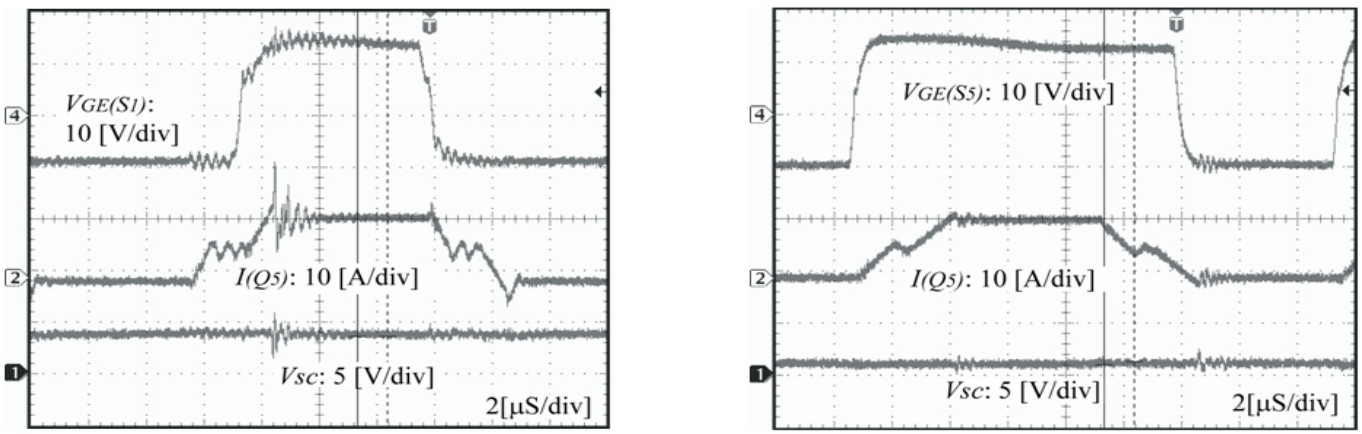
The conduction loss of Q_5 (Q_6) obtained by the synchronous rectification is compared with one by the diode rectifying mode in Fig. 13. It can be seen from the results that a reduction in the conduction loss can be achieved 60 [%] at Isc=30[A] by synchronous rectification.

It has been verified that adopting a synchronous rectifier is useful not only for reducing the conduction loss but for precluding the occurrence of ringing in the push-pull circuit.

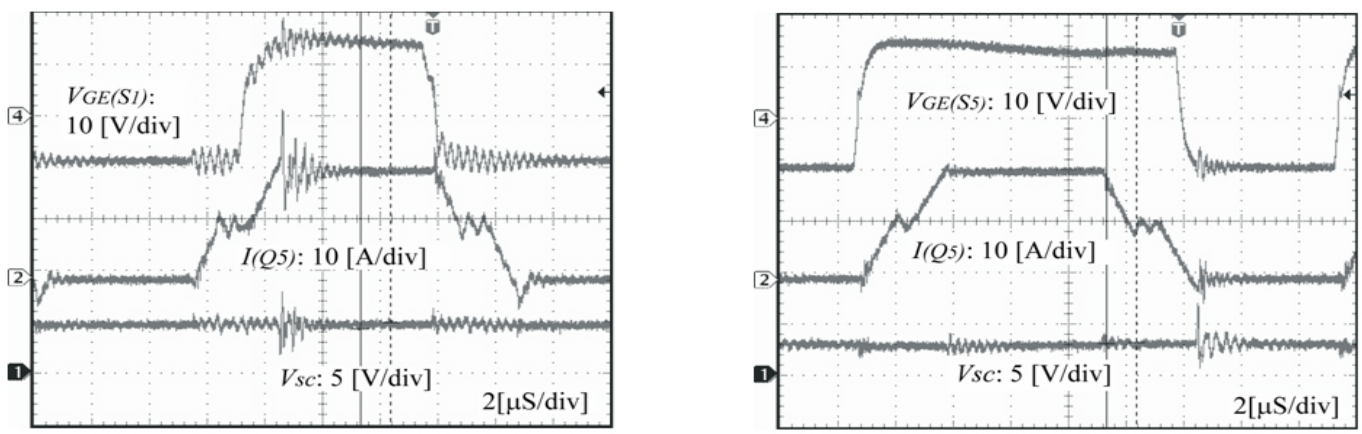


(a) Snubberless (b) RCD snubber

Fig. 11. Operating waveforms of active switch Q5 in S.C. discharging mode.



(a) diode rectifier (I_{sc} = 10[A]) (b) synchronous rectifier (I_{sc} = 10[A])



(c) diode rectifier (I_{sc} = 20[A]) (d) synchronous rectifier (I_{sc} = 20[A])

Fig. 12. Operating voltage and current waveforms of active switch Q5 in S.C. charging mode.

V. CONCLUSIONS

This paper presents the performance evaluation of a high frequency transformer-link bidirectional DC-DC converter for a super capacitor bank in the low operating voltage condition. From the simulation and experimental results based on its experimental prototype, the following advantageous properties of the bidirectional DC-DC converter have been clarified:

- The push-pull circuit is useful for a low-voltage (fewer series connections) super capacitor and its bidirectional power-flow operation.

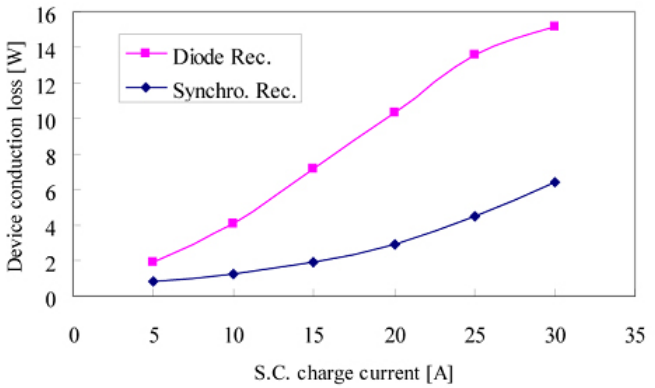


Fig. 13. Comparison on conduction losses of push-pull circuit (in S.C. charging mode).

- The wide range of charging and discharging operations of a super capacitor can be achieved seamlessly by a constant frequency phase-shifting PWM/overlapping PWM scheme.
- Power loss in the low voltage side circuit can be reduced effectively by employing synchronous rectification, thus improvement of the power conversion efficiency as well as the power density of the DC-DC converter can be expected.

In order to improve the switching performances and the conversion efficiency, employing the soft-switching technique into the push-pull circuit as well as the full bridge circuit might be the best approach. Evaluation and discussion of a soft-switching bidirectional DC-DC converter utilizing the circuit topology presented here will be reported in the future.

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