

# Isolated Topologies of Switched-Resonator Converters

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## Abstract

Switched-resonator converters are a new family of soft switching DC-DC converters where the energy is transferred via a resonator. This paper introduces some isolated topologies of this family. The achieved advantages include, load independent soft-switching, self short-circuit protection, and optimization capability due to topology variety. Compared to conventional series-resonant converters, outstanding advantages such as a smaller number of switches and diodes, a smaller transformer, and lower current stresses are achieved. A general synthesis scheme, functional topologies, and essential relations are included. Experimental results from a laboratory prototype confirm the presented theoretical analysis.

**Key Words:** Isolation, Resonant Converter, Soft Switching, Switched Resonator Converters, ZCS

## I. INTRODUCTION

Isolated switching converters are often derived from non-isolated topologies. A common scheme is to place a transformer where the high frequency voltage/current pulses are produced [1]. In such converters, the transformer leakage inductance may produce additional switching losses and high voltage spikes across the converter switches. Furthermore, the energy stored in the transformer magnetizing inductance should be reset to prevent it from saturation [2], [3].

Soft-switching techniques have been developed to reduce switching losses and electromagnetic interference (EMI). Under soft-switching conditions, the switching frequency can be increased to enhance the converter power density. This condition is commonly attained by zero voltage switching (ZVS) and zero current switching (ZCS). An insulated gate bipolar transistor (IGBT) is an appropriate switch for power applications. The ZCS technique is more compatible with the IGBT characteristics since it makes the tailing-current irrelevant [4]. In order to decrease current stresses and conduction losses, unnecessary energy circulation should be prevented and hence unidirectional switches such as the reverse-blocking IGBT (RB-IGBT) can be employed [5]–[7].

Resonant converters are a family of soft-switching converters in which energy is transferred through a high-frequency resonant tank and switching is performed at the zero-crossing instants of the current or voltage. A series LC tank is the simplest network which is employed in resonant converters to

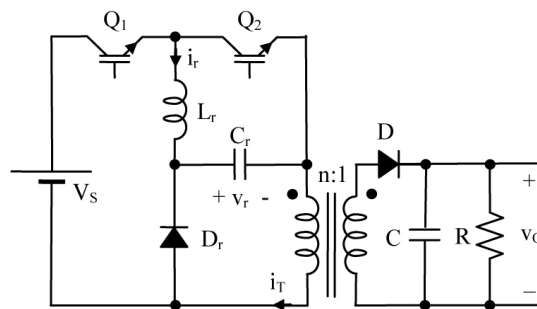


Fig. 1. Topology of HL-SwRC.

provide the ZCS condition [1], [8]–[15].

Recently a new family of resonant converters namely switched resonator converter (SwRC) was introduced [10]–[14]. This converter family contains fifteen soft-switching topologies in its basic non-isolated synthesis called group G. This group has five subgroups. These subgroups are G1 to G5. This paper presents an isolated version of a G5 converter with a transformer and a half-wave rectifier. The general synthesis scheme, functional topologies, key waveforms, and essential relations are provided. A precise comparison with a conventional series-resonant converter is performed which illustrates outstanding advantages such as a lower number of switches and diodes, a smaller transformer, less current stresses, and higher efficiency. Practical results from a 210W laboratory prototype confirm the presented theoretical analysis.

## II. PROPOSED CONVERTER

Consider one of the isolated switched-resonator topologies, called the HL-SwRC, as shown in Fig. 1 where ‘HL’ represents the topology formation. For simplicity, it is assumed that the

converter is in the steady-state, all the circuit elements are ideal, and the output capacitor  $C$  is large enough so that the output voltage stays constant during one switching cycle. In this section, the transformer is supposed to be ideal and thus the effects of the leakage and magnetizing inductances are ignored. The following quantities are defined where  $n$  is the transformer turns ratio:

$$\omega_r = 1/\sqrt{L_r \cdot C_r}, \quad f_r = 1/T_r = \omega_r/(2\pi) \quad (1)$$

$$Z_r = \sqrt{L_r/C_r} \quad (2)$$

$$r = (n^2 R) / Z_r \quad (3)$$

$$A = V_O/V_S, \quad B = n \times A. \quad (4)$$

The Equivalent Circuits Of The HI-Swrc Operating Modes Along With Its Typical Waveforms At The Steady-State Are Presented In Fig. 2. Assume That Prior To Mode I, the resonant current  $i_r$  is zero, the resonant voltage  $v_r$  is  $2V_S - nV_O$ , and all of the switches are off. The converter has four operating modes as follows:

*Mode I* ( $t_1 - t_2$ ): At  $t_1$ ,  $Q_2$  is turned on at ZCS and a resonance starts between  $C_r$  and  $L_r$  until  $v_r$  reaches  $-nV_O$  at  $t_2$ .

$$v_r(t) = (2V_S - nV_O) \cdot \cos(\omega_r \cdot (t - t_1)) \quad (5)$$

$$i_r(t) = -\frac{2V_S - nV_O}{Z_r} \sin(\omega_r(t - t_1)) \quad (6)$$

$$t_2 - t_1 = \frac{1}{\omega_r} \left[ \pi - \cos^{-1} \frac{B}{2 - B} \right] \quad (7)$$

$$i_r(t_2) = -\frac{2V_S}{Z_r} \sqrt{1 - B}. \quad (8)$$

*Mode II* ( $t_2 - t_3$ ): At  $t_2$ ,  $D_r$  starts conducting at ZVS, and  $D$  is turned on (in a non-ideal situation,  $D$  is turned on at ZCS due to the transformer leakage inductance). As a result, the energy stored in  $L_r$  begins transferring to the load. The magnitude of  $i_r$  decreases linearly until at  $t_3$  it reaches zero. At this time,  $Q_2$ ,  $D_r$  and  $D$  are turned off at ZCS.

$$i_r(t) = i_r(t_2) + \frac{nV_O}{L_r}(t - t_2) \quad (9)$$

$$t_3 - t_2 = \frac{2}{\omega_r} \cdot \frac{\sqrt{1 - B}}{B}. \quad (10)$$

*Mode III* ( $t_3 - t_4$ ): At  $t_3$ ,  $Q_1$  is turned on at ZCS due to  $L_r$ . As a result,  $D$  becomes forward biased at ZCS. A part of the energy drained from the input voltage source charges  $C_r$  through a resonance with  $L_r$ , and its remaining part is delivered to the output. At  $t_4$ ,  $i_r$  has reached zero and thus  $Q_1$  and  $D$  are turned off at ZCS. At this time  $v_r$  has reached  $2V_S - nV_O$ .

$$v_r(t) = V_S - nV_O - V_S \cos(\omega_r \cdot (t - t_3)) \quad (11)$$

$$i_r(t) = \frac{V_S}{Z_r} \cdot \sin(\omega_r \cdot (t - t_3)) \quad (12)$$

$$t_4 - t_3 = T_r/2. \quad (13)$$

*Mode IV* ( $t_4 - t_5$ ): In this mode all of the semiconductor devices are off and the load is supplied by the output capacitor. The duration of this interval is determined by the controller so that proper voltage regulation is attained (dead-time control).

According to (7), (8) and (10),  $B$  should be less than unity. In other words, if this condition ( $B \leq 1$ ) is not met, the power cannot be delivered to the load.

At the steady-state, the converter voltage gain  $A$  can be calculated by satisfying the energy-balance rule in one switching cycle. By defining  $\varepsilon_{in}$  and  $\varepsilon_{out}$  as the converter input energy and output energy in one switching cycle, the following relations are established:

$$\begin{cases} \varepsilon_{in} = \int_{t_3}^{t_4} V_S \cdot i_r(t) dt = 2C_r V_S^2 \\ \varepsilon_{out} = \frac{1}{R} \int_{T_S} v_O^2 dt \cong \frac{V_O^2 T_S}{R} \end{cases} \quad (14)$$

By defining  $S$  (scale) as in (15), the converter normalized voltage gain  $B$  is obtained as in (16).

$$S = 2(n^2 R) C_r f_S = \frac{r}{\pi} \cdot \frac{f_S}{f_r} \quad (15)$$

$$\varepsilon_{in} = \varepsilon_{out} \Rightarrow B = \sqrt{S}. \quad (16)$$

In the absence of dead-time (Mode IV), the converter operates at its maximum power handling capability where the switching frequency is also at maximum. This situation is called the Maximum Power Delivery Condition [10]. The subscript 'm' is used to denote the quantities in this condition. The interval from  $t_1$  to  $t_4$  is defined as  $T_m$ . By using (7), (10) and (13):

$$\frac{T_m}{T_r} = 1 + \frac{1}{2\pi} \left[ \frac{2\sqrt{1 - B}}{B} - \cos^{-1} \frac{B}{2 - B} \right]. \quad (17)$$

By substituting  $T_S = T_m$  into (15), (18) is attained. This equation is required for converter design. E.g., for  $n^2 \times R = Z_r$  ( $r = 1$ ), a value of  $B_m$  is obtained that is almost equal to 0.5 which shows the maximum achievable voltage gain in this case.

$$r = B_m^2 \cdot \left[ \pi + \frac{\sqrt{1 - B_m}}{B_m} - \frac{1}{2} \cos^{-1} \frac{B_m}{2 - B_m} \right]. \quad (18)$$

When the converter output is short circuited,  $B$  is zero. Therefore, according to (17)  $T_m$  is infinite which means that in this condition power transferring is automatically stopped (self short-circuit protection).

By defining  $V_D$  as the diodes forward drop-voltage and  $V_{CE,SAT}$  as the IGBTs saturation voltage, the converter efficiency  $\eta$  is given by (19). The other elements are assumed to be ideal. In this equation,  $H_D$  and  $H_I$  represent the loss coefficients of the diodes and the IGBTs respectively [10]. The expressions of  $H_D$  and  $H_I$  are presented in Table I.

$$\eta = 1 - \frac{V_D}{V_O} \cdot H_D - \frac{V_{CE,SAT}}{V_O} \cdot H_I. \quad (19)$$

### III. TRANSFORMER EFFECTS

The equivalent circuit of a HL-SwRC is shown in Fig. 3 where the transformer model is applied.  $L_1$  and  $L_2$  are the leakage inductances, and  $L_m$  is the magnetizing inductance of the transformer.  $L_S$  is the transformer inductance looking into the primary when the secondary winding is short-circuited, and is given by (20).

$$L_S = L_1 + L_2 \parallel L_m. \quad (20)$$

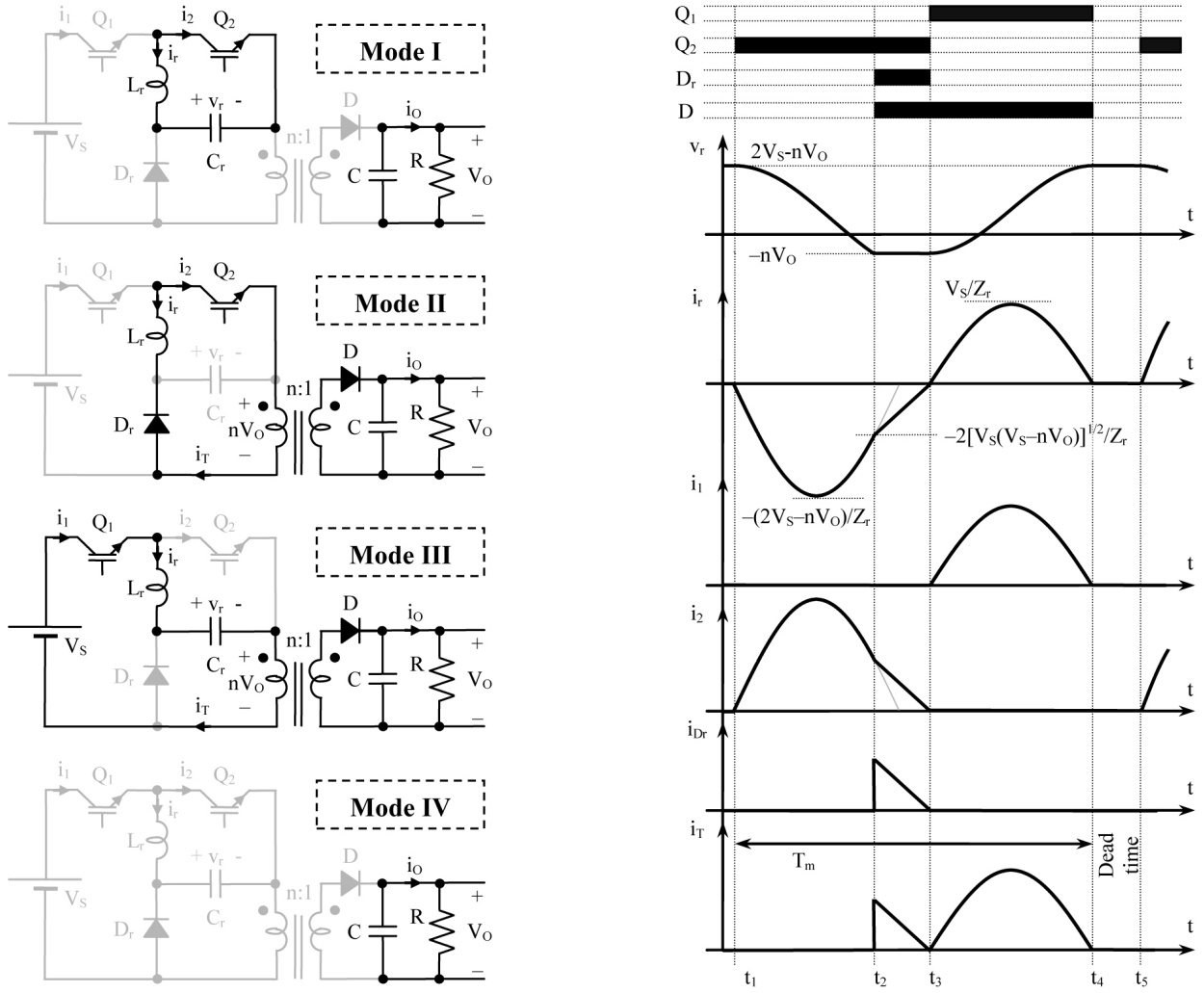


Fig. 2. Equivalent circuits and typical steady-state waveforms of HL-SwRC.

Similar to the ideal situation, by turning  $Q_2$  on, the voltage polarity of  $C_r$  starts reversing until at  $t_2$  it reaches  $-nV_O$  and then  $D_r$  and  $D$  start conducting. However, due to the transformer leakage inductance,  $v_r$  is not clamped at  $-nV_O$ . During  $t_2$  to  $t_3$ , a part of the energy stored in  $L_r$  increases the magnitude of  $v_r$  to  $nV_O + \Delta V$ . By turning  $Q_2$  off under ZCS at  $t_3$ , the transformer current  $i_T$  continues through  $C_r$ . When  $Q_1$  is turned on at  $t_3$ , energy is transferred from the input voltage source to the output and it simultaneously charges  $C_r$ . The duration of this interval becomes more than  $T_r/2$  because  $L_S$  increases the effective value of the resonance inductor to  $L_r + L_S$ . Consequently, the peak of  $i_1$  is also decreased because the characteristic impedance of the resonant tank ( $Z_r$ ) has increased. According to the equivalent circuits shown in Fig. 3, approximately  $nV_O$  is placed across  $L_m$  during  $t_2$  to  $t_4$ . By turning  $Q_1$  off at  $t_4$ ,  $i_m$  continues through  $C_r$  and  $D_r$ , and thereby a negative voltage equal to  $-v_r(t_4)$  is placed across  $L_m$ . Therefore, the transformer core is reset at  $t'_4$ . In fact,  $v_r(t'_4)$  is a bit greater than  $v_r(t_4)$ , or in other words, the energy stored in the transformer core is recovered. During  $t'_4$  to  $t_5$  the magnetizing current  $i_m$  cannot become negative due to  $D_r$ . Since in this procedure, the voltage  $v_r$  reaches the

constant value of  $-nV_O$  at  $t_2$ , the instant  $t_2$  is a fixed point of operation and thus stability is guaranteed.

#### IV. EXPERIMENTAL RESULTS

The experimental results of a 210W HL-SwRC prototype for  $V_S=156V \pm 20\%$  and  $V_O=60V$  are presented in this section. The specifications of the employed transformer are  $n=1.85$ ,  $L_m=8mH$ , and  $L_S=18\mu H$ . The values of the resonant tank components are  $L_r=7.4\mu H$  and  $C_r=100nF$  where a 20% overdesign is considered. The switches are IXRP15N120, the diode  $D_r$  is a BYT52, and the rectifying diode  $D$  is a MUR840. A guard-time of about  $1\mu s$  is placed between the turn off instant of  $Q_2$  and the turn on instant of  $Q_1$ . The switching operation of the HL-SwRC for  $V_S=156V$  and  $P_{out}=210W$  are shown in Fig. 4. The voltage spikes that appeared across the switches during guard-time are due to the parasitic output capacitance of the switches. This phenomenon also exists in series-resonant converters and can be resolved easily by placing a small RCD snubber across the switches if it is deemed necessary [4]. The soft-switching operations of  $Q_2$  and  $Q_1$  are shown in Figs. 5 and 6 respectively. According to these figures, both switches are turned on and turned off under

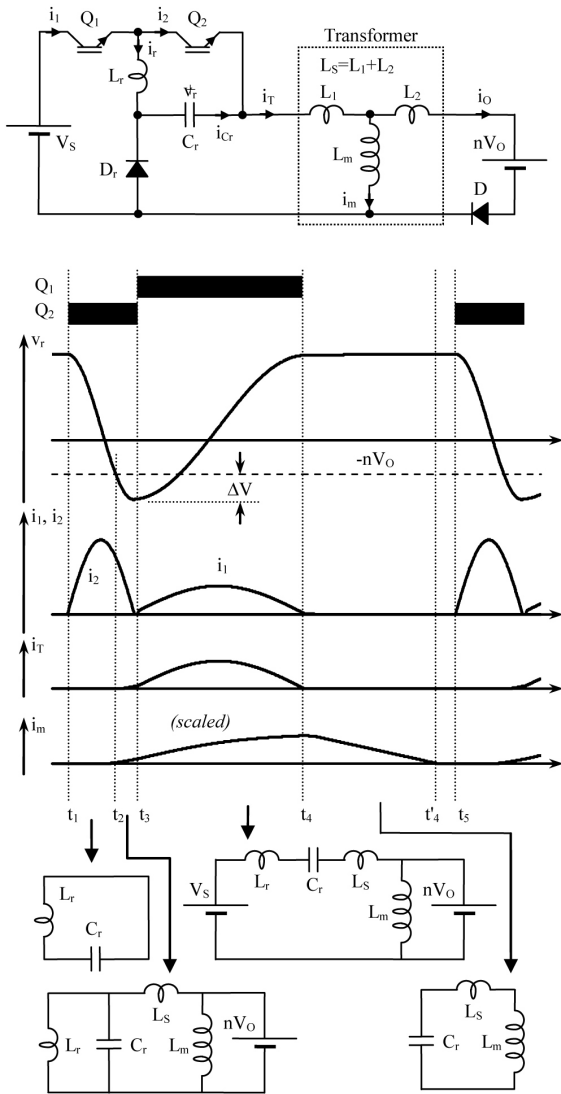


Fig. 3. HL-SwRC with the transformer model and its typical waveforms.

the ZCS condition. The current of the transformer’s secondary winding ( $i_D$ ) along with the output voltage ripple are illustrated in Fig. 7, and the converter efficiency at the nominal input voltage is presented in Fig. 8. The conduction losses of the rectifying diode are responsible for a 3% efficiency degradation.

V. SYNTHESIS OF GROUP H

A general synthesis scheme for the proposed converters is presented in Fig. 9. In this figure, the two unidirectional switches  $Q_1$  and  $Q_2$  along with the output capacitor  $C$  construct the frame circuit [10]. The frame is a fixed circuit and its obligation is to switch the resonator alternatively. The four nodes S (source), M (middle), L (load), and G (ground) belong to the frame circuit. The voltage source  $V_S$  is always connected to the nodes S and G. The other part of the converter is a resonator where the capacitor  $C_r$  along with the inductor  $L_r$  create a series resonant tank, and either a diode  $D_r$  or a unidirectional switch  $Q_r$  stabilizes converter operation. Either pin of each resonator element is connected to the node J (joint)



Fig. 4. Switching operation of HL-SwRC, respectively from top:  $V_{CE}$  of  $Q_2$ ,  $I_c$  of  $Q_2$ ,  $V_{CE}$  of  $Q_1$ , and  $I_C$  of  $Q_1$ . Scales:  $2\mu\text{s}/\text{div}$ ,  $20\text{A}/\text{div}$ ,  $200\text{V}/\text{div}$ .

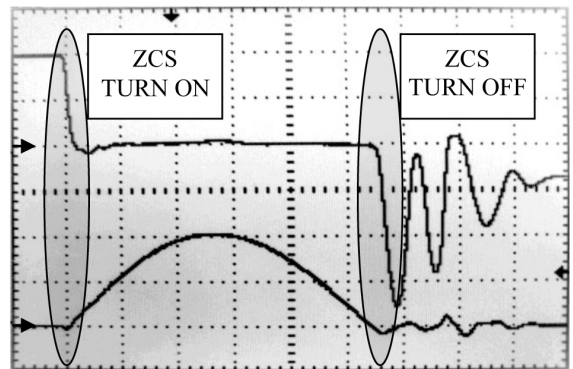


Fig. 5. Soft-Switching operation of  $Q_2$ , respectively from top: collector-emitter voltage and collector current. Scales:  $500\text{ns}/\text{div}$ ,  $10\text{A}/\text{div}$ ,  $80\text{V}/\text{div}$ .

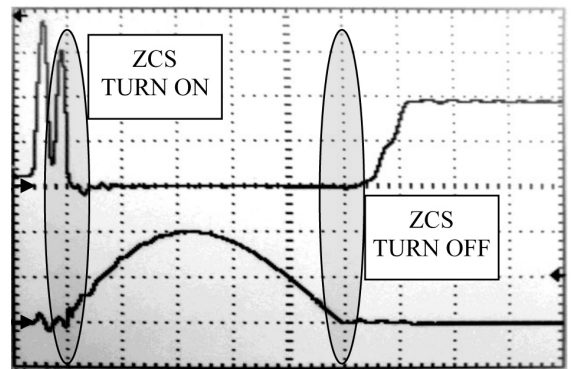


Fig. 6. Soft-Switching operation of  $Q_1$ , respectively from top: collector-emitter voltage and collector current. Scales:  $1\mu\text{s}/\text{div}$ ,  $5\text{A}/\text{div}$ ,  $80\text{V}/\text{div}$ .

[10]. The transformer intersects the frame circuit, and the diode  $D$  is used as a half-wave rectifier. The derived functional topologies are designated as group H, where H denotes the manner of rectifying as half-wave.

By applying a diode to the resonator network, the 2-switch topologies (half-bridge) HL, HG, and HS-SwRC are created. The topology of the HL-SwRC was already shown in Fig. 1, and the topologies of the HG and the HS-SwRC are presented in Fig. 10. In these topologies, the first letter, H, refers to the group name, and the second letter shows the node that  $C_r$

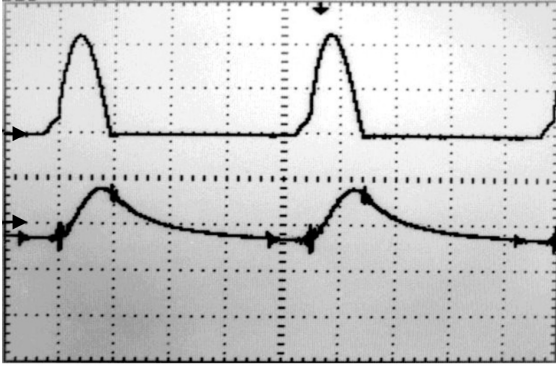


Fig. 7. Transformer secondary winding current (top), and output voltage ripple (bottom)  
Scales:  $5\mu\text{s}/\text{div}$ ,  $10\text{A}/\text{div}$ ,  $1\text{V}/\text{div}$ .

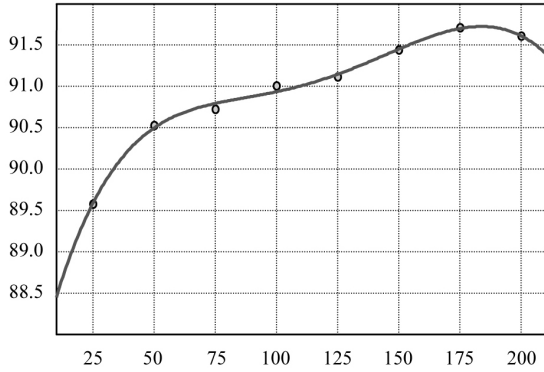


Fig. 8. The converter efficiency (%) versus output power (W) at nominal input voltage (156V).

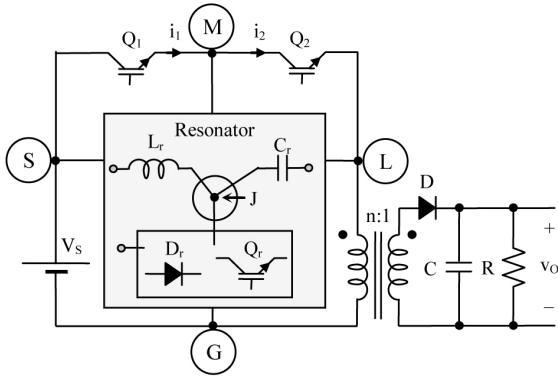


Fig. 9. General synthesis of topologies of group H.

is connected to. The 3-switch topologies (3/4-bridge), HGL and HLG-SwRC, are formed when a switch is applied to the resonator network as shown in Fig. 10. The letter H shows the group as well, and the second and third letters refer to the nodes that  $L_r$  and  $Q_r$  are connected to respectively. In these topologies, the switch  $Q_r$  is gated simultaneously with one of the frame switches as shown by the dashed-line. This is similar to a full-bridge inverter in which two diagonal switches are turned on simultaneously.

In the HG and HS SwRC, it is necessary to employ another capacitor ( $C_1$ ), as shown in Fig. 10, in order to provide the required current loop for a transformer reset. This capacitor

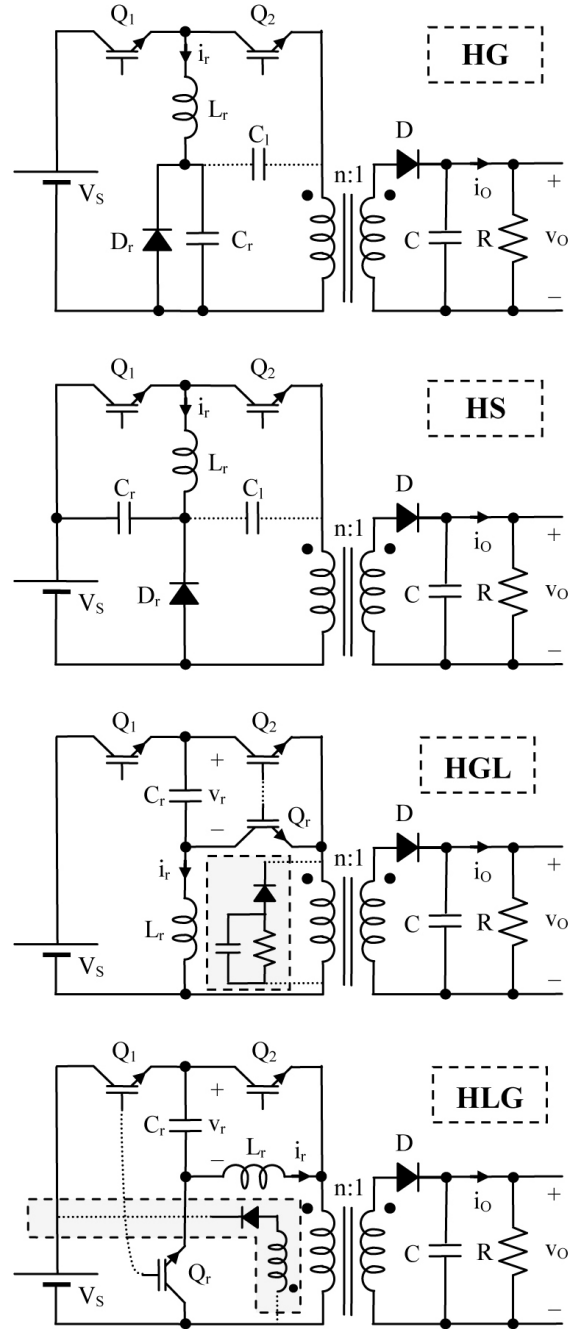


Fig. 10. General synthesis of topologies of group H.

can be much smaller than the main resonance capacitor ( $C_r$ ). In 3-switch topologies, such as the HLG-SwRC, the stored energy in the transformer core can be recovered by a tertiary winding similar to a forward converter. The maximum amount of energy is stored in  $L_m$  ( $\varepsilon_m$ ) under the worst conditions is as (21). According to this equation, the stored magnetic energy in the transformer is much lower than the transferred energy (easily less than 1%). As a result, a small clamp circuit can also be placed in parallel with the transformer's primary side to absorb  $\varepsilon_m$  as shown for the HGL-SwRC.

$$\max \left\{ \frac{\varepsilon_m}{\varepsilon_{out}} \right\} = \frac{\pi^2}{4} \times \frac{L_r}{L_m}. \quad (21)$$

For all members of group H, the voltage gain is obtained from (16), efficiency is as (19), and (18) gives the maximum attainable voltage gain. The other specifications are presented in Table 1. According to this table, the resonance voltage swing is between 0 to  $2V_S$  (always positive) for the HG and HGL-SwRC. Therefore, these topologies are appropriate for high power and/or low switching frequency converters in which  $C_r$  is obtained in the range of micro-Farad and electrolytic capacitors are employed. The swing of  $v_r$  is between  $-V_S$  to  $+V_S$  in the HS and HLG SwRC. Thus, these topologies are suitable for high frequency converters in which  $C_r$  is attained in the range of nano-Farad and bipolar capacitors such as the MKP types are used. According to the column of  $H_D$ , the 3-switch topologies have better efficiency than the 2-switch topologies. In general, the operation of these converters is the same as that of the non-isolated topologies [10].

## VI. COMPARISON

The presented circuits are resonant converters containing a 1/2 or 3/4-bridge inverter and an LC resonant tank that provide the ZCS condition. Among the various resonant converters presented in the literature, the well-known series-resonant converter (SRC) has the nearest structure and operation to the proposed converters [1], [4], [8], [9]. Two conventional SRCs are the half-bridge (HB) and full-bridge (FB) types. In these converters, the output section is either a transformer with a single output winding connected to a FB rectifier, or a transformer with two output windings (center-tapped) and two rectifying diodes. The former case leads to a smaller transformer, which is at the expense of higher conduction losses due to the fact that the two diodes are placed simultaneously in the output current path. For the first comparison, the transformer in the proposed converters has only one output winding and only one rectifying diode is required. The complete ZCS condition at the turn on and turn off instants is attained by the HB- and FB-SRC only when these converters operate in DCM ( $f_s < f_r/2$ ) in which  $B_m$  is limited to 1/2 and 1 respectively [1]. The HB-SRC is not recommended for high-power applications because only one half of the source voltage is applied in each switching interval. Since in the proposed converters, the power is drained from the entire  $V_S$ , and  $B_m$  is limited to 1, another attractive advantage appears. The proposed converters are similar to the FB-SRC but with a smaller a fewer number of switches and diodes. The proposed 3-switch converters can be viewed as 3/4-bridge topologies. The efficiency of the FB-SRC can also be written as (19) which is the same as that of the proposed converters  $H_I = (1+B)/n$  (see Table 1), but  $H_D$  is now given by (22). In this equation,  $k=1$  if the transformer has two output windings, and  $k=2$  if the transformer has one output winding.

$$H_D = k + \frac{1-B}{n}, \quad k = 1 \text{ or } 2. \quad (22)$$

Therefore, for a specific design, the switches conduction losses in a FB-SRC and in the proposed converters are equal. The diodes conduction losses ( $H_D$ ) in the proposed 3/4-bridge

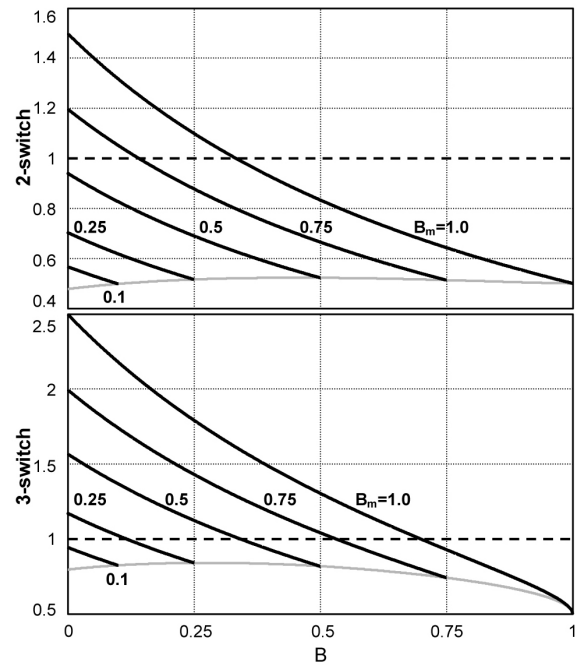


Fig. 11. Comparison of current stresses with FB-SRC.

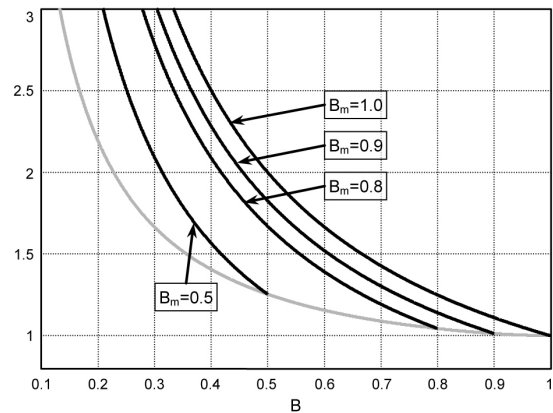


Fig. 12. Comparison of output voltage ripple with FB-SRC.

topologies are always less than those of the FB-SRC (4/4-bridge) even if the transformer of the FB-SRC has two output windings. For this transformer, the  $H_D$  of the FB-SRC is equal to the  $H_D$  of the proposed 2-switch topologies. For a specific design, the switches current stresses of the proposed converters and those of the FB-SRC are compared in Fig. 11. Since in the proposed converters the switches peak currents are different, the mean of the switches current stresses are considered to be  $((\text{stress of } Q_1 + \text{stress of } Q_2)/2)$ . In a proper design, the maximum attainable normalized voltage gain is chosen as  $B_m \cong 1$  in order to increase the efficiency and reduce the current stresses. When the input voltage variations are low,  $B$  is also around  $B_m$ . Hence the sum of the current stresses created in the proposed converters are about half of the FB-SRC. This is due to the fact that in a SRC a part of the energy stored in the resonant tank is returned to the source via the switches anti-parallel diodes. In SRCs, the voltage stresses of all of the switches are  $V_S$ , which is similar to either  $Q_1$

TABLE I  
SPECIFICATIONS OF GROUP H

Topology	$v_r^\dagger$		$H_D$	Voltage stress <sup>†</sup>			Current Stress <sup>‡</sup>			Peak of $i_r^\ddagger$		$H_I$
	min	max		$Q_1$	$Q_2$	$D_r/Q_r$	$Q_1$	$Q_2$	$D_r/Q_r$	min	max	
HG	0	2	$1 + \frac{1-B}{n}$	1	$2-B$	2	1	$2-B$	$2\sqrt{1-B}$	1	$2-B$	$\frac{1+B}{n}$
HS	1	1										
HL	$B$	$2-B$										
HGL	0	2										
HLG	1	1										

<sup>†</sup> Absolute value and normalized to  $V_S$

<sup>‡</sup> Absolute value and normalized to  $V_S/Z_r$

or  $Q_2$  in the proposed converters (see Table 1). The voltage stresses of the other frame switch are  $(2-B) \times V_S$  which is again around  $V_S$  in a proper design ( $B \approx B_m \cong 1$ ). In the 3-switch topologies, the voltage stress of  $Q_r$  is  $2V_S$ , however this issue is not restrictive for most applications. The output voltage ripple of the proposed converters is compared to that of the FB-SRC in Fig. 12. As shown in this figure, although a half-wave rectifier is employed in the proposed converters and a full-wave rectifier is used in the FB-SRC, the output voltage ripple of the presented converters is almost equal to that of the FB-SRC in a proper design ( $B \approx B_m \cong 1$ ).

## VII. CONCLUSIONS

Some basic isolated topologies of the switched resonator converter family are presented in this paper and designated as group H. All of the topologies were synthesized according to special structural rules. Some advantages of the proposed converters are, optimization ability due to topology variety, independent soft-switching condition for all of the active elements, and self short-circuit protection. In addition, all of the parasitic elements including the transformer leakage inductance are absorbed. A comparison with conventional resonance converters shows outstanding advantages such as a lower number of switches and diodes, a smaller transformer, higher efficiency, and lower current stresses. Experimental results from a 210W laboratory prototype confirm the integrity of the proposed converters and their theoretical analysis.

## REFERENCES

- [1] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed., John Wiley & Sons, 2002.
- [2] Y. Gu., Z. Lu, Z. Qian, X. Gu, and L. Hang, "A novel ZVS resonant reset dual switch forward DC-DC converter," *IEEE Trans. Power Electron.*, Vol. 22, No. 1, pp. 96-103, Jan. 2007.
- [3] Y. Xi, and P. K. Jain, "A forward converter topology employing a resonant auxiliary circuit to achieve soft switching and power transformer resetting," *IEEE Trans. Ind. Electron.*, Vol. 50, No. 1, pp. 132-140, Feb. 2003.
- [4] G. Ivensky, I. Zeltser, A. Kats, and S. Ben-Yaakov, "Reducing IGBT losses in ZCS series resonant converters," *IEEE Trans. on Ind. Elect.*, Vol. 46, No. 1, pp. 67-74, Feb. 1999.
- [5] C. Klumpner, and F. Blaabjerg, "Using reverse blocking IGBTs in power converters for adjustable speed drives," in *Proc. IEEE IAS Annu. Meeting*, Vol. 3, pp. 1516-1523, Oct. 2003.
- [6] J. Itoh, I. Sato, A. Odaka, H. Ohguchi, H. Kodachi, and N. Eguchi, "A novel approach to practical matrix converter motor drive system with reverse blocking IGBT," *IEEE Trans. Power Elect.*, Vol. 20, No. 6, Nov. 2005.
- [7] D. Zhou, K. Sun, Z. Liu, L. Huang, K. Matsuse, and K. Sasagawa, "A novel driving and protection circuit for reverse-blocking IGBT used in matrix converter," *IEEE Trans. Ind. Appl.*, Vol. 43, No. 1, Jan./Feb. 2007.

- [8] V. Vorperian, and S. Cuk, "A complete DC analysis of the series resonant converter," *IEEE Power Electronics Specialist Conf. 1982 Rec.*, pp. 85-100, 1982.
- [9] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Trans. on Power Electronics*, Vol. 3, No. 2, pp. 174-182, Apr. 1988.
- [10] M. Jabbari, and H. Farzanehfard, "Family of soft switching resonant DC-DC converters," *IET Power Electron.*, Vol. 2, Issue 2, pp. 113-124, 2009.
- [11] M. Jabbari, "Resonant Inverting-Buck Converter," *IET Power Electronics, to be published*.
- [12] M. Jabbari, and H. Farzanehfard, "A new soft-switching step-down/up converter with inherent PFC performance," *Journal of Power Electronics*, Vol.9, No.6, pp. 835-844, Nov. 2009.
- [13] M. Jabbari, and H. Farzanehfard, "New resonant step-down/up converters," *IEEE Trans. on Power Electronics*, to be published.
- [14] M. Jabbari, H. Farzanehfard, and S. Farhangi, "A new resonant step-up converter based on unidirectional switches," *IEEE ECON'09*, pp. 862-865, Saint-Petersburg, Russia, 2009.
- [15] J.-H. Jung, J.-M. Choi, and J.-G. Kwon, "Design methodology for transformers including integrated and center-tapped structures for LLC resonant converters," *Journal of Power Electronics*, Vol. 9, No. 2, pp.215-223, Mar. 2009.



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