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A Novel Interleaving Control Scheme for Boost Converters Operating in Critical Conduction Mode

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Abstract

Interleaving techniques are widely used to reduce input/output ripples and to increase the power capacity of boost converters operating in critical conduction mode. Two types of phase-shift control schemes are studied in this paper, the turn-on time shifting method and the turn-off time shifting method. It is found that although the turn-off time shifting method exhibits better performance, it suffers from sub-harmonic oscillations at high input voltages. To solve this problem, an intensive quantitative analysis of the sub-harmonic oscillation phenomenon is made in this paper. Based upon that, a novel modified turn off time shifting control scheme for interleaved boost converters operating in critical conduction mode is proposed. An important advantage of this scheme is that both the master phase and the slave phase can operate stably in critical conduction mode without any oscillations in the full input voltage range. This method is implemented with a FPGA based digital PWM control platform, and tests were carried out on a two-phase interleaved boost PFC converter prototype. Experimental results demonstrated the feasibility and performance of the proposed phase-shift control scheme.

Key Words: Critical conduction mode, Interleaving, Phase shift, Sub-harmonic oscillation

I. INTRODUCTION

Boost converters operating in critical conduction mode (CRM) can achieve zero current switching (ZCS) for the diode and eliminate its reverse recovery loss, which enables the application of a low cost silicon PiN diode while still keeping switching losses low. However, in this operation mode, the switching frequency is variable and thus the current/voltage ripple of converters with CRM is higher than it is in converters with continuous conduction mode (CCM). This is generally undesirable for high power and power factor correction applications [1]–[3]. Therefore, in many high power applications, multiple phase boost converters are often adopted in order to increase the power capacity and interleaving operation is used to cancel the current ripple and reduce the volume of the input EMI filter. Meanwhile, the input/output current/voltage ripple can still be minimized without sacrificing efficiency [4]–[6].

It is well known that, it is not difficult to achieve interleaving control for converters operating at a constant frequency. However, it is difficult to generate gate signals for converters operating in CRM. Traditionally, there are two types of interleaving control schemes, the turn-on time shifting method and the turn-off time shifting method [7]–[10]. With the turn-on time shifting method, a boost converter operated in the slave phase may turn on before the inductor current reaches zero, and it may lose ZCS for the diode. Thus the turn-off time shifting method appears to be a better choice since both the master phase and the slave phase can be worked with CRM operation which guarantees ZCS operation for the diode in any case. However, a so-called sub-harmonic oscillation phenomenon occurs at high line voltages for this operating mode.

One solution is to add a transformer in order to increase the output voltage. However, the objectives of high power density and low cost will not be accomplished. For this reason and, in order to maintain the high efficiency of the converter, a complete analysis of the sub-harmonic oscillation phenomenon is made in this paper. Then a novel modified turn off time phase-shift interleaving control scheme is proposed. A distinguished feature of the proposed scheme is that the slave phase can operate in the critical conduction mode and the phase-shift is nearly $360^\circ/N$. (N is the number of phases in parallel.)

In addition, since a phase-shift control scheme is usually realized by analog circuits, the solution for an ideal phase-shift will inevitably lead to a complex analog control circuit. In this paper, a digital PWM control circuit based on a FPGA is used to implement the control scheme, which greatly simplifies the design process. The experimental results of a two-phase interleaved CRM boost PFC are presented to verify the feasibility and performance of the novel phase-shift control scheme.

This paper is organized as follows: first, an evaluation of existing control schemes is introduced for interleaved boost converters operating in critical conduction mode in section II. In section III, an analysis of the sub-harmonic oscillation

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problems in turn off time shifting control is made in detail. The derivation of the proposed control scheme for phase-shift is given in section IV. Finally, in section V, the proposed control scheme is implemented and verified in a boost PFC rectifier.

II. EVALUATION OF EXISTING CONTROL SCHEMES

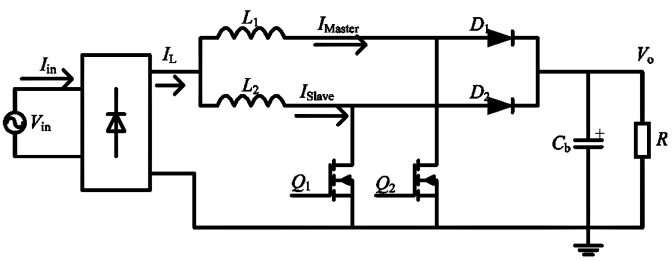
The system configuration of a two-phase interleaved CRM boost PFC converter and its key waveforms are shown in Fig. 1. The switch is turned on when the inductor current reaches zero. The turn-on time is controlled to be constant. Because of the high current/voltage ripple, interleaving operation is usually used to damp the current and voltage stress.

In this section, two types of existing interleaving control schemes are discussed. The interleaving control scheme shown in Fig. 2 shifts the turn-on signal to achieve interleaving operation. The scheme shown in Fig. 3 shifts the turn-off signal and the slave phase turns on when the inductor current becomes zero. For converters with a constant frequency, it is easy to determine the phase-shift interval. For a two-phase boost converter with CRM operation, the operation is varying. The interleaving signal can be generated from the turn-on signal P_1 or the turn-off signal P_2 by shifting these signals with $T_s/2$ or $T_s'/2$. The master phase is turned on by zero current detectors and turned off by a variable on-time controller. We assume that the difference between the two adjacent operation periods can be omitted. As a result, we can use the previous operation period to determine the present shift period. For high frequency operation, this assumption is feasible.

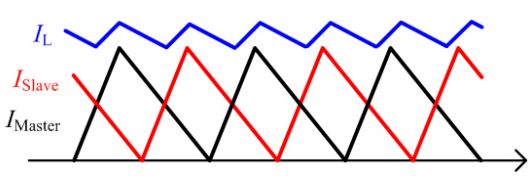
A. Type I Phase shift method

As shown in Fig. 2, the slave phase is turned on by shifting the turn-on signal P1, which is generated from the master phase and always lagging the master phase by 180°. The turn-on time of the master phase and the slave phase are equal.

With this phase-shift method, the slave phase may work in CCM or DCM mode, since the turn-on signal may not occur while the inductor current of the slave phase drops to zero.



(a) System configuration



(b) Key waveforms

Fig. 1. System diagram and its key waveforms of a two-phase interleaved CRM boost PFC.

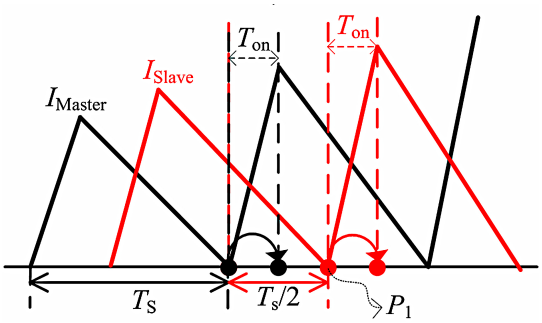


Fig. 2. Shifting turn-on signal to achieve interleaving operation.

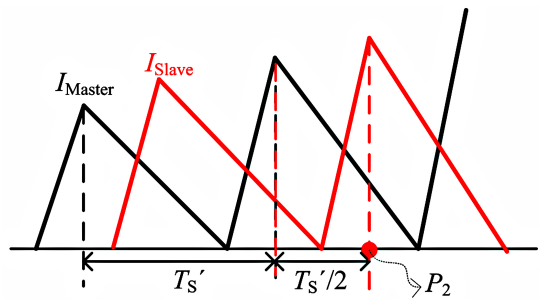


Fig. 3. Shifting turn-off signal to achieve interleaving operation.

B. Type II Phase shift method

As shown in Fig. 3the slave phase is turned on by a zero current detector signal but turned off by shifting the turn-off signal P2, which is generated from the master phase and always lagging the master phase by 180°.

With this phase-shift method, both the master phase and the slave phase can work in CRM mode.

For an interleaved CRM boost converter, P_2 is a better choice for a converter in the slave stage, since it requires a zero voltage detector to generate a turn-on signal and can insure the soft-switching feature. As for P_1, the slave stage may not turn on with soft-switching.

However, when using the type II phase shift method to achieve interleaving operation, the inductor current of the slave phase exhibits a sub-harmonic oscillation phenomenon at high line voltage. The turning-on time of the slave phase is not equal to the master phase anymore. Both the simulation and experimental results proved it, as shown in Fig. 4.

III. PERFORMANCE ANALYSIS

An ideal instance of the type II phase-shift control scheme is when the turning-on period of the slave phase is equal to the master phase. However, if a disturbance at the input voltage or the output voltage occurs, then there will be a ΔT_{on} between the actual and ideal turning on period. The inductor current waveforms are illustrated in Fig. 5. I_{Master} is the master phase inductor current waveform, I_{Slave} is the ideal slave phase inductor current waveform and I'_{Slave} is the actual slave phase inductor current waveform after a disturbance ΔT_{on}. Fig. 5(a) and Fig. 5(b) are two different instances after a disturbance. In Fig. 5(a), the slave inductor current begins oscillation and is unstable. In Fig. 5(b), the slave inductor is gradually becoming stable.

If the slave current I'_{Slave} is stable, ΔT_{on} should be convergent, as shown in Fig. 5(b). When the switches are turning on, the inductor currents are increasing at the same rate. When the switches are turning off, the inductor currents are decreasing at the same rate. The rising and falling slope of the inductor current can be calculated form Fig. 5:

$$S_n = \frac{U_{in}}{L} \tag{1}$$

$$S_f = \frac{U_{in} - U_o}{L}. \tag{2}$$

So we can get

$$\left| \frac{\Delta T_{on}{}'}{\Delta T_{on}} \right| = \frac{U_{in}}{U_o - U_{in}} < 1. \tag{3}$$

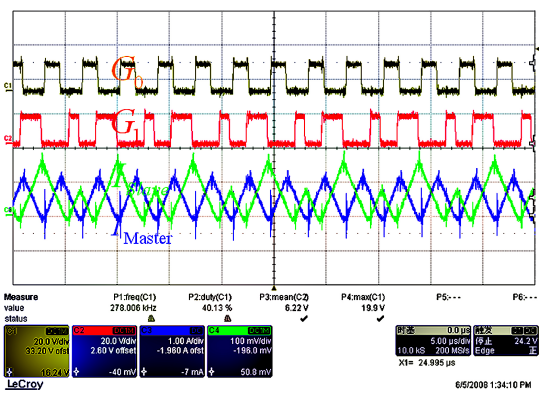
Then

$$U_{in} < \frac{1}{2} U_o. \tag{4}$$

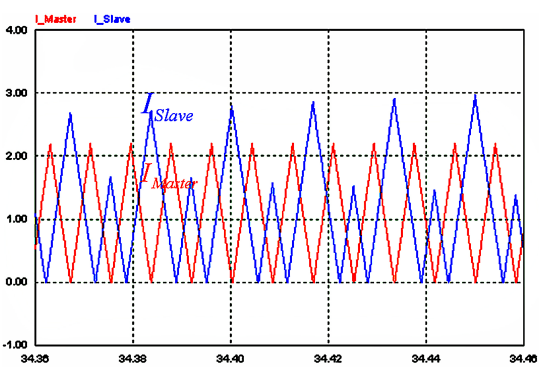
This relationship can also be derived according to the magnetic flux balance of the boost inductors:

$$\frac{U_o}{U_{in}} = \frac{2}{1-D} \tag{5}$$

$$D = 1 - \frac{2U_{in}}{U_0}. \tag{6}$$

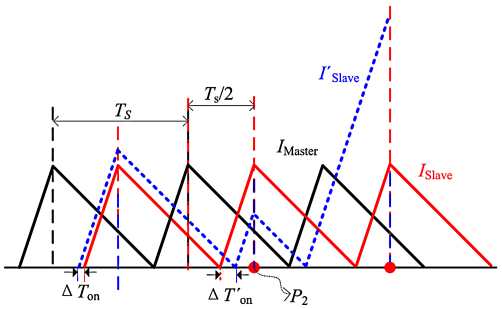


(a) Experimental waveforms of inductor currents I_{Master} and I_{Slave}, and gate signals G_0 and G_1

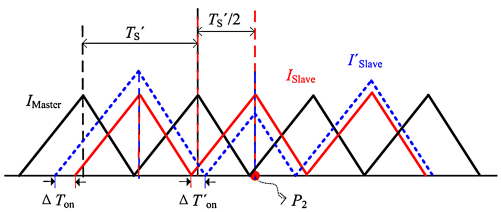


(b) Simulation waveforms of inductor currents I_{Master} and I_{Slave}

Fig. 4. Sub-harmonic oscillation phenomenon.



(a) $D < 0.5$



(b) $D > 0.5$

Fig. 5. The inductor currents after a disturbance ΔT_{on}.

Because $D \leq 1$, hence

$$U_0 \geq \frac{1}{2} U_{in}. \tag{7}$$

This equation shows that the output voltage should be at least two times the input voltage. So if the type II phase shift method is adopted, a sub-harmonic oscillation is unavoidable when $U_{in} > 0.5U_o$, as it is shown in Fig. 5(a).

In this paper, a simple control scheme is proposed for a two-phase boost converter. The theory behind this control method and its operation modes will be explained below.

IV. PROPOSED PHASE-SHIFT INTERLEAVING CONTROL SCHEME

In order to solve this problem and utilize the advantages of the shifting turn-off signal method, this paper gives a complete analysis of the sub-harmonic oscillation phenomena in section III. Moreover, a novel phase-shift interleaving control scheme is proposed.

In peak current mode control, we adopt ramp compensation to keep the current stable and to avoid sub-harmonic oscillation. Actually, ramp compensation sacrifices the power factor to achieve a stable current. Similarly we can change the interleaving method to keep ΔT_{on} convergent.

From the previous analysis, we can see that ZVS, the 180° phase shift and stability can not all be obtained in one design. Since ZVS is the main feature of this method, so in order to achieve stability, the 180° phase shift should be sacrificed. To illustrate the operation process, the main waveforms are shown in Fig. 6 and Fig. 7, respectively.

When the type I phase shift method is adopted, just as the I'_{Slave}, the turning-on period of the slave phase after a disturbance is:

$$T_{on\_slave} = \Delta T_{on} + T_{on}. \tag{8}$$

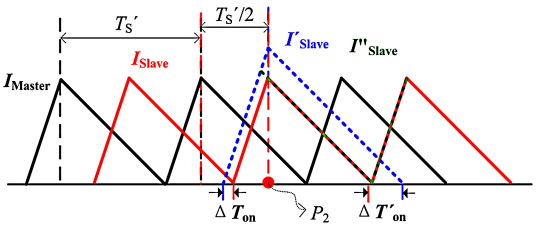


Fig. 6. Waveforms of I_{Master}, I_{Slave}, I'_{Slave} and I''_{Slave}.

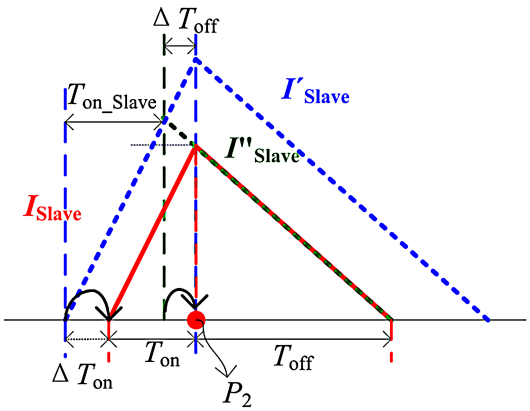


Fig. 7. Waveforms of I_{Slave}, I'_{Slave} and I''_{Slave}.

The disturbance after a switching cycle is

$$|\Delta T_{on}{}'| = \frac{U_{in}}{U_o - U_{in}}|\Delta T_{on}|. \tag{9}$$

If we want to keep $\Delta T_{on}{}' = 0$, just like the I''_{Slave}, as shown in Fig. 6, then the turning-on period of the slave phase is

$$T_{on\_slave} = T_{on\_master} + \Delta T_{on} - \Delta T_{off} = D \cdot \Delta T_{on} + T_{on} \tag{10}$$

$$D = \frac{T_{on}}{T_{on} + T_{off}}. \tag{11}$$

We assume that the difference between the two adjacent operation periods can be omitted. As a result, we can make use of the previous duty cycle to determine the present duty cycle.

Therefore, we can keep ΔT_{on} convergent by controlling ΔT_{on_slave}. By using the proposed phase-shift control scheme, both the master and the slave phase can work in CRM mode and the phase-shift is nearly 180°.

Similarly, we can get a coefficient k, as shown in Fig. 8 by

$$T_{on\_slave} = k \cdot \Delta T_{on} + T_{on\_master}. \tag{12}$$

When $k < 0$, $\frac{\Delta T_{on}{}'}{\Delta T_{on}{}'} < -1$, like I_{Slave1};
When $k = 0$, $\frac{\Delta T_{on}{}'}{\Delta T_{on}} = -1$, like I_{Slave2};
When $k = D = \frac{T_{on}}{T_{on}+T_{off}}$, $\frac{\Delta T_{on}{}'}{\Delta T_{on}} = 0$, like I_{Slave3};
When $k = 2D = \frac{2T_{on}}{T_{on}+T_{off}}$, $\frac{\Delta T_{on}{}'}{\Delta T_{on}} = 1$, like I_{Slave4};
When $k > 2D$, $\frac{\Delta T_{on}{}'}{T_{on}} > 1$, like I_{Slave5};
So, we can see
when $0 < k < 2D$, $\left|\frac{\Delta T_{on}{}'}{\Delta T_{on}}\right| < 1$.

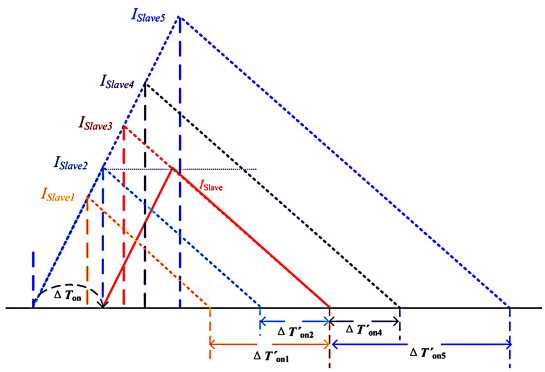


Fig. 8. Slave inductor current waveforms with different coefficient k.

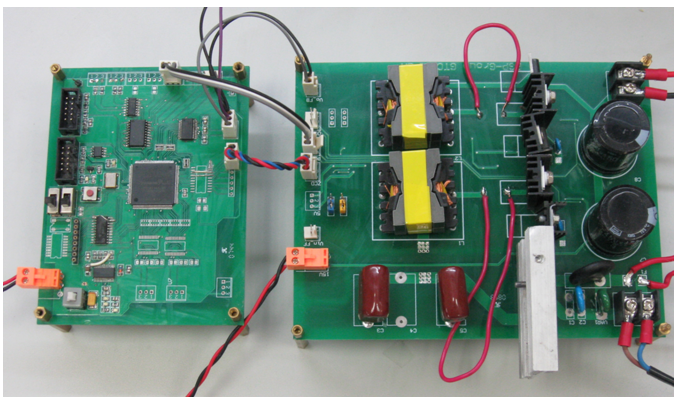


Fig. 9. Photo of the experimental setup.

In addition, we can use the PI or PID method to keep ΔT_{on} convergent. Experiments have proved that this interleaving method is feasible. The slave phase works in CRM mode and ΔT_{on} is almost zero.

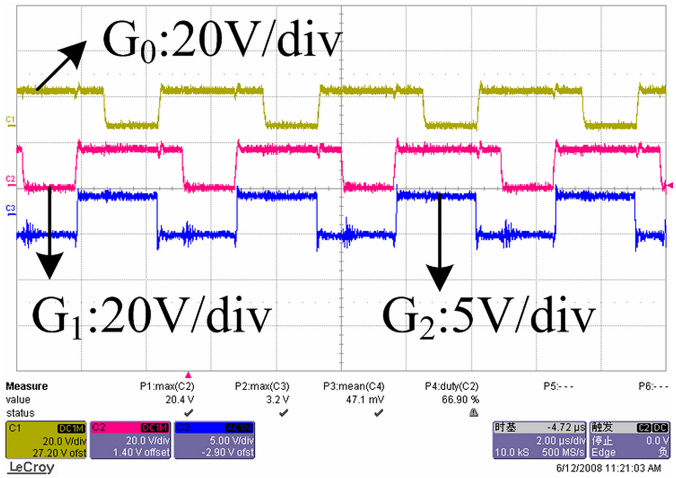
V. Experimental Results

In order to verify the feasibility of the proposed interleaving phase-shift control scheme, an experimental two phase interleaved boost PFC converter was designed and built. The digital controller was implemented using FPGA and AD converters. The control algorithm was developed using a hardware description language (Verilog HDL). The following specifications were implemented:

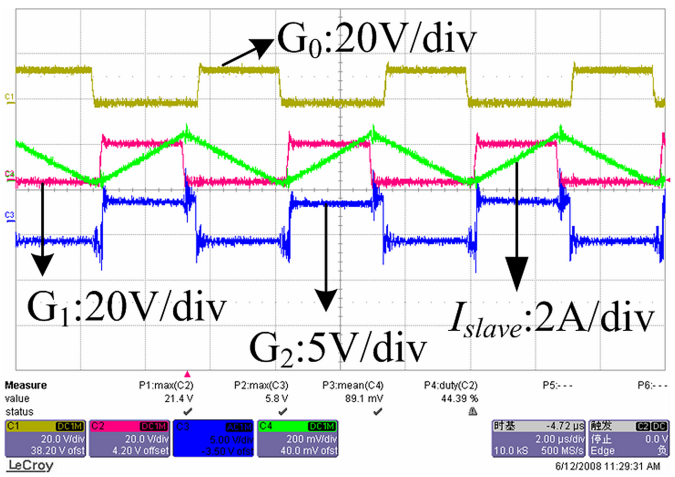
- No. of phases: 2 (180° phase shift)
- Operating frequency: 35 kHz 450 kHz
- Input voltage: $V_{in} = 85 \sim 265 V_{rms}$
- Output voltage: $V_{out} = 400 V_{dc}$
- Total output power: $P_o = 250W$ (2-phase)
- Output capacitor: $C_{dc} = 300\mu F$

The experimental setup of a CRM Boost PFC with the novel phase-shift control scheme is shown in Fig. 9.

Fig. 10 shows the gate signals G_0 and G_1, and the I_{Slave} when the duty cycle $D > 0.5$. It can be seen that the slave phase inductor current I_{Slave} works in CRM mode. The rising edge of G_2 shows the ideal turning-on moment of the slave phase. ΔT_{on} is the difference of the rising edge between G_1 and G_2. Since ΔT_{on} is very small, the phase shift is almost 180°.

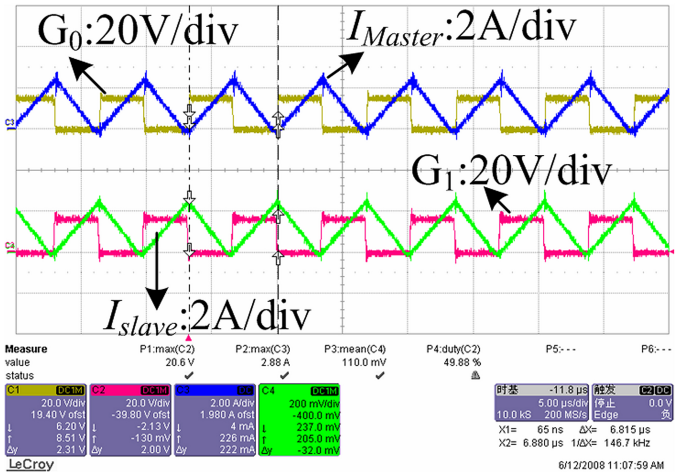


(a) $(G_0, G_1 : 20V/div, G_2 : 5V/div; 2.00\mu s/div)$

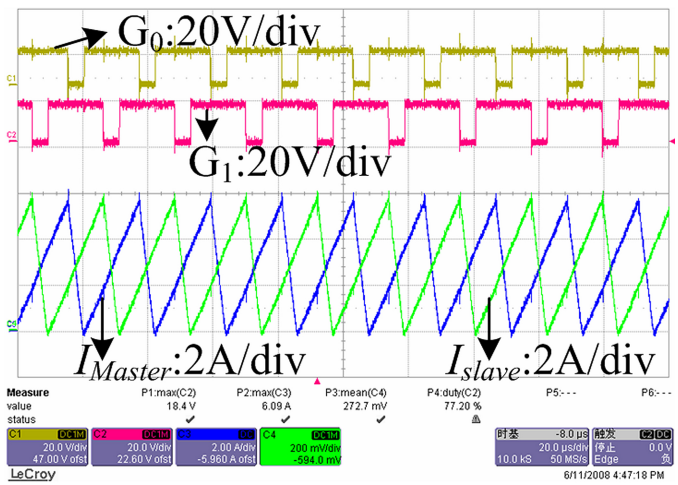


(b) $(I_{Slave} : 2A/div, G_0, G_1 : 20V/div, G_2 : 5V/div; 2.00\mu s/div)$

Fig. 10. Gate signal when $D > 0.5$. (a) Measured gate signals G_0 and G_1 and the ideal turning-on waveforms G_2; (b) Measured inductor current I_{Slave} and gate signals G_0 and G_1 and the ideal turning-on waveforms G_2.



(a) $(I_{Master}, I_{Slave} : 2A/div, G_0, G_1 : 20V/div; 5.00\mu s/div)$



(b) $(I_{Master}, I_{Slave} : 2A/div, G_0, G_1 : 20V/div; 5.00\mu s/div)$

Fig. 11. Inductor currents of the interleaved boost PFC. (a) Measured inductor current I_{Master}, I_{Slave} and gate signals G_0 ,G_1 and the ideal turning-on waveforms G_2. (b) Measured inductor current I_{Master}, I_{Slave} and gate signals G_0 ,G_1.

Fig. 11 shows the inductor currents I_{Master} and I_{Slave}, and G_0 and G_1 of the interleaved boost PFC. It can be observed that both the master phase and the slave phase are working in CRM mode.

Fig. 12 shows the input voltage V_{in}, the input current I_{in} and the output voltage V_O of the PFC while $P_o = 250W$. This experimental result is mainly used to demonstrate two things. First, it shows that the proposed control scheme can be used well in a PFC with a full designed load. Second, and most importantly, it can be seen from the output voltage curve that the PFC circuit worked very well without any sub-harmonic oscillation. If this system was an unstable one, there would be some noise on the output voltage curve. There would not be a smooth curve as shown in Fig. 12.

VI. CONCLUSIONS

This paper described a quantitative analysis of the sub-harmonic oscillation phenomena when adopting turnoff time shifting control schemes for interleaved boost converters operating in critical conduction mode. Based on that, a novel modified turnoff time shifting control scheme was proposed

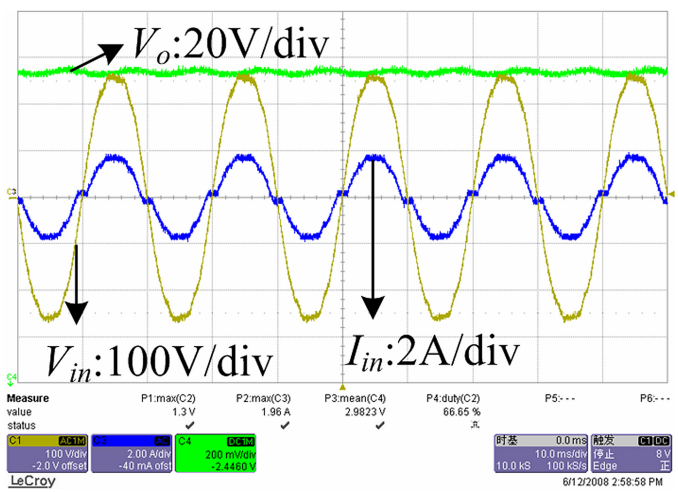


Fig. 12. Measured input voltage V_{in}, input current I_{in} and output voltage V_O $(V_O : 20V/div, V_{in} : 100V/div, I_{in} : 2A/div; 10ms/div)$.

to achieve interleaving operation, where both the master phase and the slave phase can operate stably under CRM mode

within the full input voltage range. This phase-shift control scheme can be used in other interleaved CRM converters such as the flyback or buck topologies. It can also be extended to more phases.

ACKNOWLEDGMENT

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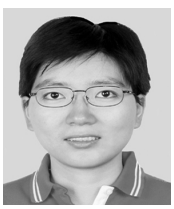

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