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Dual Vector Control Strategy for a Three-Stage Hybrid Cascaded Multilevel Inverter

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Abstract

This paper presents a voltage control algorithm for a hybrid multilevel inverter based on a staged-perception of the inverter voltage vector diagram. The algorithm is applied to control a three-stage eighteen-level hybrid inverter, which has been designed with a maximum number of symmetrical levels. The inverter has a two-level main stage built using a conventional six-switch inverter and medium- and low- voltage three-level stages constructed using cascaded H-bridge cells. The distinctive feature of the proposed algorithm is its ability to avoid the undesirable high switching frequency for high- and medium- voltage stages despite the fact that the inverter's dc sources voltages are selected to maximize the number of levels by state redundancy elimination. The high- and medium- voltage stages switching algorithms have been developed to assure fundamental switching frequency operation of the high voltage stage and not more than few times this frequency for the medium voltage stage. The low voltage stage is controlled using a SVPWM to achieve the reference voltage vector exactly and to set the order of the dominant harmonics. The inverter has been constructed and the control algorithm has been implemented. Test results show that the proposed algorithm achieves the desired features and all of the major hypotheses have been verified.

Key Words: Inverters, Power conversion harmonics, Pulse width modulated inverters, Pulse width modulation.

I. INTRODUCTION

Multilevel inverters, MLIs, refer to the class of inverters with output points which have more than two voltage levels with respect to a reference point. The feature of having an output voltage level that is higher than those of the power semiconductor switching devices' ratings puts the MLIs in high power converters class. The application of MLIs, however, has been extended to the medium power range due the advantages of reduced distortion, dv/dt stress and common mode voltage [1]–[3].

The cascaded H-bridge (CHB) is a MLI topology with a modular structure that, unlike other topologies, makes the extension of the inverter circuit a straightforward procedure. The main drawback of a CHB inverter is the need for a large number of isolated dc supplies [4]–[6].

Supplying the arm cells of a CHB inverter with different dc voltages provides different voltage steps and therefore increases the number of levels for the same circuit configuration [6]–[9]. With ratio-3 related dc voltages for the cascaded cells (1:3:9: ...) the number of levels of an asymmetrical CHB inverter is maximized [10]–[14]. This ratio has been used to construct inverters with a large number of levels and consequently very little voltage distortion for various applications [14], [15]. It has been found, however, that inverters with ratio-3 dc sourced cells are not appropriate for high frequency PWM control methods since the high voltage stages are subjected to a high switching frequency [11], [16], [17].

Asymmetrical inverters, like other CHB inverters, suffer from the need for a large number of isolated dc supplies [18], [19]. To ease this problem a hybrid multilevel inverters created by cascading smaller dissimilar inverter circuits has been suggested [20]. Hybrid inverters have different approaches to achieve the goal of dc supply cost reduction, such as:

- Replacing the dc supply of the lower voltage stages with capacitors and controlling the inverter to receive zero average power from the capacitor-fed stages [21], [22].
- Replacing the highest voltage cascaded stages with a singly-supplied inverter such as a basic 2-level, six-switch inverter [23] or a multilevel neutral point clamped stage [24].
- For open winding loads, it is possible to cascade two inverters each with three output points, such as a neutral-point clamped MLI, by connecting their outputs to the two sides of an open-winding load [25].
- A mixed-level topology based on using multilevel neutral point clamped or flying capacitor branches as special full bridge cells arms. Two l-level arms construct a $(2l-1)$-level H-bridge cell, so that the required number of isolated dc supplies is reduced [26], [27].
- Supplying various hybrid inverter stages using the same dc source and isolating the outputs using a multi-primaries transformer [28], [29]. This option is not suitable when a wide frequency range including a near dc frequency is needed.

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Many studies have been done on the control of MLIs. Both high and low frequency switching approaches have been considered. Examples of high frequency switching approaches include the multicarrier PWM strategy, space vector modulation and carrier based space vector modulation. High switching frequency approaches have been used mainly with symmetrical topologies where effective amplitude control and the harmonics reduction method is crucial due to the small number of levels [30]–[35].

Among the fundamental frequency control techniques are voltage vector approximation which has been applied to asymmetrical MLIs [14], and selected harmonics elimination which has been extended to MLIs and implemented using switching angles lookup tables [6] or real time harmonic elimination [36], [37].

The approach of combining high and low switching frequencies for various stages of a hybrid inverter has been considered recently [21], [26] where the two level stages have been operated in square wave mode, while the three-level inverter has been controlled by a carrier-comparison PWM strategy. In [38] a 9-level, 3-stage, asymmetrical cascaded MLI has been controlled with a hybrid strategy; the high power cells have been operated at the fundamental frequency while the low power stage is controlled by high frequency PWM.

According to the modulation condition concept, a multistage MLI is suitable for PWM control only if it is designed in such a way that switching between any two adjacent voltage levels is achievable by controlling the lowest voltage stage while fixing the states of the other higher voltage stages [9]. As PWM control implies high frequency switching between adjacent voltage levels, this switching must be applicable by controlling the low voltage stage only. In inverters designed with a maximum number of levels, some of the transitions between adjacent voltage steps cannot be achieved without switching other inverter stages. When a controller operates an inverter to produce a reference voltage level between these two levels, simultaneous and high voltage stage high switching frequencies occur.

Previous studies have often chosen to satisfy the modulation condition, and therefore to not design inverters with a maximum number of levels. In this case PWM control can be considered as in [21], [26], [38]. In other studies, when the dc souring is selected to have a maximum number of levels PWM control is unsuitable as the high voltage stage will be subjected to a high switching frequency as in [13]. The authors, so far, have not came across any published research that combines a maximum number of levels and PWM control without the high voltage stage being requested to commutate at a high switching frequency.

The main aim of this research is to control an inverter designed with a maximum number of levels in an effective high frequency PWM mode. In the proposed control algorithm, the high voltage stage will be operated in square wave mode. The medium voltage stage will be operated in low frequency mode, while the low voltage stage will be controlled by a SVPWM at the intended switching frequency. An approach based on voltage vector decomposition has been developed to ensure the frequency conditions for the high and medium stages and, at the same time, to set the low voltage stage in a valid PWM controlled region.

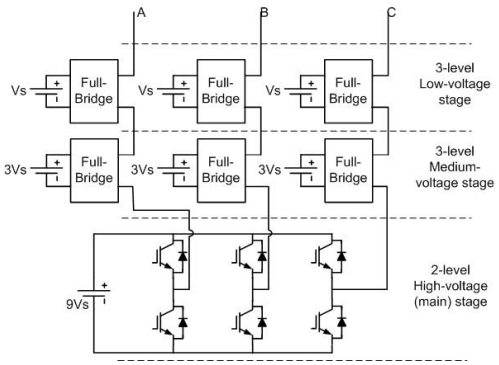


Fig. 1. Three-stage, 18-lelvel hybrid MLI topology.

The inverter circuit topology, definitions of the switching variables and the inverter voltage vectors are described in section II. The dual control concept is presented in section III. In section IV the implementation of the power circuit and the control strategy have been presented. Experimental results and discussions are given in section V.

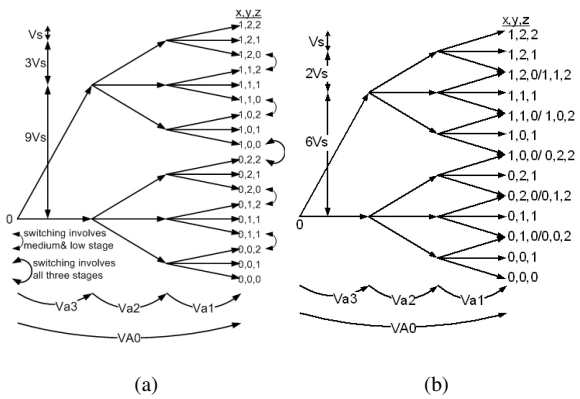
II. Inverter Topology and Switching States

The inverter circuit shown in Fig. 1 consists of the "main" high voltage six-switch inverter with each output line in series with two single-phase full bridge inverters. The medium and low voltage stages are three level inverters composed of three H-bridge cells. The main and H-bridge cells are fed by isolated dc sources of 9Vs, 3Vs, and Vs. This voltage ratio provides an 18-level inverter. In this design the high voltage stage has only one dc source that operates with a reduced current ripple compared to the three dc sources of the CHB design [13]–[16]. Therefore, a considerable reduction in the number of dc sources and losses can be achieved.

Fig. 2(a) shows the possible output voltage levels with respect to the negative side of the main dc source (9Vs). Switching between any two adjacent states may involve not only the low voltage stage, but also the medium or even the high voltage stages as indicated. As the PWM control scheme involves fast switching between adjacent voltage levels, it is not appropriate to control this inverter using traditional PWM as the design violates the modulation condition [9]. Considering the same inverter topology, to fulfill the modulation condition with a maximum number of levels the voltage ratio should be 1:2:6 as shown in Fig. 2(b). This ratio gives a 13-level inverter rather than 18. As a result, complying with the modulation condition results in a reduction of 5 levels in this case. In our design we have modified the control method to prevent any undesirable high switching frequency without sacrificing the maximum number of levels.

A. The voltage vectors and inverter states

The switching variables of the inverter are denoted by $\{(\boldsymbol{x}_{abc}), (\boldsymbol{y}_{abc}), (\boldsymbol{z}_{abc})\}$ where x is a binary digit while y and z are trinary digits. The states of the high, medium and low voltage stages are determined by $\boldsymbol{x}_{abc}$, $\boldsymbol{y}_{abc}$ and $\boldsymbol{z}_{abc}$



(a) (b)

Fig. 2. Voltage levels of used topology. (a) Maximum number of levels. (b) Satisfying the modulation condition.

respectively. The output voltage vector can be represented in terms of the switching state as shown in the following derivation. Line-to-line voltages are represented in terms of the switching variables in (1).

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = 9V_S \begin{bmatrix} x_a - x_b \\ x_b - x_c \\ x_c - x_a \end{bmatrix} + 3V_S \begin{bmatrix} y_a - y_b \\ y_b - y_c \\ y_c - y_a \end{bmatrix} + V_S \begin{bmatrix} z_a - z_b \\ z_b - z_c \\ z_c - z_a \end{bmatrix}. \quad (1)$$

The phase voltages of the Y-connected load can be represented as follows:

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} v_{ab} - v_{ca} \\ v_{bc} - v_{ab} \\ v_{ca} - v_{bc} \end{bmatrix} = \frac{V_S}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} 9x_a + 3y_a + z_a \\ 9x_b + 3y_b + z_b \\ 9x_c + 3y_c + z_c \end{bmatrix}. \quad (2)$$

The voltage vector is achieved by Park's transformation given in (3).

$$\begin{bmatrix} v_D \\ v_Q \end{bmatrix} = \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} v_D \\ v_Q \end{bmatrix} = V_s \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} 9x_a + 3y_a + z_a \\ 9x_b + 3y_b + z_b \\ 9x_c + 3y_c + z_c \end{bmatrix}. \quad (4)$$

Using (4), the voltage vector corresponding to any inverter state can be achieved. Alternatively, the voltage vector diagram for the three-stage inverter is drawn in two superposition steps. First, the vector diagram of the 3-level medium voltage stage inverter (composed of 19 vectors) is drawn at the end of each of the seven vectors of the high voltage stage. Then, the vector diagram corresponding to the low voltage stage has been superimposed at the ends of the resultant vectors as shown in Fig. 3.

B. The voltage vectors in G-H axis system

The 60°-spaced gh-coordinate system shown in Fig, 4 will be used to represent the voltage vectors in the proposed control algorithm. This system allows for straightforward calculations since it is tightly related to the inverter voltage vectors. The gh-coordinates of the voltage vectors of the 2-level inverter take only the values V_{dc}, 0, and $-V_{dc}$, where V_{dc} is the inverter dc source voltage. The three-level inverter's vectors

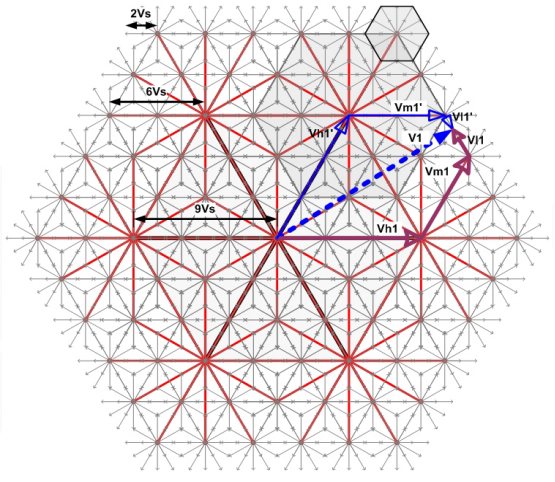


Fig. 3. Voltage vectors of the 18-level inverter.

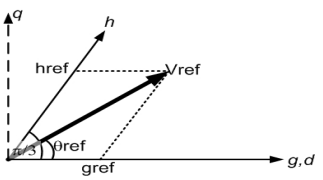


Fig. 4. The 60°-spaced gh-axis system used to represent the voltage vectors.

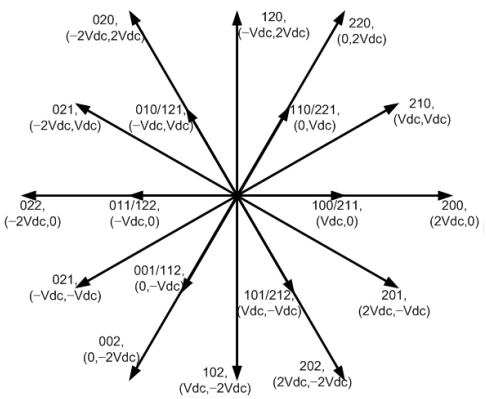


Fig. 5. Voltage vectors in gh-coordinate system for a three-level inverter.

gh-coordinates, as shown in Fig, 5 take 2, 1, 0, -1 and -2 multiples of V_{dc}. This allows for simple control of the inverter by short fixed point calculations.

C. High and medium states domains

Each of the 18-level inverter vectors can be represented by the addition of three vectors belonging to the high, medium and low stages. With the exception of the outmost vectors, most of the 18-level inverter vectors can be represented by more than one combination of the three stages' voltage vectors, as for the example vector V1 shown in Fig. 3.

To achieve fundamental frequency operation at the high voltage stage, the control algorithm explained in the next section aims to hold the high voltage state as long as the reference vector can be reached by adding medium and

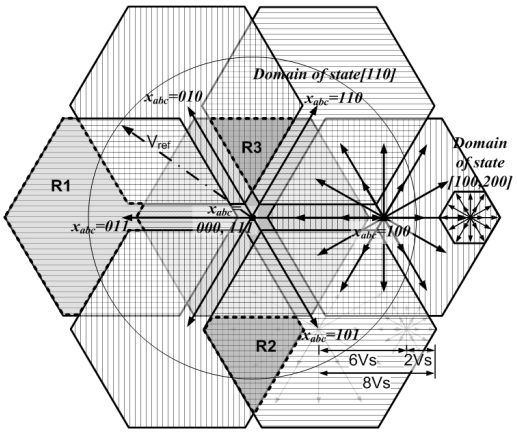


Fig. 6. High voltage vectors domains.

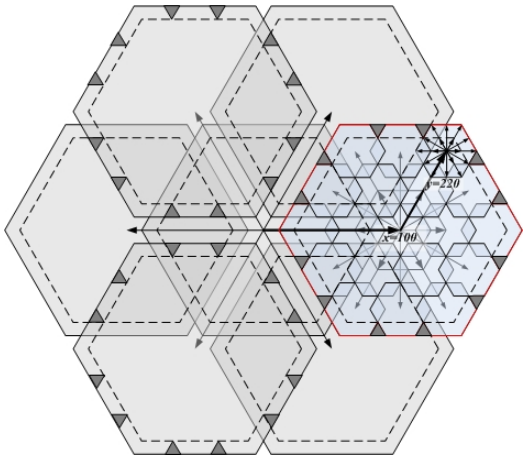


Fig. 7. Medium stage domains corresponding to the high state $\boldsymbol{x}_{abc}$=100, dashed lines define the PWM high voltage stage domains.

low vectors to this high voltage vector. We shall define the hexagonal area marked by the medium and low stages vectors superimposed on a given high state vector by its "domain." The seven domains of the high voltage stage vectors are shown in Fig. 6.

In Fig. 6 the grand hexagon, the inverter vector space, is composed of seven partially overlapping high states hexagonal domains. Some regions in the space belong to exactly one high state domain without overlap, e.g. the region denoted by R1 which is covered only by the domain of state $\boldsymbol{x}_{abc}$=011. If the reference vector is located in this area, the controller should select the corresponding high state. The other areas are overlaps of more than one high state domain, such as R2 (R3) which is mutual between $\boldsymbol{x}_{abc}$=001 and 101 ($\boldsymbol{x}_{abc}$=000,110,010, and 111). If the reference is located in such a region there is more than one option in the selection of $\boldsymbol{x}_{abc}$. The circular trajectory of the reference vector shown in Fig. 6 passes through the six high state domains consecutively, and the controller will change the high voltage stage state every 60°.

The domains of the middle stage vectors can be defined in a similar way. The nineteen hexagons, which represent the area covered by the low voltage stage vector diagram, can be drawn within each of the seven high state domains at the tips of the 19 medium voltage vectors as shown in Fig. 7 within the domain of $\boldsymbol{x}_{abc}$=100. The medium state selection determines which of the 19 hexagons is covered by the PWM control of the low voltage stage inverter.

By holding the state of the high voltage stage, the medium stage state selection and the PWM control of the low voltage stage will cover the high voltage stage domain area defined in Fig. 6 except for the twelve small darkly shaded triangles at the outer sides of the hexagons in Fig. 7. Therefore, we are going to define the PWM control domain as the hexagon with a side length of 7Vs shown within the dashed lines in Fig. 7.

III. Dual SVPWM Control Strategy

A. The control concept

A flow diagram of the control algorithm is shown in Fig. 8. The reference vector is sampled at a sampling rate of T_s. During the sampling period, the controller determines the next switching states for the high, medium and low voltage stages consecutively. The outputs of the high and medium stages routines are the values of $\boldsymbol{x}_{abc}$ and $\boldsymbol{y}_{abc}$ to be applied during the following sampling period. The low voltage stage routine determines the three vectors nearest to the low stage reference and their corresponding duty ratios during the following switching period. The output of the low voltage routine is a j-element states vector [$\boldsymbol{z}_{abc}$], rather than one state $\boldsymbol{z}_{abc}$. During the following sampling period, $\boldsymbol{z}_{abc}$ will take the values of these vector elements consecutively for the sub-periods of T_c(=T_s/j).

B. Determination of high and medium states

Initially the reference vector is converted to its g-h components using the following equations:

$$g_{ref} = |V_{ref}| \times \left(\cos\theta_{ref} - \frac{\sin\theta_{ref}}{\sqrt{3}} \right)$$
$$h_{ref} = |V_{ref}| \times \left(\frac{2\sin\theta_{ref}}{\sqrt{3}} \right). \quad (5)$$

The calculation of $\boldsymbol{x}_{abc}$ ($\boldsymbol{y}_{abc}$) begins by determining if the reference vector is located in the domain of the current high (medium) voltage state by comparing the reference absolute gh-coordinates to the first quadrant portion of the domain as shown in Fig. 8. If so, $\boldsymbol{x}_{abc}$ ($\boldsymbol{y}_{abc}$) holds its value during the next switching interval.

If the reference vector is not within the current state domain, the new high (medium) switching state will be calculated as follows:

1) The reference vector is compared to the 7 high (19 medium) domains and a short list of the feasible states for the next switching period is generated. A feasible state is any state that has the reference vector located in its domain.
2) If the feasible states list has only one element, this state will be the next high (medium) state (end).
3) Otherwise, the feasible states list is compared to the initial state and the state with minimum difference is taken as the next state.

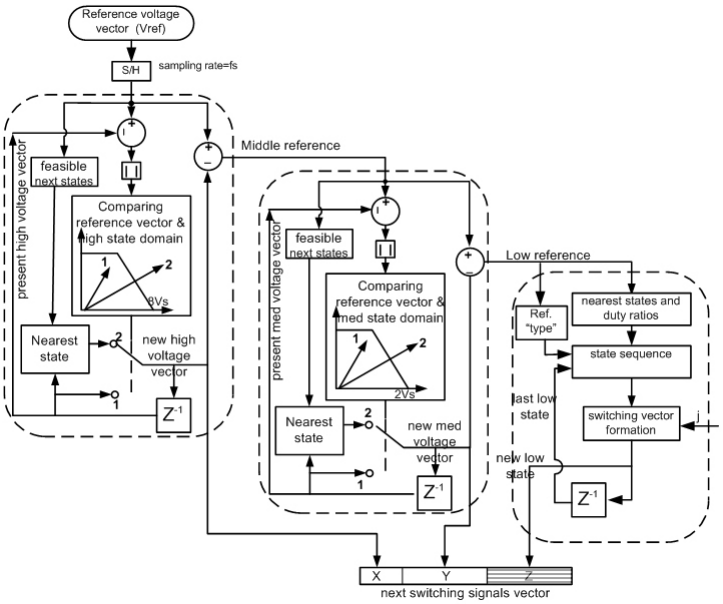


Fig. 8. Flow diagram of the control algorithm.

C. Low voltage state voltage vector control

The low voltage stage is composed of a three-level inverter and it is controlled using the voltage vector control strategy. The control routine is carried out according to the following steps:

STEP 1: The three inverter states nearest to the reference state and the corresponding duty ratios have been determined following the procedure presented in [31]. This procedure is suitable since it applies a 60°-displaced axis system to determine the inverter vectors and the duty ratios. The equations used to determine the three nearest vectors and the duty ratios are given in the Appendix. However, the abovementioned reference provides no information about the sequence of sorting the inverter states.

STEP 2: The inverter is operated in four switching states within each sampling interval, T_s, to realize the reference vector. The first and last switching states are equivalent. The states sequence has been determined by identifying the type of the triangle in which the reference vector is located according to Fig. 9. The three types of the triangles are defined as follows:

- Type 1: the triangle is formed by two outer vectors and one inner vector.
- Type 2: the triangle is formed by one outer vector and two inner vectors.
- Type 3: the triangle is formed by zero vector and two nonzero inner vectors.

The outer vectors are associated with unique switching states and the inner six vectors are associated with two equivalent switching states, while the center zero vector is associated with three zero states. In Fig. 9 the outer vector states are denoted by (λ). The inner vectors states are denoted by (σ_1, σ_1', σ_2 and σ_2') where the three trinary digits ($\boldsymbol{z}_{abc}$) of the σ_1 state are composed of one (1_3) and two (0_3) digits,

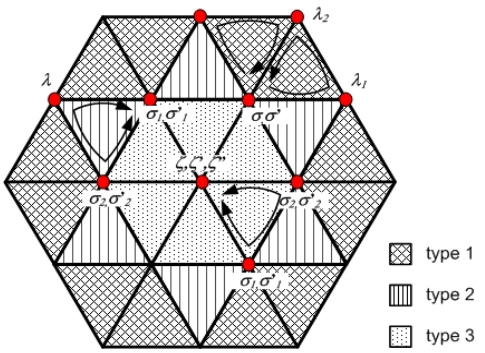
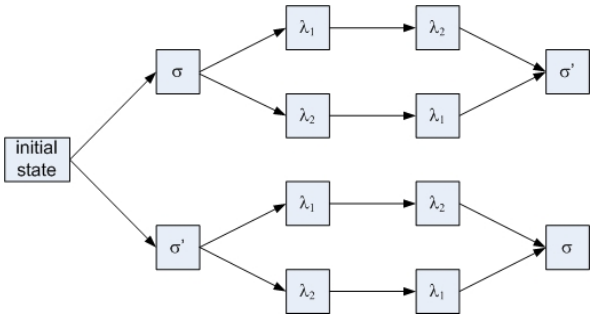


Fig. 9. Types of the three-level inverter triangles.

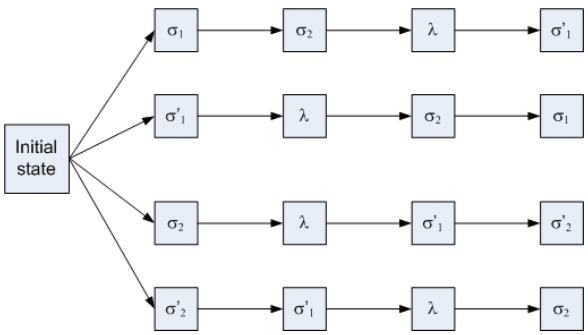
where the subscript indicates that the digit is trinary. State σ_1' is equivalent to σ_1 but with one (2_3) and two (1_3) digits. On the other hand σ_2 has in its trinary expression ($\boldsymbol{z}_{abc}$) one (0_3,) and two (1_3) digits while σ_2' is its equivalent with one (1_3) and two (2_3) digits.

The states sequence has been assigned according to Fig. 10. In figures 10a-10c, when there is a branched next state, the controller selects the path with the minimum switching transitions and when there is a unique next state, the switching involves one digit switching to the adjacent position, i.e. $0_3 \leftrightarrow 1_3$ or $1_3 \leftrightarrow 2_3$.

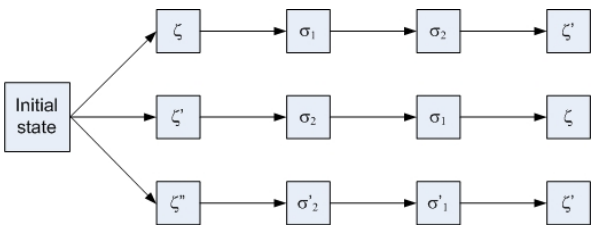
STEP 3: The state sequence and duty ratio information are expanded to form the switching states vector with the four switching states repeated proportionally to their duty ratios. As indicated earlier, this vector has j elements. Consider for example a type 1 triangle and assume the sequence (σ, λ_1, λ_2, σ') is to be followed according to the nearest state criteria. Denoting the duty ratios of the states σ, λ_1 and λ_2 with d_σ, $d_{\lambda 1}$ and $d_{\lambda 2}$ respectively, the low stage states vector will be



(a) State sequence of type 1



(b) State sequence of type 2



(c) State sequence of type 3

Fig. 10. State sequence of the SVM controlled low voltage stage.

in the following form:

$$z_{abc}(1:j) = \begin{bmatrix} \sigma \\ \vdots \\ \sigma \\ \lambda_1 \\ \vdots \\ \lambda_1 \\ \lambda_2 \\ \vdots \\ \lambda_2 \\ \sigma' \\ \vdots \\ \sigma' \end{bmatrix} \begin{matrix} \\ \\ \leftarrow z_{abc}(n_\sigma) \\ \leftarrow z_{abc}(n_\sigma + 1) \\ \\ \leftarrow z_{abc}(n_\sigma + n_{\lambda 1}) \\ \leftarrow z_{abc}(n_\sigma + n_{\lambda 1} + 1) \\ \\ \leftarrow z_{abc}(n_\sigma + n_{\lambda 1} + n_{\lambda 2}) \\ \leftarrow z_{abc}(n_\sigma + n_{\lambda 1} + n_{\lambda 2} + 1) \\ \\ \leftarrow z_{abc}(j) \end{matrix} \quad (6)$$

where:

$$n_\sigma = round(j * d_\sigma/2) \quad (7)$$

$$n_{\lambda 1} = round(j * d_{\lambda 1}) \quad (8)$$

$$n_{\lambda 2} = round(j * d_{\lambda 2}). \quad (9)$$

In (7)–(9) "round" stands for rounding to the nearest integer.

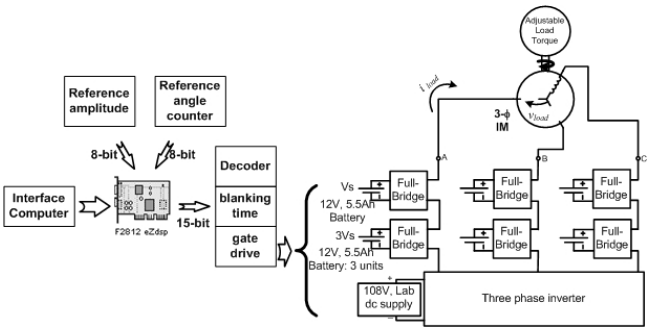


Fig. 11. Experimental setup.

IV. Experimental Setup Description

A prototype of the proposed inverter has been constructed. The low and medium voltage stages have been supplied by lead acid 12V -5.5Ah batteries. Three series connected units are used for the medium voltage stage to supply 36V. The high voltage stage has been fed 108V using a laboratory dc power supply. For high and medium voltage stages, IGBTs are used, while MOSFETs have been used for the low voltage stage. A 0.9kW, 380V, 50Hz, 4-pole asynchronous motor has been used as a load.

The control algorithm has been implemented using a DSP controller board eZdsp R2812 based on a 150MHz, fixed point TMS320R2812 CPU. The sampling time (T_s) for the outer loop has been set to 111μs.

The sampling period has been divided into (j=) 100 subintervals, therefore the 50 Hz reference voltage will be represented by ($1 \div (50 \times 111\mu)$=) 180 samples. The low stage state will have a period of $2T_s$ or a switching frequency of 4.5kHz assuming that the final state could be taken as the initial state for the following period. The consequence of selecting j of 100 is that the minimum switching pulse width for the low voltage stage will be $2T_s/100$.

One of the 16-bit digital ports has been allocated for the input and another port for the output. Eight out of the 16 input port bits have been allocated for the reference vector amplitude, where the voltage vector with a norm of Vs is represented by $(10)_H$. The base or 100% of the reference amplitude is taken as the radius of the largest circle that can be drawn inside the inverter hexagonal vector space. The radius of this circle is (17Vs$\times\sqrt{3}/2$=)14.722Vs and according to the defined scale equivalent to $(EC)_H$.

Fifteen out of the 16-bit output ports have been used to provide the switching signal. Each arm of the two and three level sub-inverters is driven by one bit. An external logic circuit has been used to decode the switching signals and insert a blanking time as shown in Fig. 11.

V. Experimental Results

Two algorithms have been tested. The first algorithm implements the basic high state hexagonal domain of the side length equivalent to 8Vs. The second algorithm uses the PWM hexagonal domain of the side length equivalent to 7Vs, as indicated in section II and Fig. 7.

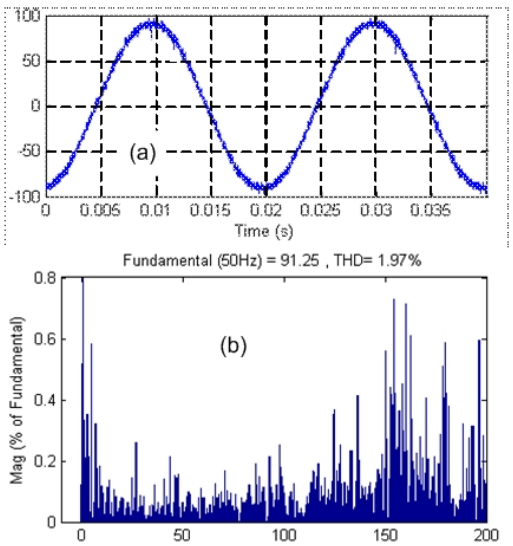


Fig. 12. Phase voltage measurements with 80% amplitude and 50Hz frequency reference.(a) Phase-voltage waveform, (b) Frequency spectrum of the phase voltage.

A. *Inverter characteristics with basic high state domain*

Fig. 12(a) shows the measured phase voltage waveform and its corresponding frequency spectrums with a sinusoidal reference of 80% amplitude and 50Hz. The total harmonic distortion is less than 2% reflecting a low distortion of the output voltage. Fig. 12(b) shows that the dominant harmonics order is around 180, which is the number of sampling intervals per cycle. Fig. 13 shows the switching signals for the three stages. The top signal verifies that the high voltage stage operates in square wave mode, the second signal shows that the medium stage operates at an average switching frequency equivalent to four times the fundamental frequency, and the third is the switching signal for the low voltage stage. As the low voltage stage signal is not visible on the same time scale, a horizontal zoom-in of a 1 ms interval ($9T_s$) is shown at the bottom of Fig. 13. This Fig. shows 4.5 pulses during this interval which confirms what was mentioned in section IV that the low voltage stage switching signals have one pulse every $2T_s$.

The total harmonic distortion variation with the reference voltage amplitude is shown in Fig. 14. The output voltage has a low harmonic distortion over a wide range of M. The high THD experienced when M<0.2 is due to the fewer number of levels available to form the output voltage as shown in Fig. 15a. As shown in Fig. 15b the frequency of the dominant harmonics is around 9kHz, or $(1/T_s)$ and this is twice the average switching frequency of the low voltage stage.

It can be noticed in Fig. 14 that there is a rise in the harmonic distortion when the reference amplitude, or the magnitude control ratio M, is around 45% and 65%. To investigate the cause of the THD rise, consider the measurement of the phase voltage with a reference amplitude of 45% in Fig. 16. As can be seen, the waveform has a defect almost every 30°. This can be explained by recalling that the high voltage domain assumed in this algorithm is a 8Vs hexagon. As shown in Fig. 7 there are 12 triangular areas within that hexagon which are not covered by the PWM controlled region.

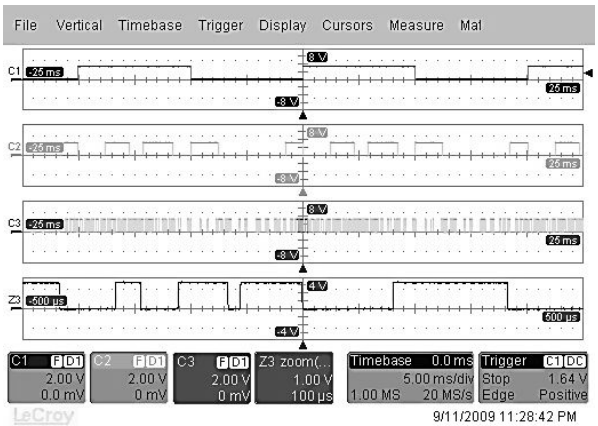


Fig. 13. The switching pulses from the top c1: high voltage stage, c3: medium voltage stage c2: low voltage stage, The switching pulses of the three stages 5ms/div), (b) Zoon in the low voltage stage switching pulses (100μs/div).

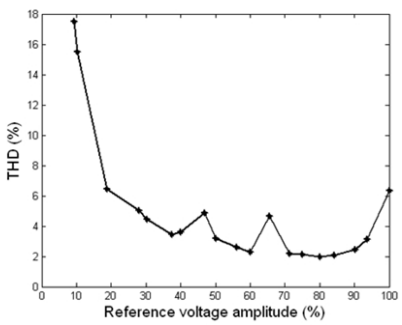


Fig. 14. Harmonics distortion variation against the reference amplitude (%).

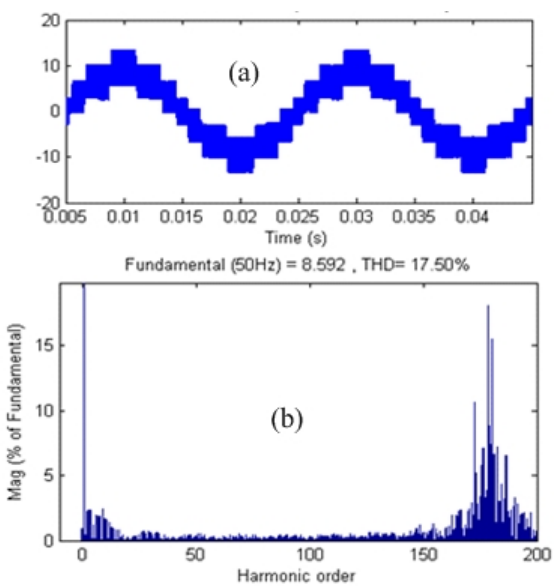


Fig. 15. Phase voltage measurements with 9.4% amplitude and 50Hz frequency reference. (a) Phase-voltage waveform, (b) Frequency spectrum of the phase voltage.

Fig. 17 shows that within the two rings where 0.41<M<0.47 and 0.65<M<0.71, as the reference voltage rotates it will be subjected to pass though the triangular areas

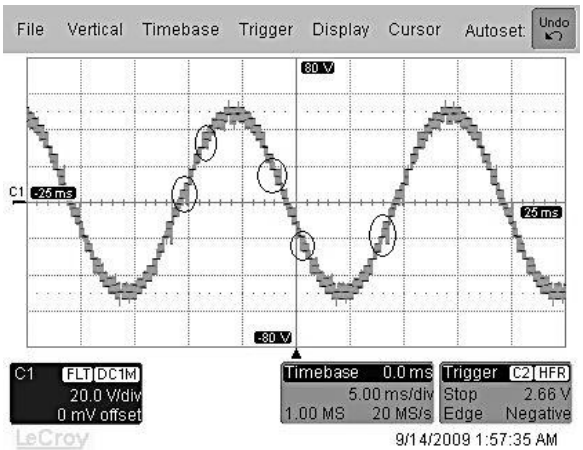


Fig. 16. Phase voltage measurement with reference amplitude=45%. Scale =20V/div, 5ms/div.

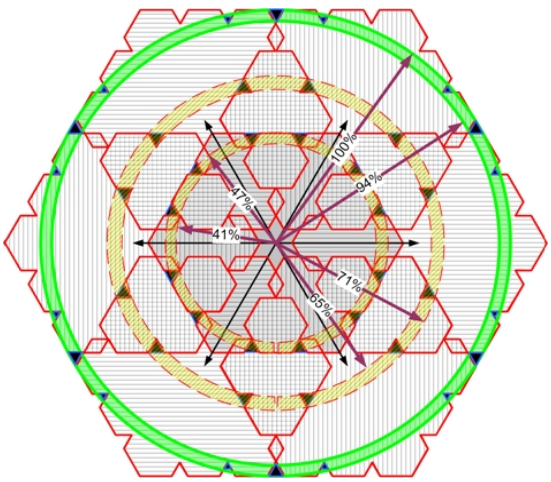


Fig. 17. The two rings show the area at which inverter is prone to high distortion using the basic high state domain.

outside the PWM control region.

B. Inverter characteristics with a modified high state domain

We have diagnosed the distortion in the waveforms for certain ranges of M that occurs when the reference voltage vector falls in the part of the high domain which in not covered by the PWM control range of the low stage. To cure this problem we can redefine the high voltage domain by excluding these regions from the hexagonal shape. However, this option adds complexity to the control algorithm due to the complex shape of the domain. Instead, we have considered the smaller hexagons with 7Vs sides, which are entirely located in the PWM controlled region. The characteristic of an inverter with this domain can be predicted from Fig. 18. Since the 7Vs hexagon is entirely under the PWM control, we can obtain full PWM for any reference voltage amplitude less than 82%.

This hypothesis has been verified by the output voltage measurement with a reference amplitude of 45% shown in Fig. 19. In figure19a, the defects in the phase voltage waveform examined in Fig. 16 are cancelled. The high voltage stage switching pulses are shown in Fig. 19b, which shows modulating the zero states (current circulation mode) with

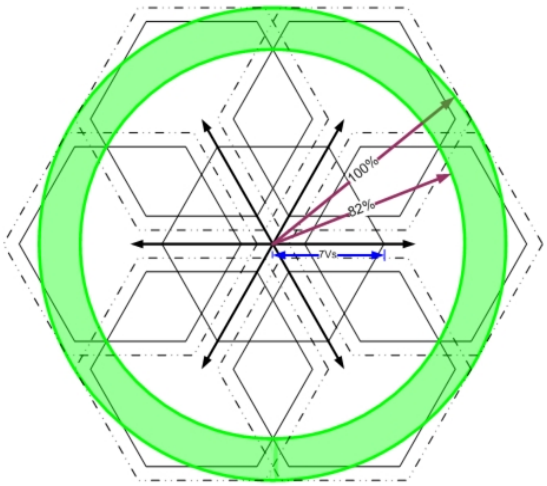


Fig. 18. The shaded ring represents the range of reference amplitude at which the inverter prone to distortion.

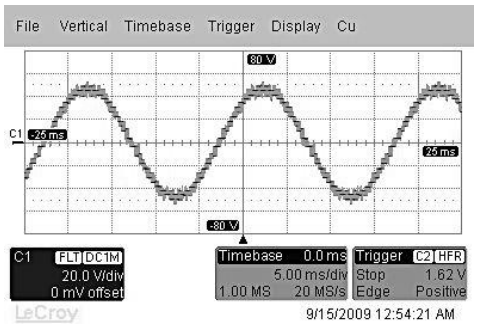
the nonzero states. With the basic domain considered in the previous section and the same value of M the high state remains in the current circulating mode as shown earlier. Fig. 19c and d show the phase voltages corresponding to the high voltage stage and lower stages respectively.

While the 7Vs domain solves the PWM coverage problem within the two ranges of the reference amplitude indicated in Fig. 17, Fig. 18 shows that proper PWM operation will be lost if the reference amplitude exceeds 82%. Therefore, the basic 8Vs domain should be used in this region. The THD over the entire range of the reference amplitude in Fig. 20 shows that for $0<M<0.8$, the selection of 7Vs high domains has cured the problem of increased distortion around M=0.45 and M=0.65 apparent in Fig. 14. However, we can notice a fast rise in harmonic distortion for $M>0.8$ due to the presence of a reference voltage vector in the regions not covered by the modified 7Vs domains.

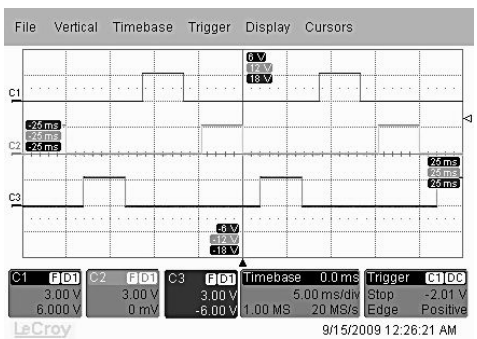
From the THD characteristics of the two domains (8Vs and 7Vs) it can be seen that the problems of intermitted range distortion associated with the basic high state domain and the high distortion for $M>0.8$ associated with the modified domain can be avoided by setting the domains of 7Vs to $M<0.8$ and 8Vs to $M>0.8$. This solution will not disturb the switching frequency or the maximum number of levels.

In the proposed algorithm, the high voltage stage switching frequency equals the output fundamental frequency and the medium stage operates at no more than five times this frequency. The SVPWM method is used to control the low voltage stage, which operates at an average frequency equivalent to half the sampling frequency and provides all the PWM control advantages.

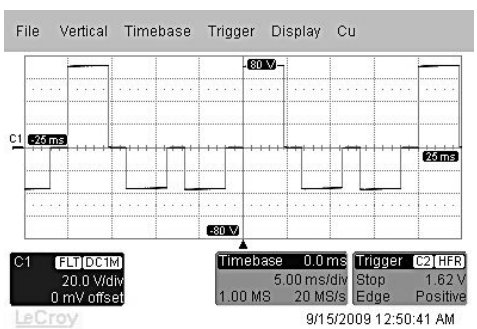
The suggested strategy has been tested using a fixed point low cost DSP controller card and, thanks to the 60° coordinate system, the controller execution speed is shown to be satisfactory for most applications. During the experimental testing stage, the distortion problem occurring with a certain reference amplitude has been addressed. To solve this problem, a simple modification has been introduced and tested without compromising any of the system features.



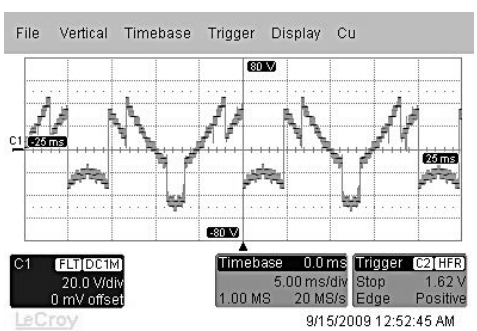
(a) Phase voltage, 50V/div, 10ms/div



(b) High voltage stage switching signals



(c) Phase voltage corresponding to high stage only



(d) The phase voltage due to medium and low voltage stages

Fig. 19. Measurements with modified 7Vs high state domain and 45% reference amplitude.

The experimental results prove the hypothesis regarding the switching frequency and show that the proposed inverter provides very low harmonic distortion over a wide range of the modulation index. The results also show that the dominant harmonics frequency is around the sampling periods or twice the low voltage stage switching frequency.

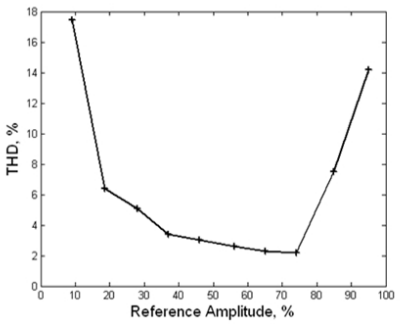


Fig. 20. Harmonic distortion variation against the reference amplitude (%) using the modified 7Vs high state domain.

VI. Conclusion

In this paper a three stage, 18-level inverter and its innovative control strategy have been presented. The inverter has been designed with one main dc source to reduce the dc supply cost and the supply voltage ratios have been selected to maximize the number of symmetrical levels. While this design has been known to be unsuitable for PWM control since it subjects the high voltage stage to a high switching frequency, the suggested control method has been proven to avoid this problem.

APPENDIX

The determination of the low voltage stage voltage vectors and duty ratios:

1) The low reference gh components normalized to Vs as a base, denote the reference dimensions by (g_{ref}, h_{ref})
2) The nearest four states around the reference vector are:
   a) $(\text{ceil}(g_{ref}), \text{floor}(h_{ref}))$
   b) $(\text{floor}(g_{ref}), \text{ceil}(h_{ref}))$
   c) $(\text{floor}(g_{ref}), \text{floor}(h_{ref}))$
   d) $(\text{ceil}(g_{ref}), \text{ceil}(h_{ref}))$

   where $\text{ceil}(x)$ is the integer nearest to and higher than the $\text{real}\ x$ and $\text{floor}(x)$ is the integer nearest to and lower than the $\text{real}\ x$.
3) The three inverter states around the reference vector are vectors a and b, and one of the vectors (c or d) according to the following condition:
   IF $(g_{ref} + h_{ref}) < (\text{ceil}(g_{ref}) + \text{floor}(h_{ref}))$
   Then the third state is state (c)
   ELSE the third state is state (d)
4) The duty ratios of the three states:
   IF the third state is state c
   $$d_a = \text{ceil}(h_{ref}) - h_{ref}$$
   $$d_b = \text{ceil}(g_{ref}) - g_{ref}$$
   $$d_c = 1 - d_a - d_b$$
   ELSE
   $$d_a = g_{ref} - \text{floor}(g_{ref})$$
   $$d_b = h_{ref} - \text{floor}(h_{ref})$$
   $$d_d = 1 - d_a - d_b$$

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