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Three-Phase Line-Interactive Dynamic Voltage Restorer with a New Sag Detection Algorithm

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Abstract

This paper describes the development of a three-phase line-interactive DVR with a new sag detection algorithm. The developed detection algorithm has a hybrid structure composed of an instantaneous detector and RMS-variation detectors. The source voltage passes through the sliding-window DFT and RMS calculator, and the instantaneous sag detector. If an instantaneous sag is detected, the RMS variation detector-1 is selected to calculate the RMS variation. The RMS variation detector-2 is selected when the instantaneous sag occurs under the operation of the RMS variation detector-1. The feasibility of the proposed algorithm is verified through computer simulations and experimental work with a prototype of a line-interactive DVR with a 3kVA rating. The line-interactive DVR with the proposed algorithm can compensate for an input voltage sag or an interruption within a 2ms delay. The developed DVR can effectively compensate for a voltage sag or interruption in sensitive loads, such as computers, communications equipment, and automation equipment.

Key Words: DFT (Discrete Fourier Transform), DVR (Dynamic Voltage Restorer), Line-Interactive, PLL(Phase-Locked Loop), RMS variation detector, Voltage sag or Interruption

I. INTRODUCTION

Recently computers, communication devices and automation devices have come into wide use in the office, in industry, and even in people's homes. These devices, which operate continuously for 24 hours, require a highly reliable input power. Supplying an unreliable input power to these devices brings about severe losses to customers. One type of input power disturbances is a voltage sag or interruption due to a fault in the interconnected power system [1], [2].

A compensator for voltage sag or interruption is called a DVR (Dynamic Voltage Restorer) [3]. A DVR for voltage sag does not require an energy storage unit, while a DVR for voltage interruption does. DVRs are divided into two types with reference to the connection pattern. A DVR connected in series with a load through a transformer is the most common structure [4]. One severe disadvantage of this configuration is its high system losses due to continuous operation. Another disadvantage is its delicate protection due to the series connection of the system.

A DVR connected in parallel with a load and operated with a line-interactive scheme is another structure. One strong advantage is its relatively low system rating and losses since this type of DVR operates only during the disturbance time. However, one disadvantage is the compensation delay between the disturbance beginning point and the compensated point, which is critical in system performance. Another disadvantage is the conduction losses of the source separation switch, which conducts the load current continuously in the normal state.

A major part of the compensation delay is the detection delay of the voltage sag or interruption [5]. Instantaneous detection is a rapid way to detect a voltage sag or interruption, but it is not applicable to a distorted input voltage. RMS detection is an accurate way to detect a voltage interruption, but it has a quarter-period delay time.

This paper proposes a hybrid structure for a fast sag detection algorithm in a line-interactive three-phase DVR, which is composed of an instantaneous detector and two RMS-variation detectors. In addition, a new switching scheme for the load separation switch is proposed to offer reliable system operation. Performance verification of the proposed algorithm was carried out through computer simulations, and by experimental work with a prototype of a line-interactive DVR with a 3kVA rating.

II. PROPOSED DETECTION ALGORITHM

The waveform for one-phase voltage can be expressed by equation (1) for considering the harmonic components.

$$v(t) = \sum_{n=1}^{N} V_n \sin(n\omega t + \theta_n). \quad (1)$$

If the voltage waveform is composed of only the fundamental component, the value of n is equal to 1. Otherwise, the value of n is an integer larger than 1. In the case of a sinusoidal input voltage, it is easy to detect a sag or interruption quickly and precisely by checking the instantaneous value.

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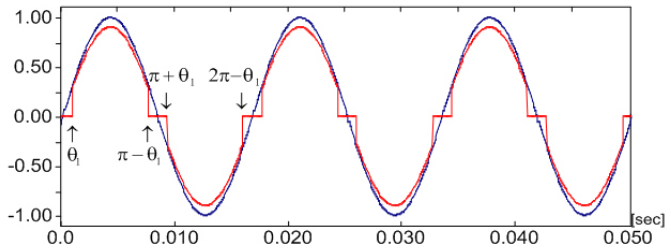


Fig. 1. Principle of instantaneous sag- detection.

However, real input voltage contains harmonic components, which bring about difficulties in detecting voltage sags and interruptions. The RMS detection scheme was proposed to solve this weak point. However, this method causes a delay in detection because it takes time to compute the RMS value from the instantaneous value.

In order to eliminate these weak points, this paper proposes a novel algorithm, which includes instantaneous detection and RMS variation detection using the DFT method [6].

The measured input voltage is converted into a signal with unit magnitude. It is then divided by the peak value as in the following equation:

$$v_{pu} = v(t)/v_{peak}. \tag{2}$$

Normally input voltage has distortion. Therefore, this voltage is converted into a unit sine signal passing through the PLL circuit [7]. This unit sine signal is used to generate a reference signal for instantaneous sag detection. The reference signal has 90% of the unit sine signal around the peak point, and a value of zero around the zero-crossing point as shown in Fig. 1.

The reference signal for instantaneous detection v_{sag_ref} can be expressed by equation (2) as follows:

$$v_{sag\_ref} = \begin{cases} 0.9 \times \sin \omega t, & \theta_1 \le \theta \le \pi - \theta_1 \\ 0, & -\theta_1 < \theta < \theta_1 \end{cases} \tag{3}$$

where, θ_1 is 20°, and the sine value of θ_1 is 0.3.

When the input voltage is distorted, the reference signal for instantaneous sag detection is as shown in Fig. 3. When the voltage signal is lower than the reference, the instantaneous detection scheme identifies it as a voltage sag, although it is not. Therefore, a double checking scheme is required. In the proposed algorithm, the RMS variation of the fundamental component is measured to judge the voltage sag. Then a DFT (Discrete Fourier Transform) algorithm is used to calculate the RMS value of the fundamental component.

The source voltage $v(t)$ can be expressed as the following equation using the Fourier series.

$$v(t) = \frac{a_0}{2} + \sum_{n=0}^{\infty} a_n \cos n\omega_0 t + \sum_{n=0}^{\infty} b_n \sin n\omega_0 t. \tag{4}$$

The fundamental component for n=1 is obtained as in equations (5) and (6), by separating the real and imaginary parts.

$$a_1 = \frac{2}{T}\int_0^T v(t)\cos\omega_0 t \; dt \tag{5}$$

$$b_1 = \frac{2}{T}\int_0^T v(t)\sin\omega_0 t \; dt. \tag{6}$$

By applying the DFT to equations (5) and (6), equations (7) and (8) are obtained as follows:

$$a_1 = \frac{\sqrt{2}}{N}\sum_{i=0}^{N} v\left(t - i\frac{T}{N}\right)\cos\left(2\pi\frac{i}{N}\right) \tag{7}$$

$$b_1 = \frac{\sqrt{2}}{N}\sum_{i=0}^{N} v\left(t - i\frac{T}{N}\right)\sin\left(2\pi\frac{i}{N}\right). \tag{8}$$

Using the values of a_1 and b_1, the RMS value of the fundamental component can be easily obtained as follows:

$$V_{RMS} = \sqrt{a_1^2 + b_1^2}. \tag{9}$$

Fig. 2 shows the structure of the hybrid detection method which consists of an instantaneous detector, RMS variation detector-1, and RMS variation detector-2. The source voltage passes through the sliding-window DFT and RMS calculations, and the instantaneous sag detector. If an instantaneous sag is detected, the RMS variation detector-1 is selected and the present RMS value is stored at $X1$. While the instantaneous sag is present, the same procedure is repeated 8 times. It takes 0.8ms because the control period is 100us. The final

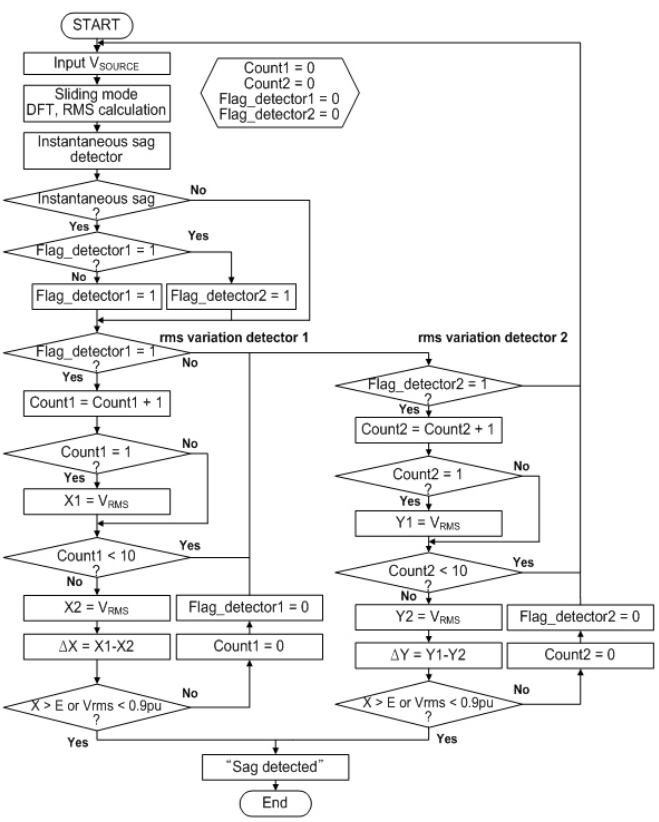


Fig. 2. Hybrid detection method for voltage interruption.

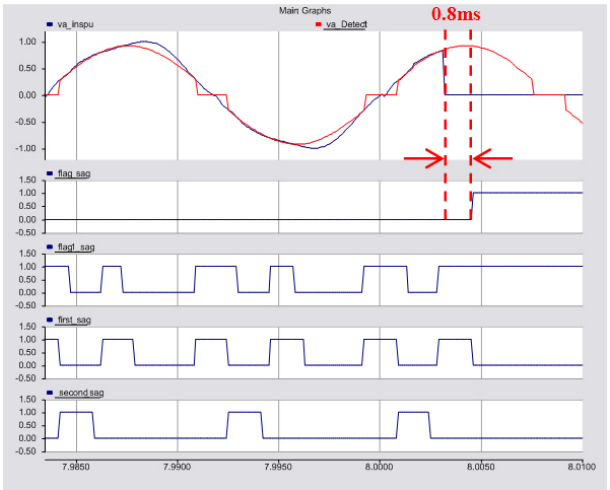


Fig. 3. Instantaneous detection scheme for A-phase input voltage.

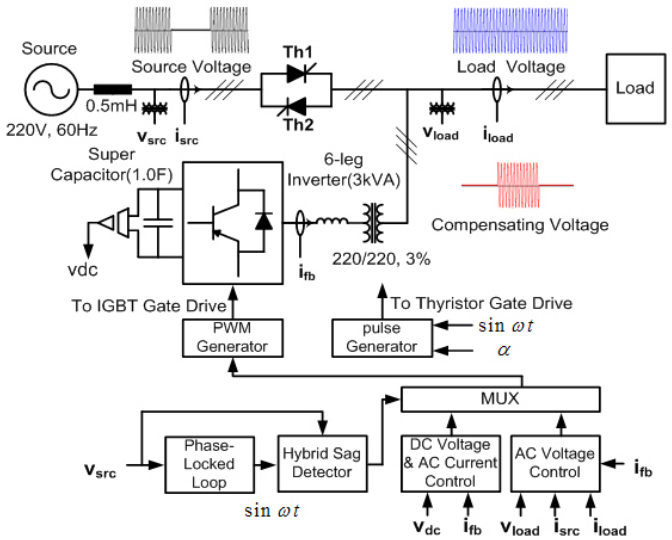


Fig. 4. Configuration of proposed three-phase DVR.

RMS value is stored at $X2$ to calculate the RMS variation, $\Delta X = X2 - X1$. If the RMS variation ΔX is larger than ΔE or the RMS voltage is less than 0.9, the sag is acknowledged. Otherwise, the next input is processed.

If an instantaneous sag occurs while the RMS variation detector-1 is under operation, it is impossible to calculate the RMS variation within 1ms. Therefore, the RMS detector-1 can not successfully detect the actual sag. In order to remove this weak point, the RMS variation detector-2 starts to operate at this moment. Therefore, two state machines of a RMS variation detector operate in parallel with complementary roles. The critical value ΔE is determined by the minimum RMS variation obtained at the instant when the 0.9 sag occurs at $n\pi + 20°$. The proposed algorithm offers a fast detection of voltage sag, which allows the DVR to compensate for it within 2.0ms.

Fig. 3 shows the simulation results obtained from the proposed sag detection algorithm. The instantaneous sag is detected when the input voltage is lower than the reference signal as shown in the 3rd graph. Two RMS variation detectors are selected according to the operation flow shown in Fig. 2. Although the two RMS variation detectors are selected many times under instantaneous sag situations, the calculated RMS variation is larger than the critical value. It is confirmed that there is no real sag for the first cycle. According to the 2nd graph, it is known that the detection delay is about 0.8ms.

III. LINE-INTERACTIVE DVR

A. SYSTEM CONFIGURATION

Fig. 4 shows the configuration of a DVR with the proposed algorithm including the source and the load. The DVR consists of three full-bridge inverters to control each phase voltage, a super-capacitor, a power transformer, anti-parallel thyristor switches, and a system controller. In the normal state the source supplies power directly to the load through the thyristor switch. When a voltage interruption occurs, the controller detects the disturbance and the inverter supplies nominal voltage through the power transformer by discharging the super-capacitor, in which the anti-parallel thyristor switch turns off to separate the sources.

When the source is recovered, the compensating voltage is removed by cutting off the gate signals for the inverter. The thyristor switch turns on to supply power from the source. After a few seconds elapse, the inverter starts charging the super-capacitor to be ready for the next disturbance.

The measured source voltage is sent to the phase-locked loop to obtain the unit sine signal, which is needed to calculate the reference value for instantaneous sag detection. DFT operation is carried out in the sliding-window pattern for a half-period of the power frequency. The source voltage is passed through the hybrid detection flow in Fig. 2. Once the sag is detected, the inverter injects a sinusoidal voltage obtained from the current and voltage control procedures.

The DC voltage and AC current of three full-bridge inverters are sent to the DC voltage and AC current control. The load voltage and current, the source current, and the full-bridge inverter current are sent to the AC voltage control. The output of these control blocks are sent to the MUX. The output of the MUX is sent to the PWM pulse generator. The unit sine from the phase-locked loop is sent to the gate pulse generator for the anti-parallel thyristor switches.

The size of the super-capacitor bank is determined depending on the duration of the voltage interruption and the size of the connected load. It is assumed that the voltage interruption has a duration of 4 seconds and that the load has a power rating of 3kVA. Therefore, the total energy to be released during a voltage interruption is designed to be 12kJ. The bank of the super-capacitor is designed considering the size of the energy storage, the DC link voltage, the voltage and the current rating of each capacitor unit. Table I shows the specification of the selected super-capacitor.

TABLE I
SPECIFICATION OF SUPER-CAPACITOR

Rated working voltage	2.7 VDC
Operating temperature	-40 to +60°C
Nominal Cap. Range	100F
Equivalent Series Resistance	0.014 Ω(@ 1kHz)

The bank is designed to utilize the upper 20% of the maximum storage capacity, considering the expandability of the operation capacity. The maximum current flows through the super-capacitor bank when it discharges the maximum power. The minimum voltage across the super-capacitor bank can be determined with the maximum discharge power and the current rating.

It is assumed that the super-capacitor is charged by 2.5V, which is 92% of the maximum charging voltage of 2.7V, considering an 8% margin. The lowest discharge voltage is determined to be 2.0V. Therefore, the minimum DC link voltage and the lowest discharge voltage determine the number of super-capacitor units. 100units of super-capacitors were connected in series to provide enough of a safety margin.

B. THYRISTOR SWITCH OPERATION

The line-interactive DVR with the proposed algorithm has an anti-parallel thyristor switch at each phase as in Fig. 5. It holds the on-state in normal operation, and disconnects from the source when a sag or interruption occurs.

If the inverter starts to compensate when the thyristor switch is on, the inverter current flows into the source side instead of the load side. Since the source impedance is very small, the inverter supplies over-current and burns down and the load voltage can not be restored. Because of this, the inverter starts to compensate after the thyristor switch turns off by compulsion.

The gate pulse for the thyristor switch is normally supplied for $180°$ in the case of resistive load. However, in the case of an inductive or capacitive load, it should be supplied for more than $180°$. In this paper, the gate pulse was supplied for $270°$, which was considered enough phase shift due to the load type. The gate pulses for $Th1$ and $Th2$ are supplied for 1.5π. Both of the gate pulses are overlapped for 0.5π two times in every cycle as shown in Fig. 5. One band is located between 0.5π and π, while the other is located between and 1.5π and 2π.

At band 1, since both the gate pulses for $Th1$ and $Th2$ are in the on-state, both the source voltage and the inverter voltage are positive at the instant of sag. After both of the thyristor gate pulses are removed after detecting the sag, $Th1$ turns off and $Th2$ holds the conduction state. This causes a reverse current flow. In order to prevent this reverse current, the system detects the load current and makes both of the thyristor switches turn off.

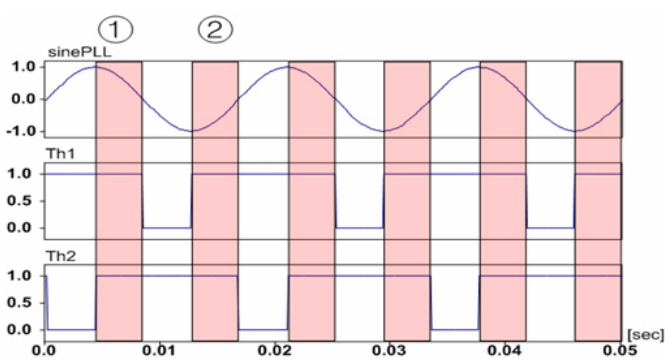


Fig. 5. Gate pulse supplying for thyristor switch.

At band 2, since both the gate pulses for $Th1$ and $Th2$ are in the on-state, both the source voltage and the inverter voltage are negative at the instant of sag. After both of the thyristor gate pulses are removed after detecting the sag, $Th2$ turns off and $Th1$ holds the conduction state. This causes a reverse current flow. In order to prevent this reverse current, the system detects the load current and makes both of the thyristor switches turn off.

When a voltage sag occurs, the inverter injects a voltage after the controller turns off the thyristor switch by checking the phase angle of the source voltage and that of the source current. Equation (10) represents the inverter output voltage in order to turn off the thyristor switch.

$$v_{inv} = v_{src}K_T + L\frac{I_{src}}{K_T T} \tag{10}$$

where, L is the leakage inductance of the transformer, T is the control operation period, K_T is the turn ratio of the transformer, and I_{src} is the source current at the instant of sag.

The turn-off time of the thyristor switch is determined by dividing the calculated source voltage by the minimum inverter voltage. The thyrisor switch is turned off considering the voltage difference due to the transformer characteristics.

C. INVERTER OUTPUT VOLTAGE CONTROL

When a sag or interruption occurs, the full-bridge inverter supplies the load with a nominal voltage after preventing the reverse current flow. Fig. 6 shows a voltage control scheme developed for a full-bridge inverter. Using the general P control method gives rise to a steady-state error and distortion depending on the load characteristic. Therefore, open-loop control is the best method to avoid distortion of the output voltage. The leakage reactance and the AC capacitor connected to the inverter output terminal operate as a LC filter to cut off the harmonics due to the switching operation.

The general open-loop scheme cannot generate the output voltage without distortion because it brings about overshoot and oscillation for the step change of the inverter voltage. In order to solve this problem, the capacitor current is measured and its differential value is added to the inverter voltage control. This method also offers a rapid rise for the output voltage. However, the magnitude of the output voltage varies depending on the size of the load. Therefore, the output voltage is adjusted by calculating the effective value for one period right after the compensation is completed. This can overcome the weak point of open loop control for the output voltage.

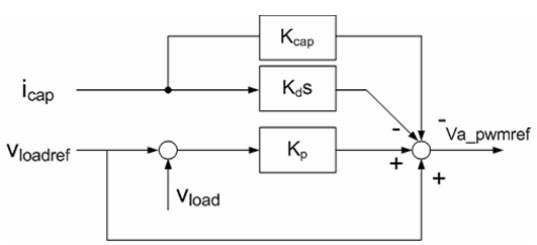


Fig. 6. Inverter output voltage controller.

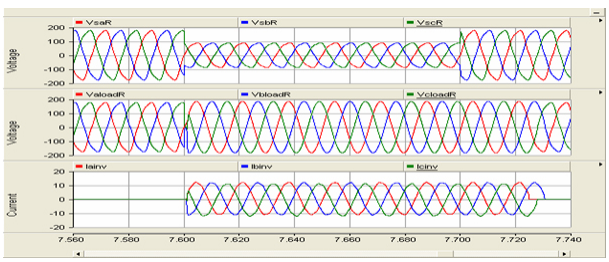
IV. SIMULATION

Many computer simulations with PSCAD/EMTDC software were carried out for analysing the performance of the proposed DVR. The power circuit and controller were modelled as closely as possible to the real system, by using passive and active components, and the built-in control block in PSCAD/EMTDC software. Particularly, the controller was designed using a user-defined model programmed with C code to implement the control action and PWM pulse generation as accurately as possible. It is very effective to implement the hardware controller using a DSP. Table II shows the circuit parameters for the 3kVA DVR system considered in the simulation.

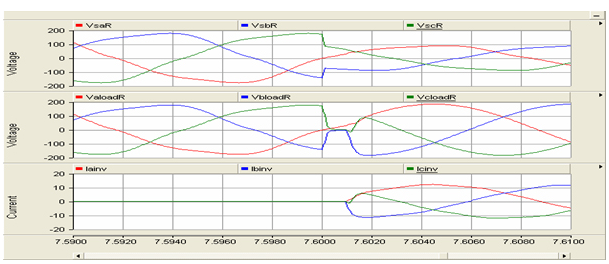
TABLE II
SPECIFICATION OF SUPER-CAPACITOR

Voltage Rating	220V, 60Hz
Power Rating	3kVA
Source Reactance	0.5mH
Energy Storage Capacitor	1.0F
Power Transformer	3kVA, 220:220, 3%
IGBT switch	600V, 200A
Switching Frequency	10kHz

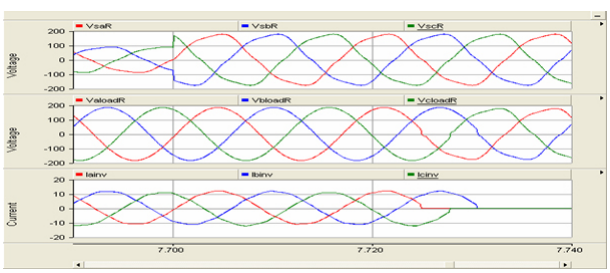
Fig. 7(a) shows the source voltage, the load voltage, and the compensating current from the inverter when a 50% voltage sag occurs. The load voltage maintains a constant value because the inverter injects a nominal voltage during the sag.



(a) Source voltage, load voltage, compensating current

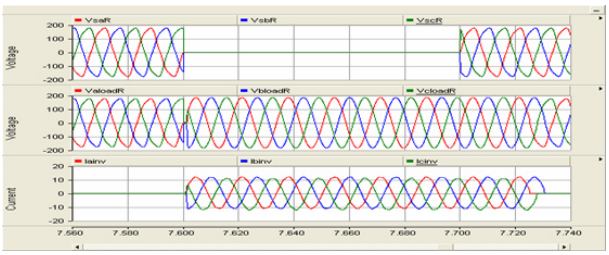


(b) Expanded waveform at sag beginning point

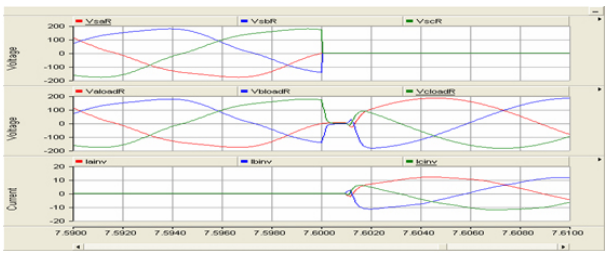


(c) Expanded waveform at sag ending point

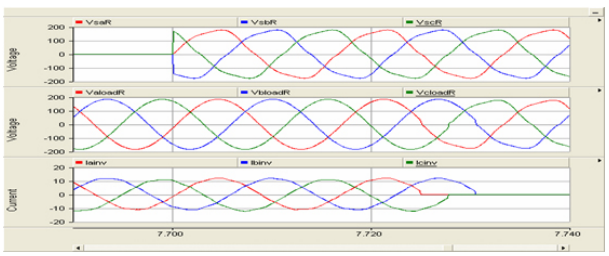
Fig. 7. Simulation results for voltage sag.



(a) Source voltage, load voltage, compensating current



(b) Expanded waveform at interruption beginning point



(c) Expanded waveform at interruption ending point

Fig. 8. Simulation results for voltage interruption.

Fig. 7(b) and 7(c) show expanded waveforms focusing on the sag beginning and ending points. The load voltage is restored within 2.0ms after the instant when the voltage sag occurs. This delay is due to the sag detection time and the turn-off time of the thyristor switch.

Fig. 8(a) shows the source voltage, the load voltage, and the compensating current from the inverter when a voltage interruption occurs. The load voltage maintains a constant value because the inverter injects a nominal voltage during the interruption.

Fig. 8(b) and 8(c) show expanded waveforms focusing on the interruption beginning and ending points. The load voltage is restored within 2.0ms after the instant when the voltage interruption occurs. This delay is due to the interruption detection time and the turn-off time of the thyristor switch. The inverter continuously supplies the load voltage for 20ms after the instant when the voltage sag is restored to confirm the turn-on state of the thyristor switch.

V. PROTOTYPE EXPERIMENT

A prototype of the proposed DVR was built and tested to confirm the feasibility of the hardware implementation, based on the simulation results. The prototype is composed of three full-bridge inverters to control each phase voltage, a gate-drive circuit, a super-capacitor bank, a power transformer, an anti-parallel thyristor switches, a display circuit, and a DSP controller as shown in Fig. 9. The circuit parameters for the hardware prototype are exactly same as the ones in Table II.

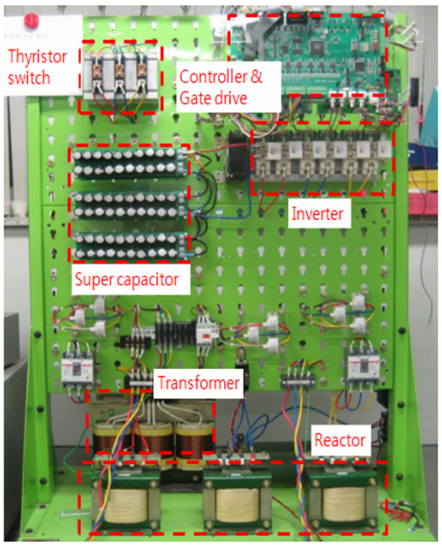
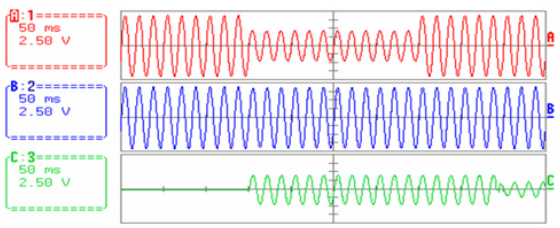
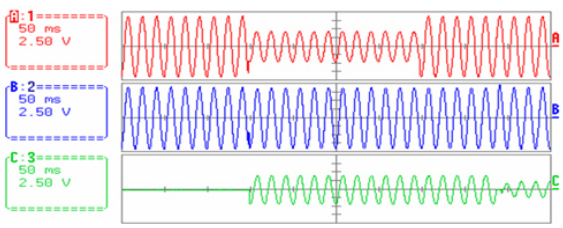


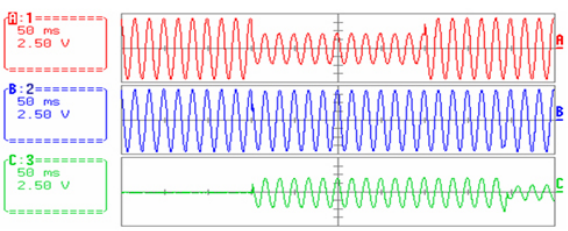
Fig. 9. Prototype of proposed Line-interactive DVR.



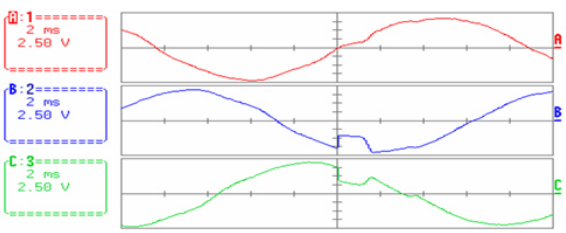
(a) A-phase Source voltage, load voltage, compensating current



(b) B-phase Source voltage, load voltage, compensating current



(c) C-phase Source voltage, load voltage, compensating current



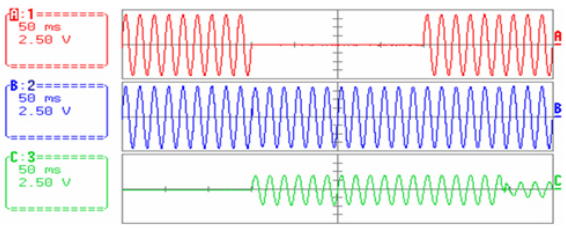
(d) Expanded waveform of load voltage at sag beginning point

Fig. 10. Experiment results for voltage sag.

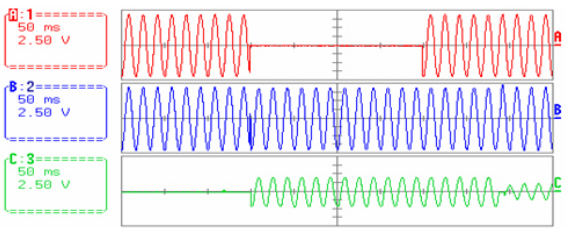
One remarkable feature of the proposed DVR is its fast detection and compensation. The DVR utilizes the algorithm described in chapter II. This fast detection algorithm can be implemented during real time operation using a high performance DSP controller. The DSP controller offers a display function, which monitors the whole system operation and indicates the number of voltage disturbances in real time.

The DSP controller was designed using a TMS320vc33 DSP chip for real time operation and an EPLD chip for logic implementation. The proposed DVR sets the operation frequency automatically by checking the source voltage when the system starts up. All operations are carried out automatically when the main switch is turned on.

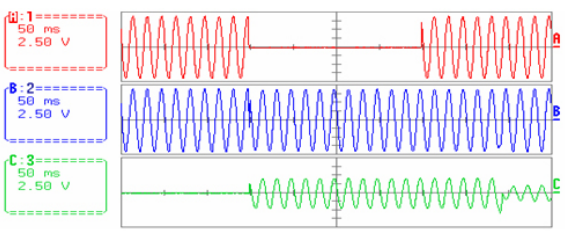
Fig. 10(a), 10(b) and 10(c) show the source voltage, the load voltage, and the compensating current from the inverter when a 50% voltage sag occurs. The load voltage maintains a constant value as confirmed by the simulation results. Fig. 10d shows an expanded waveform focusing on the sag beginning point. The load voltage is restored within 2.0ms as confirmed



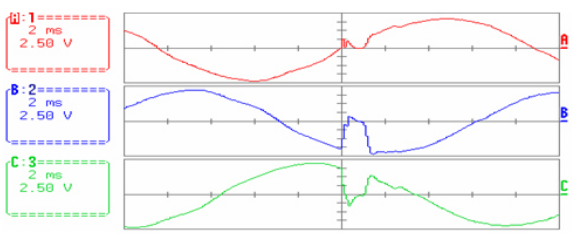
(a) A-phase Source voltage, load voltage, compensating current



(b) B-phase Source voltage, load voltage, compensating current



(c) C-phase Source voltage, load voltage, compensating current



(d) Expanded waveform of load voltage at interruption beginning point

Fig. 11. Experiment results for voltage interruption.

by the simulation results. This delay is due to the sag detection time and the turn-off time of the thyristor switches.

Fig. 11(a), 11(b) and 11(c) show the source voltage, the load voltage, and the compensating current from the inverter when a voltage interruption occurs. The load voltage maintains a constant value as confirmed by the simulation results. Fig. 11(d) shows an expanded waveform focusing on the starting point of the interruption. The load voltage is restored within 2.0ms as confirmed by the simulation results. This delay is due to the sag detection time and the turn-off time of the thyristor switch. Through the experimental results, it is confirmed that the proposed DVR can restore the input voltage within 2.0ms from the instant when the source disturbance occurs.

VI. CONCLUSIONS

The developed detection algorithm has a hybrid structure composed of an instantaneous detector and two RMS-variation detectors. The source voltage passes through the instantaneous sag detector. If an instantaneous sag is detected, the RMS variation detector-1 is selected to calculate the RMS variation. The RMS variation detector-2 is selected when the instantaneous sag occurs under the operation of the RMS variation detector-1.

The feasibility of the proposed algorithm was verified through computer simulations and experiments with a prototype of a line-interactive three-phase DVR with a 3kVA rating. The line-interactive DVR with the proposed algorithm can compensate for an input voltage sag or interruption within 2ms.

The DVR system with the proposed algorithm has a maximum allowable duration of 4 seconds. It can effectively compensate for voltage interruptions in sensitive loads, such as computers, automation equipment, and communications equipment. It has a simple structure that can be easily implemented with commercially available components and it is highly reliable in operation.

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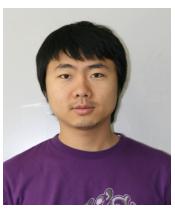

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