

Design of a Cascaded H-Bridge Multilevel Inverter Based on Power Electronics Building Blocks and Control for High Performance

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Abstract

This paper proposes a practical design for a Cascaded H-Bridge Multilevel (CHBM) inverter based on Power Electronics Building Blocks (PEBB) and high performance control to improve current control and increase fault tolerance. It is shown that the expansion and modularization characteristics of the CHBM inverter are improved since the individual inverter modules operate more independently, when using the PEBB concept. It is also shown that the performance of current control can be improved with voltage delay compensation and the fault tolerance can be increased by using unbalance three-phase control. The proposed design and control methods are described in detail and the validity of the proposed system is verified experimentally in various industrial fields.

Key Words: Cascaded H-bridge multilevel inverter, PEBB, PWM synchronization, Unbalance three-phase control, Voltage delay compensation

I. INTRODUCTION

Multilevel power conversion has been receiving increasing attention in the past few years for high power applications. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive applications in the recent literature [1], [2]. These converters are suitable in medium voltage and high power applications due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating. In the family of multilevel inverters, topologies based on series connected H-bridges are particularly attractive because of their modularity and power quality. Fig. 1 shows the power circuit configuration of a Cascaded H-Bridge Multilevel (CHBM) inverter composed of multi-phases [3], [4].

The main features of CHBM inverters for high-power motor drives are: 1) reduced harmonic injection into the utility by means of specially designed transformers which provide phase shifting of the secondary windings; 2) the ability to generate Fig. 1. The power circuit of CHBM inverter composed of multi-phase & multi-level. near-sinusoidal voltages with only low frequency switching; 3) they have almost no common-mode voltage; 4) they are low dv/dt at output voltage; 5) they do not generate significant over-voltage on the motor terminal even if the distance between the inverter and motor is long;

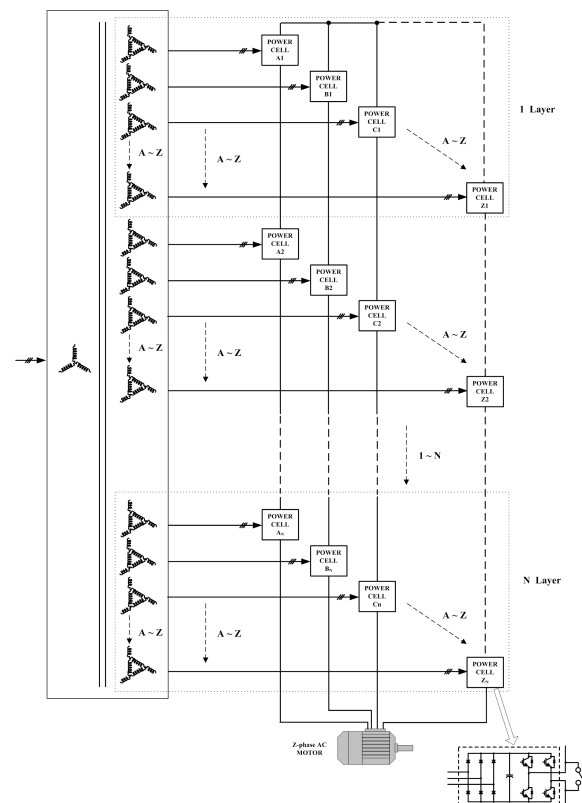


Fig. 1. The power circuit of CHBM inverter composed of multi-phase & multi-level.

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6) they are constructed using a series of low voltage cells in spite of a high voltage motor drive; 7) their voltage rate can be easily increased due to the modular design of the power modules; 8) they consist of a series of H-bridge (single-phase full-bridge) inverter units [5], [6].

However, the commercialization of CHBM inverters have many obstacles. These include the complexity of PWM implementation for controlling many electric power semiconductor devices, the lack of a flexible control structure to cope with various voltages and powers, control for high performance and fault tolerance. This paper proposes a practical design for a CHBM inverter and a high performance control to improve current control and increase fault tolerance.

II. DESIGN OF A CASCADED H-BRIDGE MULTILEVEL INVERTER BASED ON PEBB

A. Control Architecture

The need for low-cost, highly reliable, modular, easy to use and maintain CHBM inverters is fueling the drive for standardized Power Electronics Building Blocks (PEBB) [7]–[10].

This paper proposes a new distributed digital control architecture for CHBM inverters. The proposed architecture features a high level of flexibility and modularity. It also

paves the way towards future Plug and Play CHBM inverters. In a general distributed controlled multilevel inverter, the main controller includes the speed and current controllers for generation of the voltage/current command for variable speed operation, and the individual controller for each module generates the PWM signal based on the control command from the main controller. In the proposed method, Controller Area Network (CAN) serial communication [11], which is a standard protocol, is used for data transmission between the main and individual module controllers (cell controllers). In addition, PWM generation, Automated Voltage Regulation (AVR), and independent monitoring and protection are performed in each individual module. The overall system configuration and the features of the main and cell controllers, the CAN communication, and the inverter modules are summarized in Fig. 2. The controllers of the system consist of the main and cell controllers. The main controller includes a speed controller, which calculates the voltage/current command value that is required to control the speed of the motor. It also performs observation, diagnosis, monitoring, protection, Man-Machine Interface (MMI), communication, and auxiliary functions at a system level. The cell controllers, located at each module, control the phase shift and the required PWM voltage calculated by the system controller. Each individual cell unit has its own observation and protection function. The cell controller is connected to the main controller via a high speed link that utilizes an optical cable, and the data exchange is performed via serial communications. The main controller consists of a high quality DSP (TMS320C31) and auxiliary circuitry, and the cell controllers consist of lower cost DSPs (TMS320LF2406A), which are one-chip controllers with the auxiliary circuit function embedded. The communications between the main and cell controllers use CAN communication. The communication interval and the type of data exchanged between the controllers are summarized in Table 1. The overall system schematic and control scheme for the CHBM inverter, for an induction motor drive, is shown in Fig. 3. The instantaneous values of the voltage references for each of the power cells are provided via a fiber optic communications link between the main control board and the cell control board located within each power cell. PWM generation & phase-shift and automated voltage regulation are performed in each individual power cell, which can be simplified via a standardized communication protocol (CAN). All of the necessary data for proper power cell operations are encoded in the packet. All the status information and the sensed variables are sent back to the main controller providing full control over the inverter operation. The PWM synchronization information becomes active only after a communication interrupt is received from the main controller. The four main parameters required for proper operation of the PWM generator are the 1) receive interrupt, 2) voltage reference, 3) switching period, and 4) total number of power cells.

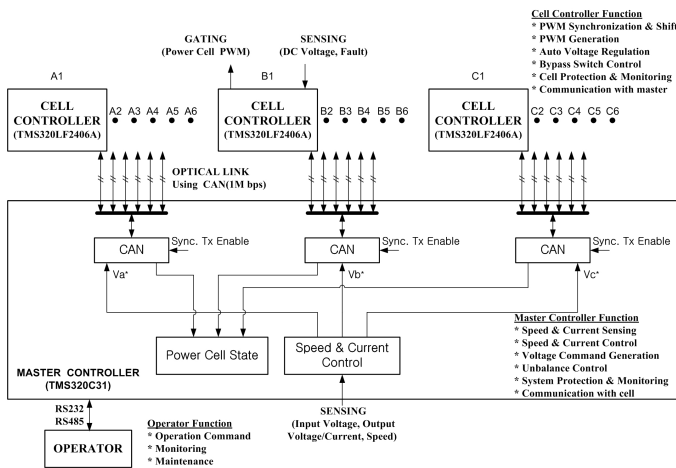


Fig. 2. A control block diagram with the proposed design based on PEBB.

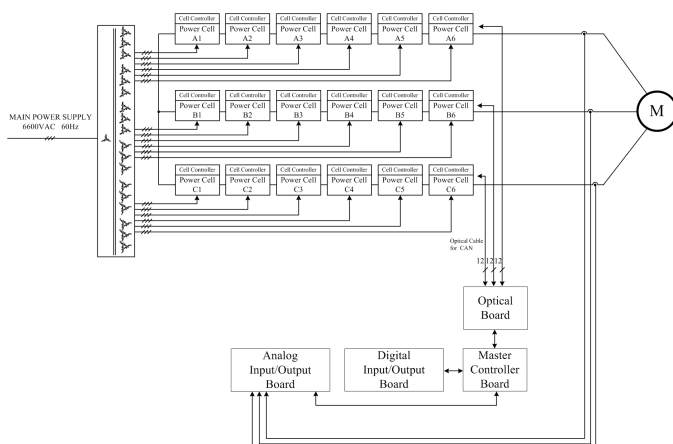


Fig. 3. The overall system configuration for CHBM inverter.

B. PWM Implementation

CHBM inverters can be implemented through a series connection of single-phase modular inverters. This paper

TABLE I
MAIN / CELL COMMUNICATION DATA

Main ⇒ Cell (Interval : Sampling Time)	Cell ⇒ Main (Interval : Sampling Time*N)
1. Sequence (Run, Stop) 2. Voltage Reference (Instantaneous Value) 3. Switching Period 4. Power Cell Total Number per Phase 5. Failed Power Cell Number 6. Failed Power Cell Location 7. Response Power Cell	1. Power Cell Number 2. Communication Check 3. Power Cell Fault 4. DC Link Voltage

presents a method that allows these modular inverters to be implemented and operated to synchronize their PWM carriers, fundamental references and sampling instances to implement a network-controlled cascaded inverter with distributed PWM computation and overall optimal system performance.

In the proposed method, the PWM signal is generated in each individual module; therefore, the PWM signals must be synchronized. The PWM synchronization and phase shift method performed in the proposed 6 layer multilevel inverter is shown in Fig. 3. As can be seen, the PWM of each module is synchronized based on the CAN communication receive interrupt. Each module individually calculates the phase shift time using the following:

$$\text{Phase Shift Time} = [(K - 1)/N] * \frac{T_s}{2} \quad (1)$$

where K and N represent the individual and total number of single-phase inverters per phase. Each module generates a delayed PWM signal by a timer inside each cell controller, as shown in Fig. 4, for generation of the instantaneous voltage command. Since each series connected inverter unit is electrically isolated, the phase voltage is a sum of the output voltage

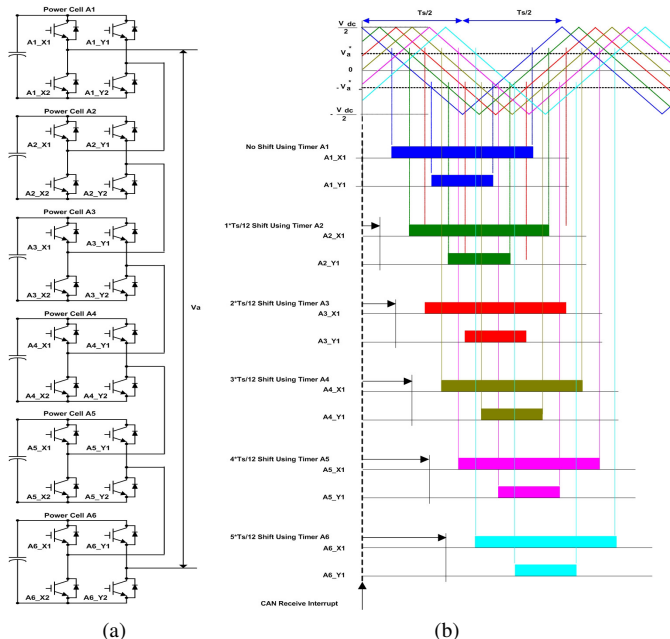


Fig. 4. (a) CHBM inverter composed of 6-layer per phase (b) PWM synchronization & phase-shift method based on the CAN communication receive interrupt.

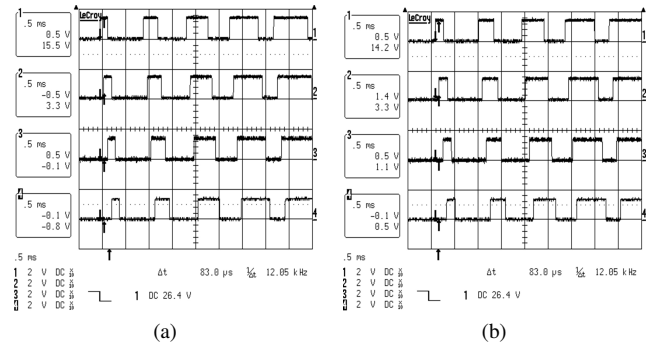


Fig. 5. Gating Signals of A phase inverter module (83µs between channels).

(a) Ch.1: A1_x1, Ch.2: A2_x1, Ch.3: A3_x1, Ch.4: A4_x1
(b) Ch.1: A3_x1, Ch.2: A4_x1, Ch.3: A5_x1, Ch.4: A6_x1
(X axis: 500µs/div., Y axis: 20V/div.)

of each inverter module.

The PWM phase-shift signals for gate X1 of each power cell A1, A2, A3, A4 are shown in Fig. 5(a), and the PWM phase-shift signals for gate X1 of each power cell A3, A4, A5, A6 are shown in Fig. 5(b). The phase-shift time is calculated using equation (1). The phase A output voltages of inverter modules 1 and 2, measured when the inverter is operated using the proposed CAN serial communication interrupt, are shown in Fig. 6. It can be seen that the phase delay between the two inverters is 83[µs], which is the phase delay calculated using equation (1) with a 1000[µs] sampling time for a 13-level CHBM inverter. The measured line to line output voltage is shown in Fig. 7. It can be seen that a 13-level phase voltage can be produced with the CHBM inverter.

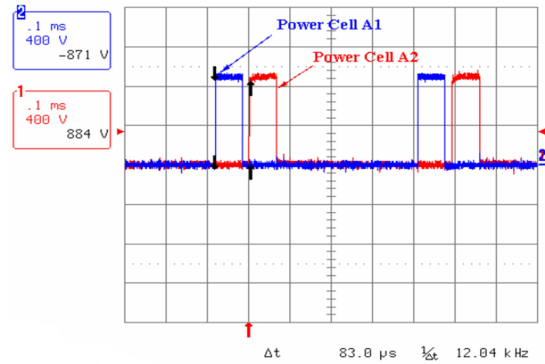


Fig. 6. Phase-shifted output voltage of inverter module 1 and 2. (X axis: 100µs/div., Y axis: 400V/div.)

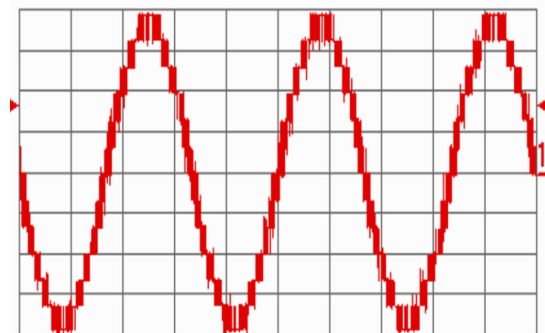


Fig. 7. Output phase voltage. (X axis: 5ms/div., Y axis: 1500V/div.)

III. CONTROL FOR HIGH PERFORMANCE

A. Voltage Delay Compensation of Current Controller

This paper proposes an analysis of the voltage delay and compensation for current control in CHBM inverters for a medium voltage motor drive with vector control. It is shown that the expansion and modularization characteristics of the CHBM inverter are improved when using Phase-Shifted Pulse Width Modulation (PSPWM) since the individual inverter modules operate more independently. However, the PSPWM of a CHBM has a phase difference between the reference voltage and real voltage, which can cause instability in the current controller at high speeds where the ratio of the sampling frequency to the output frequency is insufficient [12]–[14]. This instability in the current controller is removed by adding the proposed method which compensates for the phase difference between reference voltage and real voltage. The proposed method is suitable for HBML inverters controlled by PSPWM with a low switching frequency and a high-speed motor drive.

Fig. 8 shows the voltage delay compensation at a vector control using a CHBM inverter and PSPWM. The CHBM inverter generates a delayed output voltage by equation (2), and the rotor flux angle angular ω_e is shifted in the d-q synchronous reference frame by equation (3). Equation (4) can eliminate the instability of the current controller by using phase compensation.

$$V_{ABC_delay} = \frac{T_S}{2N} \times \frac{(N-1)}{2} \quad (2)$$

$$\theta_{shifted\ phase} = \frac{(N-1)T_S}{4N} \times \omega_e \quad (3)$$

$$\begin{aligned} V_{ds_comp}^{s*} &= V_{ds}^{s*} \cos \theta_{shifted\ phase} - V_{qs}^{s*} \sin \theta_{shifted\ phase} \\ V_{qs_comp}^{s*} &= V_{ds}^{s*} \sin \theta_{shifted\ phase} + V_{qs}^{s*} \cos \theta_{shifted\ phase} \end{aligned} \quad (4)$$

where

T_S : sampling time of the current controller.

N : number of single-phase inverters per phase.

ω_e : angular speed of the d-q synchronous reference frame.

V_{ds}^{s*}, V_{qs}^{s*} : reference voltage of the d-q stationary reference frame.

Fig. 9 (a) shows the instability of the torque & flux component currents in a synchronous reference frame by the output voltage delay in the vector control mode when PSPWM is adopted at the CHBM inverter. In the proposed method, the current controller remains stable because the ripples of the torque & flux component currents do not change because of an increase in motor speed after the compensation as can be seen in Fig. 9 (b).

B. Proposed Unbalance Three-Phase Control Using Offset Voltage

The unbalance three-phase control method can increase the fault tolerance of CHBM inverters under the condition of faulty power cells [15], [16]. It is possible to generate a balance three-phase line-to-line voltage by phase-shifting and bypassing the faulty power cells with a minimum voltage drop. In this method, the concept of voltage modulation by using

offset voltage [17], [18] is applied to an unbalance three-phase control method. Especially, it is possible to use the maximum output voltage of an inverter by adopting the real time unbalance control of phase voltage irrespective of the fault location or the number of disabled power cells. Fig. 10 shows a vector diagram for unbalance control when there are faults in power cells of B3 (B-phase), C2, C3, C4, C5, C6 (C-phase).

The proposed control method is based on balance three-phase voltage modulation using an offset voltage. The various balance three-phase voltage modulation methods can be obtained by changing the offset voltage. It is a feature of the balance three-phase voltage modulation using an offset voltage. It does not change the phase voltage when the pole voltage is added to the offset voltage. Namely, the offset voltage is a hidden freedom in three-phase voltage modulation using an offset voltage because $V_{as} + V_{bs} + V_{cs} = 0$. The proposed control method is shown in the three parts of a control block diagram (Fig. 11).

The three parts of the proposed control method are suggested in the following:

- 1) Calculation of the Unbalance Gain: It calculates the respective output voltage gain when the inverter operates with faulty power cells.
- 2) Calculation of the Neutral Point Shift Gain: It calculates the neutral point voltage for balance three-phase.
- 3) Calculation of the Output Voltage Limit: It calculates the maximum achievable output voltage.

The unbalance gain is calculated as a separate three-phase (phase A, phase B, and phase C).

$$\alpha = \frac{\text{total layer number in phase A}}{\text{total remained number in phase A}} \quad (5)$$

$$\beta = \frac{\text{total layer number in phase B}}{\text{total remained number in phase B}} \quad (6)$$

$$\gamma = \frac{\text{total layer number in phase C}}{\text{total remained number in phase C}} \quad (7)$$

where, the total layer number is the number of power cells in each phase. The total remained number is equal to the “total layer number - the number of faulty power cells at each phase”. Therefore, if all of the power cells are normal, then they are equal to “1” and if the any of power cells is faulty, then they are more than “1”.

For output voltage balancing, the offset voltage is calculated by equation (8).

$$V_{sn_comp}^* = - \int \left(\frac{V_{max}^* + V_{min}^*}{2 \times G_{max}} \right) dt \quad (8)$$

where G_{max} is obtained from the maximum value of α, β and γ (equation (9)).

$$G_{max} = \max(\alpha, \beta, \gamma). \quad (9)$$

V_{max}^* and V_{min}^* are obtained by equation (10), (11).

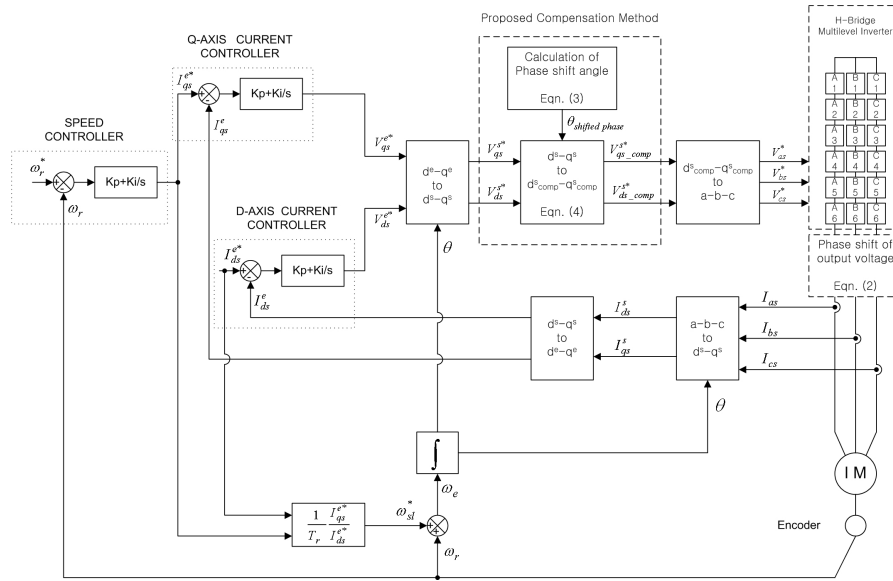


Fig. 8. Phase delay compensation block diagram of a current controller.

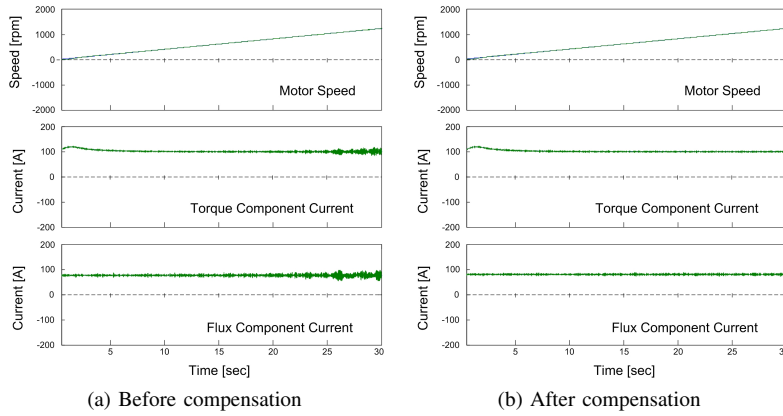


Fig. 9. Vector control results before & after compensation.

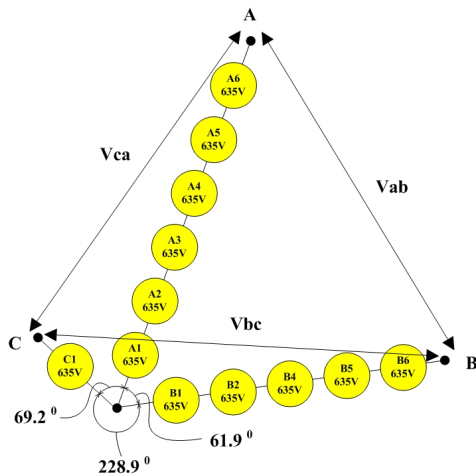


Fig. 10. Vector diagram for three-phase unbalance control.

The maximum achievable amplitude of the inverter output voltage is determined by equation (12).

$$V_{limit} = \left(\min \left(\frac{1}{\alpha} + \frac{1}{\beta}, \frac{1}{\beta} + \frac{1}{\gamma}, \frac{1}{\gamma} + \frac{1}{\alpha} \right) \right) \times \frac{1}{2} \times \frac{V_{dc}}{\sqrt{3}} \quad (12)$$

Under the condition of the inverter operating with faulty power cells, the respective voltage references $V_{an_comp}^*$, $V_{bn_comp}^*$, and $V_{cn_comp}^*$ can be expressed as:

$$\begin{aligned} V_{an_comp}^* &= (V_{as}^* + V_{sn_comp}^*) \times \alpha \\ V_{bn_comp}^* &= (V_{bs}^* + V_{sn_comp}^*) \times \beta \\ V_{cn_comp}^* &= (V_{cs}^* + V_{sn_comp}^*) \times \gamma. \end{aligned} \quad (13)$$

The balance line-to-line voltage, when applied to a three-phase balance induction motor, produces a balance motor phase voltage because the motor neutral is not connected to the inverter neutral N, whose potential is shifted due to the faulty power cells.

$$V_{max}^* = \max(V_{an_comp}^*, V_{bn_comp}^*, V_{cn_comp}^*) \quad (10)$$

$$V_{min}^* = \min(V_{an_comp}^*, V_{bn_comp}^*, V_{cn_comp}^*). \quad (11)$$

A three-phase output current with / without unbalance three-phase control, when power cells are damaged in a CHBM

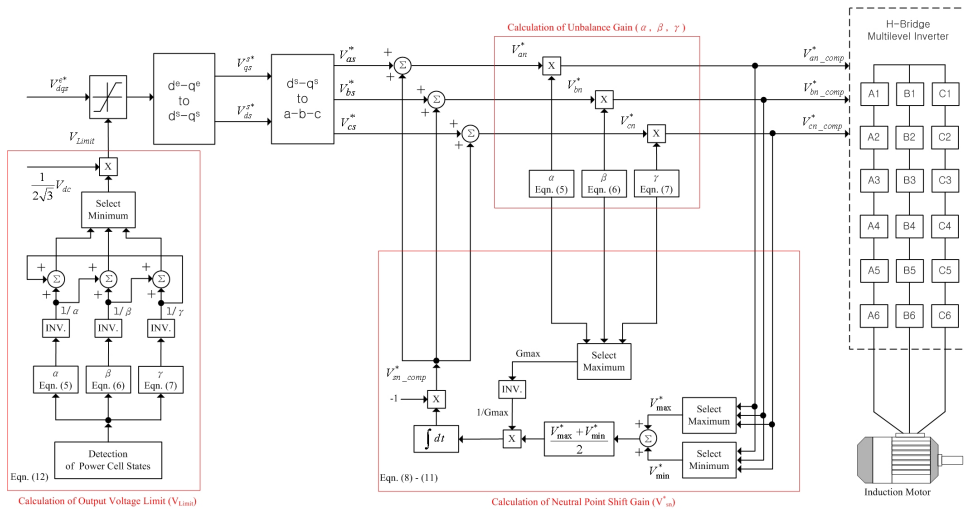


Fig. 11. Control block diagram of three-phase unbalance control.

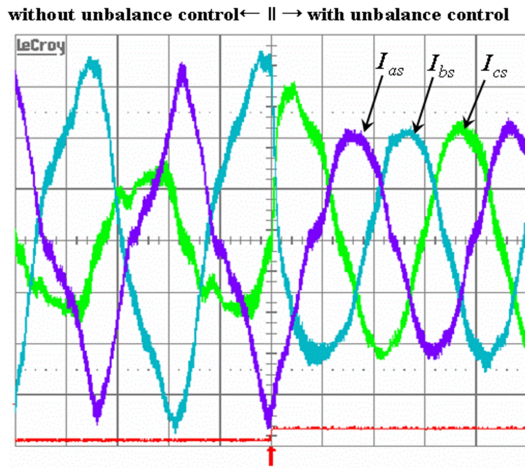


Fig. 12. Output current without/with unbalance three-phase control, condition of 15[Hz](X axis: 20ms/div., Y axis: 50A/div.).

inverter, is shown in Fig. 12. The output three-phase current is unbalanced without unbalance three-phase control, whereas it is balanced with unbalance three-phase control.

IV. EXPERIMENTAL STUDY

A 6,600[V] 2,000[kVA] three-phase 13-level CHBM inverter prototype, where each inverter module is rated at 635[V] 111[kVA], has been manufactured for testing purposes, as shown in Fig. 14. A 6,600[V] 1,400[kW] induction motor was operated under the full load condition to test the proposed design of a CHBM inverter based on PEBB and control for high performance. Fig. 13 shows the circuit configuration of a 13-level CHML inverter fed induction motor drive for 6,600[V] 2,000[kVA] operation. The DC sources for each single-phase IGBT inverter were obtained from three-phase diode rectifiers powered by an extended-delta power transformer with 18 secondary windings. There is a 10° phase shift between all of the adjacent secondary windings of the transformer to eliminate the dominant low order harmonics in the line current. Each of the blocks (power cells) consist of a single-phase

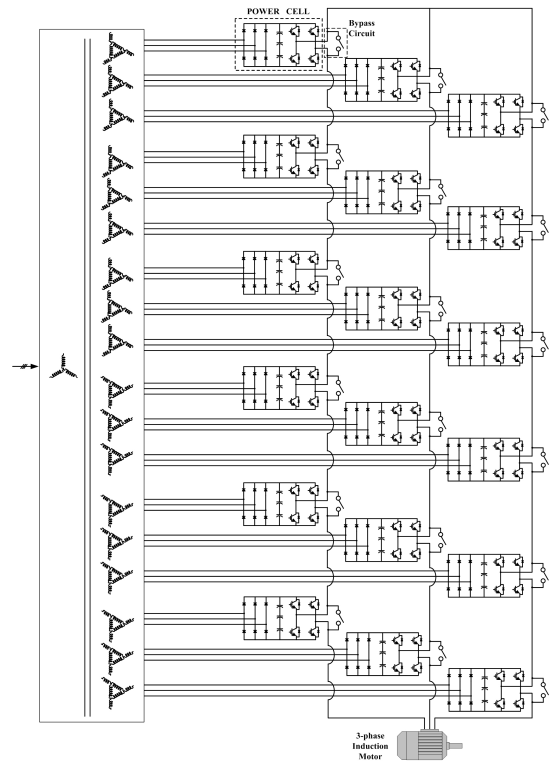


Fig. 13. The power circuit of CHBM inverter composed of three-phase & 13-level.

IGBT inverter unit, as can be seen in the inverter configuration in Fig. 13. Six series-connected IGBTs for each phase provide a rated voltage of 3,811[V] per phase, yielding a rated line-to-line voltage output of 6,600[V]. The output voltage from multiple inverters becomes a stepped waveform voltage similar in shape to a sinusoidal waveform. Each cell cabinet houses 6 cells per output phase, as can be seen in a photograph of the hardware used for the experimental evaluation in Fig. 14.

The voltage of each output phase is the sum of the horizontal cell voltages. Each cell can be disconnected and removed from the cabinet by disconnecting the three-phase input power, the

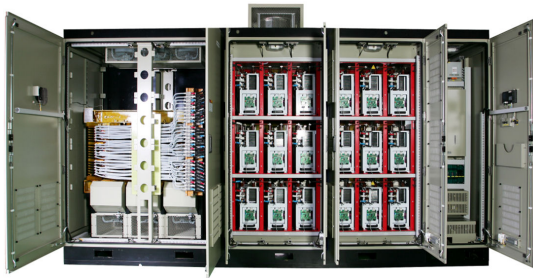


Fig. 14. The 6,600[V] 2,000[kVA] CHBM inverter hardware used for experimental evaluation.

two output connections, and the fiber optic cable. All of the cells are electrically and mechanically identical, so they may be interchanged. Each cell contains its own control boards, which communicate with the system through an isolated link using fiber optic cables. By using a multiple winding input transformer, the CHML inverter has multi-pulse rectification and more than meets the requirements of IEEE-519 as can be seen in Fig. 15. This reduces the harmonic current distortion on the power source and protects the other equipment in the plant.

As a result of PSPWM, the output waveform of Fig. 16 is close to a sine wave, and the heat loss caused by harmonics is negligible. In addition, the harmonic currents in the motor are minimized so there is very little torque ripple on the output shaft and very little risk of torsional load resonance. Fig. 17 shows possible application in various industrial fields such as blowers, induced draft fans, pumps, and generator drives.

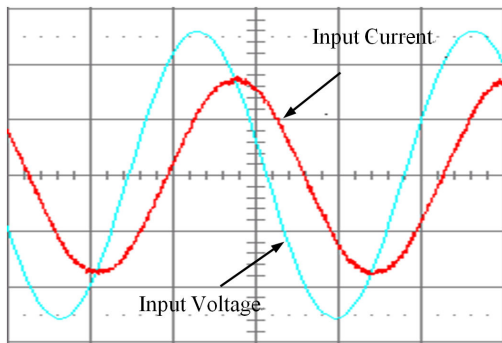


Fig. 15. Input voltage and current.
(voltage X axis: 5ms/div., voltage Y axis: 4,000V/div.)
(current X axis: 5ms/div., current Y axis: 150A/div.)

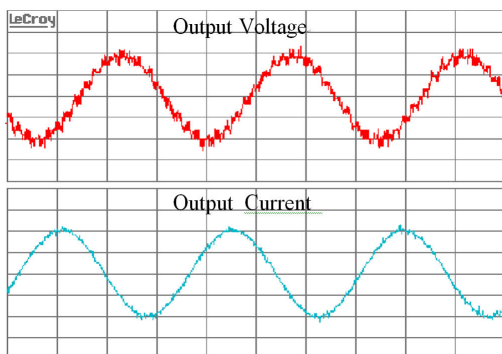
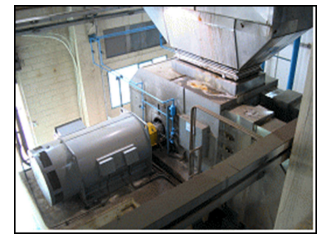


Fig. 16. Output voltage and current.
(voltage X axis: 5ms/div., voltage Y axis: 5,000V/div.)
(current X axis: 5ms/div., current Y axis: 150A/div.)



(a) Blower of sewage disposal plant



(b) Induced draft fan of waste crematory



(c) Hot water pump of steel plant



(d) Generator drive for transformer test

Fig. 17. Installation of a various industrial fields.

V. CONCLUSIONS

The design of a CHBM inverter based on PEBB and control for high performance have been proposed and experimentally verified in this paper. It has been shown that the expansion and modularization characteristics of the CHBM inverter have been improved since individual inverter modules operate more independently. It has also been shown that the performance of the current control can be improved with voltage delay compensation in the case of a higher speed where the ratio of the sampling frequency to the output frequency is insufficient. Furthermore, the fault tolerance of a CHBM inverter can be increased by unbalance three-phase control.

We proposed and verified a new design concept and control method for CHBM inverters in various industrial fields. The favorable features of proposed design and control methods are summarized in the following:

- Improvement of the expansion and modularization characteristics based on the PEBB concept in CHBM inverters
- Practical implementation of PWM synchronization & a phase-shift method for CHBM inverters based on a standard serial communication protocol
- Compensation of current control when using PSPWM
- Fault tolerance irrespective of the fault location or the number of disabled power cells

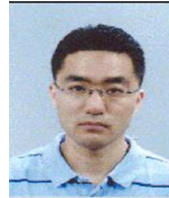
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