Efficient Hybrid Carrier Based Space Vector Modulation for a Cascaded Multilevel Inverter

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Abstract

This paper presents a novel hybrid carrier based space vector modulation for cascaded multilevel inverters. The proposed technique inherits the properties of carrier based space vector modulation and the fundamental frequency modulation strategy. The main characteristic of this modulation are the reduction of power loss, and improved harmonic performance. The carrier based space vector modulation algorithm is implemented with a TMS320F2407 digital signal processor. A Xilinx Complex Programmable Logic Device is used to develop the hybrid PWM control algorithm and it is integrated with a digital signal processor for hybrid carrier based space vector PWM generation. The inverter offers less weighted total harmonic distortion and it operates with equal electrostatic and electromagnetic stress among the power devices. The feasibility of the proposed technique is verified by spectral analysis, simulation, and experimental results.

Key Words: Cascaded multilevel inverter, Carrier based space vector modulation, Digital signal processor, Power loss analysis, Weighted total harmonic distortion

I. INTRODUCTION

Multilevel inverters have become a popular choice in recent years, because improving the output waveform of an inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by the switching operations [1]. Various multilevel converters structures are reported in the literature, and the cascaded multilevel inverter appears to be superior to other multilevel structures in applications at high power ratings due to its modulation, control and protection of each full bridge inverter [2]. The power circuit for a five level cascaded inverter topology, shown in Fig. 1, is used to examine the proposed PWM technique.

Modulation control of any type of multilevel inverter is quite challenging, and much of the reported research is based on somewhat heuristic investigations. Switching losses in high power converters represent an issue and any switching transitions that can be eliminated without compromising the harmonic content of the final waveform are considered advantages [3]. Most of the modulation methods developed for multilevel inverters are based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition PWM), or with horizontal displacements (phase-shifted PWM) [4].

A special kind of hybrid multilevel inverter topology was realized based on the combination of a gate turn-off thyristor (GTO) inverter and an insulated gate bipolar transistor (IGBT) inverter with non-identical dc voltage sources for high power drives applications [5]. A generalized hybrid converter structure was also developed for improving waveform quality, and power processing capability, while reducing switching loss [6]. This hybrid approach was also extended for multilevel power conversion systems [7]. These techniques [5]–[7] concentrate mainly on converter structure improvement for achieving more output voltage levels. Space vector modulation (SVM) offers low harmonic distortion for three-phase inverters by placing the most unwanted harmonics power on triplen harmonics.

SVM is intrinsically a non-carrier-based digital technique for generating switching angles. However, due to the constant sampling rate used in SVM, equivalent carrier-based techniques have been developed. Carrier-based SVM is appropriate for inverters with more than five levels, where the computational overhead for conventional SVM is exceeded due to many output states [8]. Wenxi Yao suggested that these techniques are harmonically equivalent, with the best spectral performance being achieved when the nearest three space vector states are selected with the middle two vectors centered in each half carrier switching interval [9]. This strategy is known as carrier based space vector pulse width modulation (CBSVM). These high-frequency methods produce high-frequency stepped-voltage waveforms that are easily filtered by the load and, therefore, present very good reference tracking and low-current harmonic distortion. However, this also causes high switching losses, which is undesirable in high-power
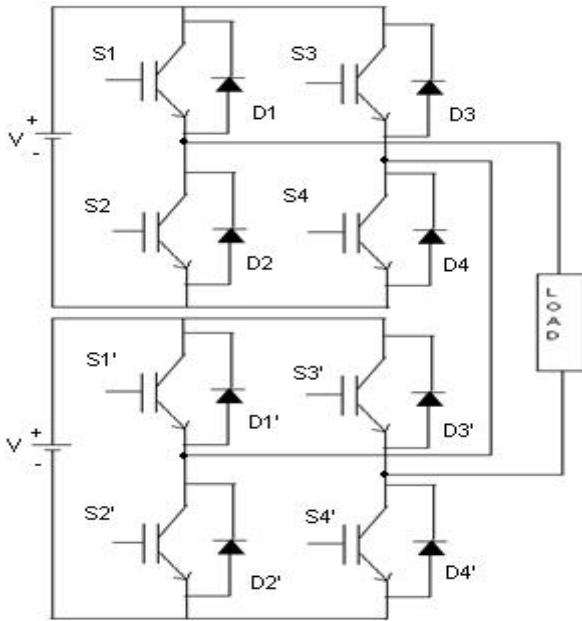
Fig. 1.   Schematic diagram of the inverter topology (one phase leg) used to verify the proposed five-level hybrid CBSVM method.

applications.

In this paper, a new modulation technique is proposed based on hybrid modulation to address the reduction of switching losses in a multilevel inverter, with improved harmonic performance. This paper is organized in the following way. Section 2 describes the development of a hybrid carrier based space vector modulation suitable for cascaded multilevel inverters. Section 3 presents the harmonics and a power loss analysis of a cascaded multilevel inverter with the proposed modulation. Section 4 illustrates the simulation and experimental results of different operating points and a discussion of the results. Finally, some conclusions are presented in section 5.

II. HYBRID CARRIER BASED SPACE VECTOR MODULATION DEVELOPMENT

The principle behind this hybrid modulation is to mix fundamental frequency PWM and carrier based space vector modulation for each inverter module of a cascaded multilevel inverter. Therefore, the output contains the features of fundamental frequency PWM and CBSVM. In this modulation technique, the four switches of each inverter module are operated at two different frequencies, two being commutated at the fundamental frequency, while the other two switches are pulse width modulated at CBSVM. Unfortunately, this arrangement causes different switching losses and therefore differential heating among the switches. In order to overcome this problem, a sequential switching scheme is embedded in this hybrid modulation. Fig. 2 shows the general structure of the proposed hybrid CBSVM method. It consists of a base PWM generator and a hybrid PWM controller to generate the new modulation pulses.

A. Base PWM Generation

Carrier based space vector modulation is derived from the addition of a common offset voltage to the three-phase

references. This will center the active space-vectors in the switching period, and hence match the carrier modulation to get optimized space vector modulation [10]. The offset voltage V_{off}' for multilevel operation can be calculated as:

$$V_{off} = -\frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2}$$

$$V_k' = (V_k + V_{off} + V_{dc}) \bmod \left(\frac{2V_{dc}}{N-1}\right), \ k = a, b, c$$

$$V_{off}' = \frac{V_{dc}}{N-1} - \frac{\max(V_a', V_b', V_c') + \min(V_a', V_b', V_c')}{2}$$

where V_{dc} is 1 p.u. The phase reference is then obtained by adding V_{off} and V_{off}' to the reference waveform V_a, V_b, or V_c.

In this carrier based N level PWM, operation consists of (N-1)/2 different carriers, where all of the carriers are out of phase with φ. The carriers have the same frequency f_c, the same peak to peak amplitude A_c, and are disposed so that the bands they occupy are contiguous. They are defined as:

$$C_i = A_c \left((-1)^{f(i)} y_c(f_c, \varphi) + i - \frac{N}{2}\right), \ i = 1, \ldots, N-1$$

where y_c is a normalized symmetrical triangular carrier defined as $y_c(f_c, \varphi) = (-1)^{[\alpha]}((\alpha \bmod 2) - 1) + \frac{1}{2}$.

$\alpha = \frac{2\pi f_c t + \varphi}{\pi}$, φ represents the phase angle of y_c. y_c is a periodic function with the period $T_c = 2\pi/\omega_c$. The modulation index is defined as $M = \frac{A_m}{KA_c}$, where A_m is the peak amplitude of the modulation waveform and A_c is the amplitude of the carrier waveform.

The modulation frequency ratio is also defined as $mf = \frac{f_c}{f_1}$, where f_1 is the fundamental frequency. In this modulation strategy, three base PWM signals are required for each module operation. The sequential signal (A) is a square wave signal with a 50% duty ratio and half of the fundamental frequency. This signal makes every power switch operate under CBSVM and fundamental frequency PWM sequentially to equalize the power losses among the switches. Fundamental frequency PWM (B) is a square wave signal synchronized with a modulation waveform; B=1 during the positive half cycle of the modulation signal, and B=0 during negative half cycle. Carrier based SVM (C and D) is based on a comparison of the modified sinusoidal reference signal $(V_k + V_{off} + V_{off}')$ with each carrier to determine the voltage level that the inverter should switch to. A sequential switching signal and fundamental frequency PWM signals are the same for all full bridge converter cells in each phase. The base PWM signals (A, B, C and D) for a hybrid PWM controller are shown in Fig. 4.

B. Hybrid PWM Controller

A hybrid PWM controller is implemented using a simple combinational logic, and hence, it can be processed very quickly. The functions of the combinational logic for a five level hybrid PWM are expressed as:

$$V_{off} = -\frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2}$$

$$V_{off}' = \frac{V_{dc}}{N-1} - \frac{\max(V_a', V_b', V_c') + \min(V_a', V_b', V_c')}{2}$$
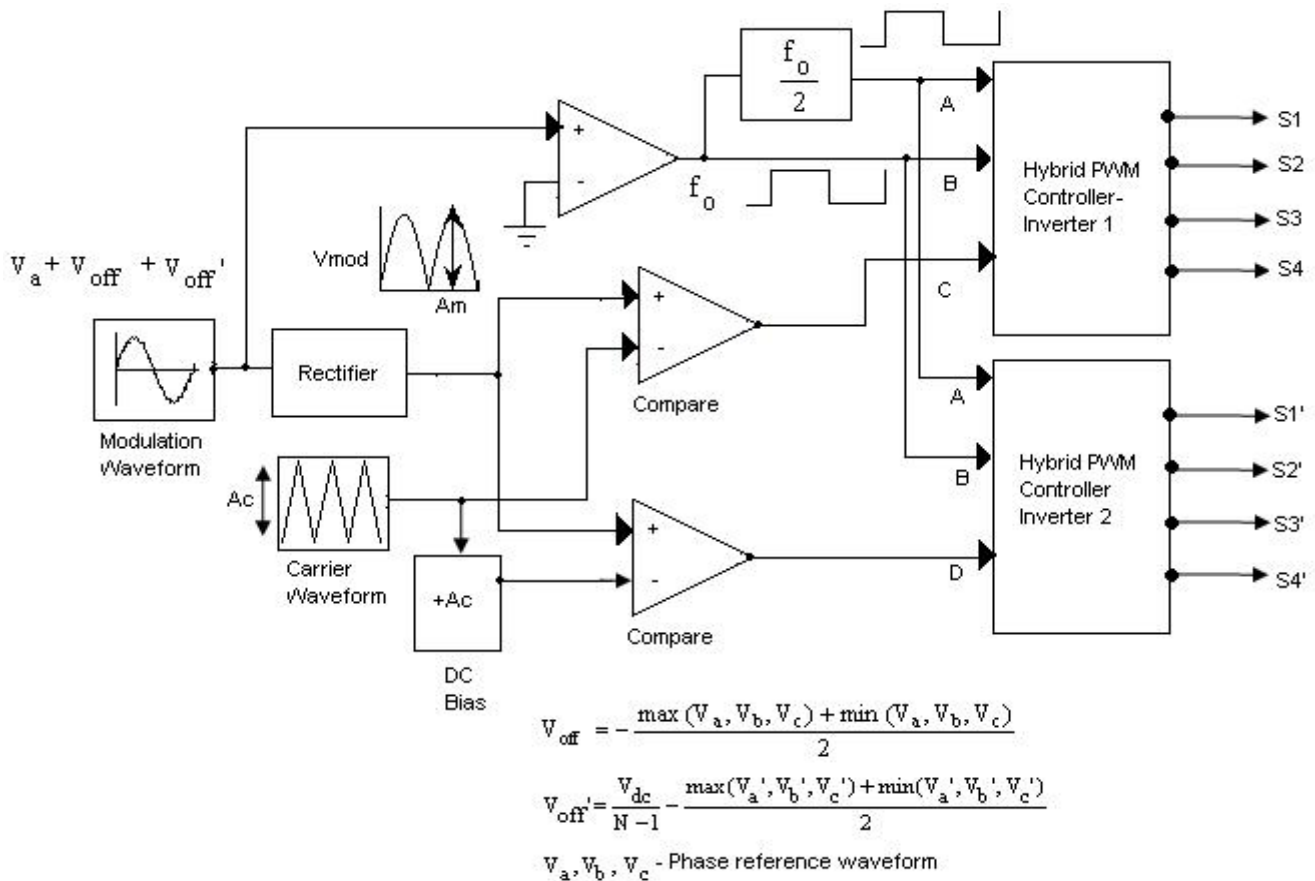
V_a, V_b, V_c - Phase reference waveform
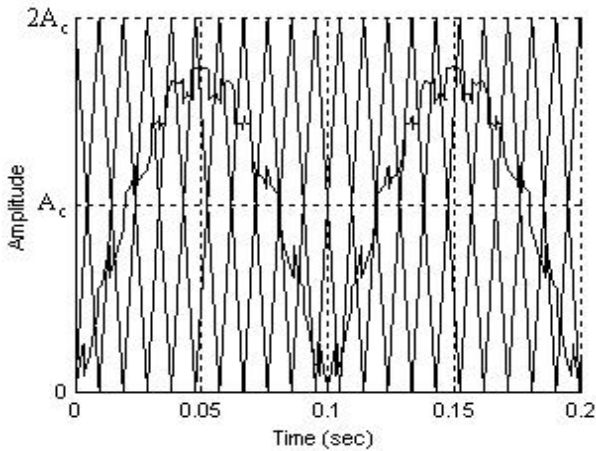
Fig. 2.　Scheme of hybrid carrier based space vector modulation.

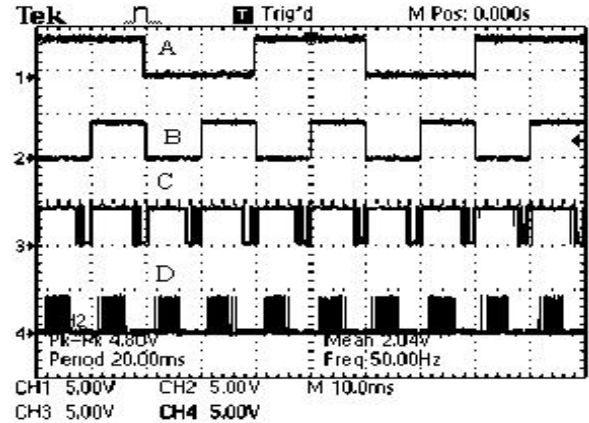Fig. 3.　Modulation and carrier waveforms for five level CBSVM.

Fig. 4.　Base PWM signals for five-level hybrid CBSVM.

$$S1 = ABC + \bar{A}B \qquad S1' = ABD + \bar{A}B$$
$$S2 = \bar{A}BC + \bar{A}\bar{B} \qquad S2' = \bar{A}BD + \bar{A}\bar{B}$$
$$S3 = \bar{A}\bar{B}C + A\bar{B} \quad \text{and} \quad S3' = \bar{A}\bar{B}D + A\bar{B}$$
$$S4 = \bar{A}\bar{B}C + AB \qquad S4' = \bar{A}\bar{B}D + AB$$

where A is a sequential signal, B is a fundamental frequency PWM, C is a CBSVM for inverter-I, and D is a CBSVM

for inverter-II. In Fig. 5, it is shown that each gate signal is composed of both fundamental frequency PWM and CBSVM pulses. If the sequential switching signal A=1, S1, S2, S1' and S2' are operated with CBSVM, while S3, S4, S3', S4' are operated with fundamental frequency PWM. If the sequential switching signal A=0, S1, S2, S1' and S2' are operated with fundamental frequency PWM, while S3, S4, S3' and S4' are operated with CBSVM. Since A is a sequential signal, the average switching frequency amongst the four switches is equalized. Voltage stress and current stress of the power
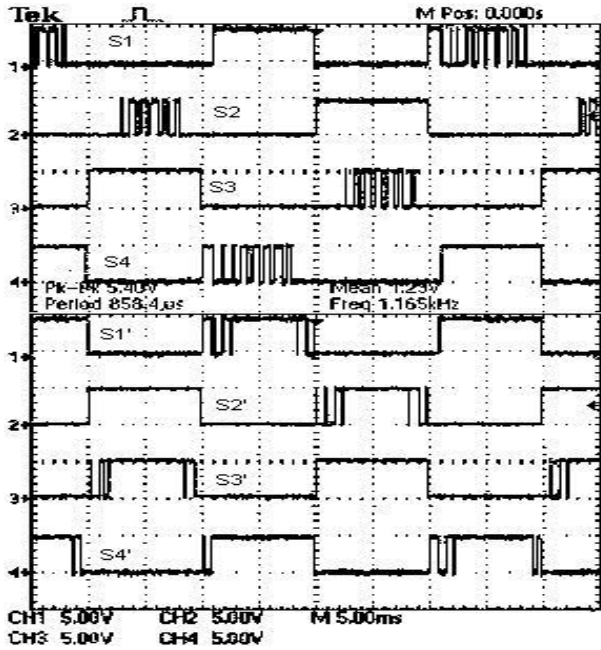
Fig. 5.   Hybrid CBSVM pulses for five-level cascaded multilevel inverter.

Fig. 6.   Voltage WTHD comparsion of hybrid CBSVM with CBSVM for five level inverter operation.

switches in each inverter bridge is also inherently equalized with this modulation.

C. Generalized Hybrid PWM Algorithm Formulation

For completeness, the generalized formulation that suits for an N level inverter and for any number of switching transitions is presented. The proposed algorithm for an N-Level Inverter is as follows:

1) Obtain the number of inverter cells K=N-1/2.
2) Modify the peak amplitude of the phase reference voltages V_a, V_b, and V_c based on the modulation index M.
3) Identify the instantaneous values of the three phase reference voltages V_a, V_b, and V_c and determine the values of V_{off} and V_{off}'.
4) The modified sinusoidal reference signal is obtained by $V_k' = V_k + V_{off} + V_{off}'$.
5) A comparison of the modified sinusoidal modulating signal with each alternative phase opposition disposition carrier signal separately is used to generate K number of CBSVM signals.
6) A common sequential signal and fundamental frequency PWM signals for each phase can be used in synchronization with the modulating signal.
7) An independent hybrid controller (combinational logic circuit) is used to mix fundamental frequency PWM and the corresponding CBSVM (X) for each inverter cell.
8) Similarly, hybrid PWM pulses are developed for all full bridge inverter modules in the N level inverter. In total 4K gate pulses per phase are developed to operate the N level cascaded multilevel inverter.
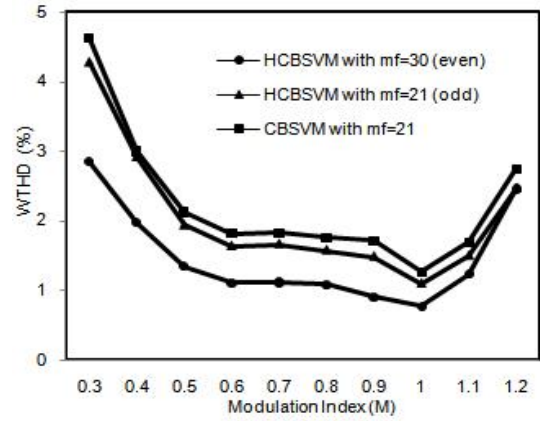
III.   PERFORMANCE ANALYSIS

A. Spectral Analysis of the output voltage and current waveform

The performance index namely the current total harmonic distortion (THD_i) and the weighted total harmonic distortion (WTHD) are chosen for the quantification of the proposed hybrid CBSVM. The weighted total harmonic distortion (WTHD) is superior to the THD as a figure of merit for a non-sinusoidal inverter waveform in which the lower portion of the frequency spectrum is weighted heavily, accurately portraying the expected harmonic current of an inductive load [11].

The WTHD uses a spectral weighting factor and is calculated using WTHD $= \dfrac{\sqrt{\sum\limits_{n=2}^{50}\left(\dfrac{V_n}{n}\right)^2}}{V_1}$ and plotted in Fig. 6. As expected, the WTHD values are lower when the modulation index is closer to unity and when the frequency ratio (mf) increases.

The current total harmonic distortion (THD_i) is defined as $THD_i = \dfrac{\sqrt{I_{rms}^2 - I_1^2}}{I_1}$, where I_{rms} and I_1 are the rms values of the output current and its fundamental component, respectively. The measured values of the THD_i at various modulation indexes for the different PWM techniques are plotted in Fig. 7. As can be seen, the hybrid CBSVM leads to the lowest current harmonic distortion among the different techniques.

B. Power Loss Analysis

A MATLAB-Simulink model of a five level inverter has been developed to study the power loss analysis. The carrier frequency f_c is 2 kHz and each converter cell is connected to a 200 V dc supply. The IGBTs selected are FF150R12KT3G, in which the maximum ratings are a forward current of 150 A and a direct voltage of 600 V. The semiconductor power losses can be estimated from the curves ($V_{sat}(\theta) \times I_1(\theta)$) ($E(\theta) \times I_1(\theta)$), presented in the datasheet of each device, where: V_{sat} is the on-state saturation voltage ($V_{ce}(\theta)$) for the IGBT and $V_F(\theta)$ for the diode; $E(\theta)$ represent the energy losses in
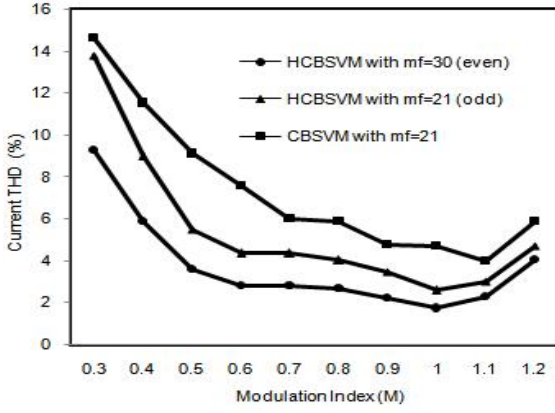
Fig. 7. THD_i comparsion of hybrid CBSVM with CBSVM for five level inverter operation.
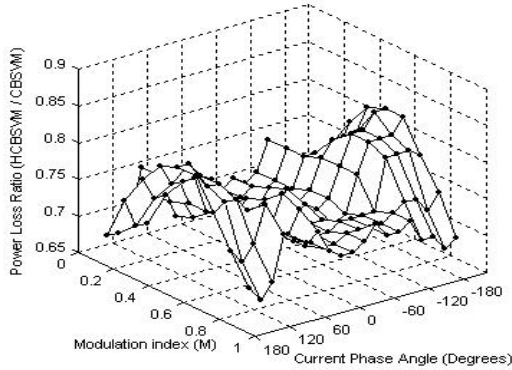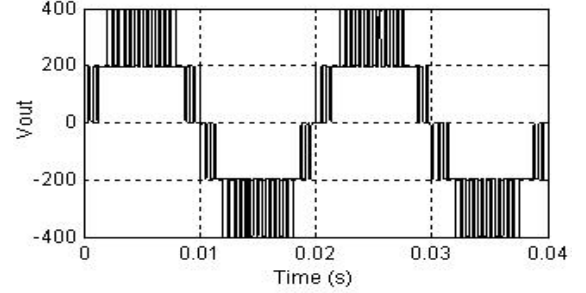

Fig. 8. Ratio of the power losses of hybrid CBSVM and conventional CBSVM fed five level cascaded inverter.

(a)

(b)

Fig. 9. Simulation results of hybrid CBSVM operation in a linear modulation region (a) Output phase voltage waveform. (b) Spectrum of the output voltage waveform.

one commutation ($E_{on}(\theta)$) if it is a turn-on commutation, E_{off} if it is a turn-off commutation and $E_{rec}(\theta)$ if it is diode reverse recovery process). These curves are used in a Matlab script developed to determine the power losses. The mathematical models are found using points extracted from the datasheets of each semiconductor device. The mathematical models obtained for an IGBT module FF150R12KT3G are given by:
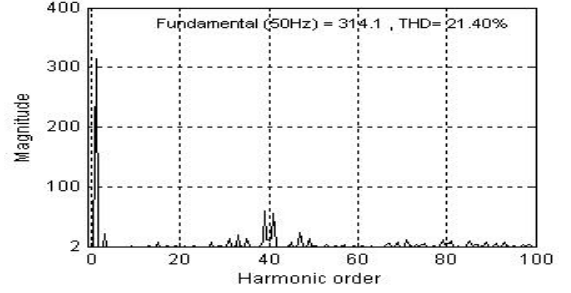
$$V_{ce} = 1.15e^{0.0026I_1(\theta)} - 0.6654e^{-0.044I_1(\theta)}$$
$$V_F = 1.2e^{0.002I_1(\theta)} - 0.7258e^{-0.0475I_1(\theta)}$$
$$E_{rec} = 0.01806e^{-0.000412I_1(\theta)} - 0.0157e^{-0.00736I_1(\theta)}$$
$$E_{on} = 0.0051e^{0.0064I_1(\theta)} - 0.0037e^{-0.00811I_1(\theta)}$$
$$E_{off} = 0.0643e^{0.00121I_1(\theta)} - 0.0647e^{-0.00107I_1(\theta)}$$
$$I_1(\theta) = M * I_{max} \sin(\theta - \delta)$$

where $I_1(\theta)$ is the load current, M is the modulation index, and δ is the load displacement angle.

Based on the models for each device, the conduction and switching power losses are calculated for each semiconductor of the inverter. The total power loss is calculated based on the sum of the switching loss and the conduction losses [12]. The switching loss for every power device (P_{sw}) is obtained separately using: $P_{sw} = \frac{1}{T} \sum (E_{on} + E_{off} + E_{rec})$ by identifying every turn-on and turn-off instant during one reference period.

The conduction power losses are those that occur while the semiconductor device is conducting current. The calculation of the conduction losses for each semiconductor of the inverter is given by:

$$P_{cond\_IGBT} = \frac{1}{2\pi} \int_0^{2\pi} V_{ce}(\theta) * I_1(\theta) * V_{cmd}(\theta) d\theta$$
$$P_{cond\_D} = \frac{1}{2\pi} \int_0^{2\pi} V_F(\theta) * I_1(\theta) * V_{cmd}(\theta) d\theta$$

where $V_{cmd}(\theta)$ is the PWM signal of the IGBT.

The sum of the conduction losses for all of the IGBT's ($P_{cond\_IGBT\_T}$) and for all of the diodes ($P_{cond\_D\_T}$) is computed to obtain the total conduction loss.

$$P_{cond\_T} = P_{cond\_IGBT\_T} + P_{cond\_D\_T}.$$

Fig. 8 shows, for the full range of the modulation index and the relative angle of the output currents, the ratio of the total power loss (switching and conduction losses) for a five level inverter with the proposed modulation strategy versus the conventional CBSVM technique. Note that the surface is always below one, which means that the power loss is significantly smaller for the proposed method. The mean value of the surface is found to be approximately 0.7326; which means the power loss reduction is about 26%. The best case is produced for a unity power factor when the modulation index is one.

IV. RESULTS AND DISCUSSION

A. Simulation Results

In order to verify that the proposed modulation can be practically implemented in a cascaded inverter, simulations were
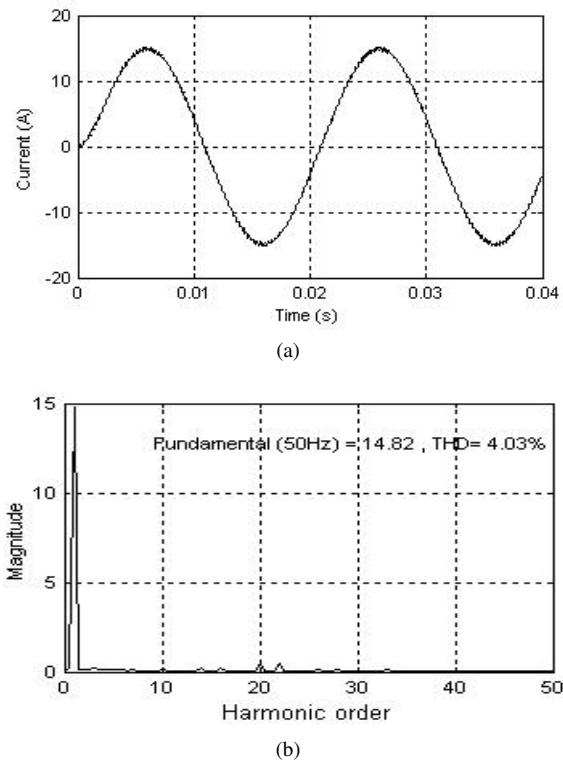
(a)

(b)

Fig. 10.   Simulation results hybrid CBSVM operation in a linear modulation region (a) Output phase current waveform. (b) Spectrum of the phase current waveform.

performed using MATLAB/Simulink. It also helps to confirm the PWM switching strategy which can be implemented in a digital signal processor (DSP) and a complex programmable logic device (CPLD). The load resistance and inductance are 20Ω and 15mH, and the dc bus voltage is set at 200 V. The inverter is operated in the linear modulation range and the corresponding voltage waveform with FFT analysis is shown in Fig. 9. It can be seen that all of the lower order harmonics are absent and that the fundamental is controlled at the pre-defined value. It is interesting to note that the next significant harmonic will be the 39th for a frequency ratio of 40.

The significant harmonics are 35, 39, 41, and 45, which are high frequency, with rms values under 11% of the fundamental term. There are some lower order harmonics in over modulation. However, the amplitude of these harmonics is not significant (below 3% of the fundamental term). In addition, the current waveform appears highly sinusoidal due to the inherent low voltage distortion provided by multilevel PWM operation. This can be clearly appreciated with the current harmonic spectrum shown in Fig. 10(b).

B. Experimental Results

To verify the validity of the proposed hybrid modulation, a five-level inverter was designed to implement this scheme. Fig. 11 shows a functional block diagram of the single phase five-level inverter that was implemented with eight insulated gate bipolar transistor (IGBT) switches with internal anti-parallel diodes. The base PWM pulses (fundamental frequency PWM and CBSVM) are generated using a low cost high speed Texas Instruments TMS320F2407 digital signal processor (DSP)

board with an accuracy of 20μs. A sequential signal was also generated to operate each IGBT with fundamental frequency PWM and CBSVM sequentially to equalize power losses and heating among the devices.

A hybrid PWM control algorithm based on combinational logic is developed and it is implemented in a Xilinx CPLD XC95108 IC. The CPLD controller combines fundamental frequency PWM, sequential signal and CBSVM to generate hybrid CBSVM pulses. The XC95108 IC is used to develop a control algorithm that is suited to this application and has the features of better response for high frequency input signals, narrow pulse width pulses and no jitter of the delay in the circuit. Optically coupled isolators MCT2E are used to provide electrical isolation between the Xilinx CPLD controller board and the power circuit. Four high voltage high speed IGBT drivers (IR2112) are used to provide proper and conditioned gate signals to the power switches. A digital real time oscilloscope (Tektronix TPS2024) is used to display and capture the output waveforms and with the use of the fast Fourier transform (FFT), the spectrum of the output voltage and current are obtained as discussed hereafter.

Fig. 12(a) shows the line to neutral voltage waveform of the proposed five-level CBSVM operation in a standard modulation and the associated spectrum is presented in Fig. 12(b). It is confirmed that the harmonic cancellation up to the sidebands around the carrier frequency is achieved in the voltage waveform and the first significant harmonic is the 17th as predicted with a carrier frequency of 1050 Hz. Second, the inverter is operated with a RL load (R=30Ω, L=24mH) in the linear modulation range (modulation index M=0.8) and the corresponding waveform is shown in Fig. 13. The lower order harmonics and ripples in the current waveform are absent and it appears sinusoidal.

V. Conclusions

An energy efficient hybrid carrier based space vector modulation has been proposed for cascaded multilevel inverters. A hybrid PWM control algorithm is developed to derive the features of the fundamental frequency PWM and the carrier based space vector modulation for inverter operation, with the same physical structure. Compared to conventional carrier based space vector modulation, the reduced numbers of switching (up to 33%) are obtained while achieving the same fundamental voltage tracking. The proposed modulation offers a 26% power loss savings with the same carrier frequency operation. The best case is produced at a unity power factor and a modulation index (M=1). In this case the power loss saving is about 28%. It is shown that the better harmonic performance of proposed PWM strategy compared to its CBSVM exists in the entire range of the modulation index. The proposed technique can be easily extended to higher levels through the generalization process. Selected simulation and experimental results are reported to confirm the validity of the proposed technique.
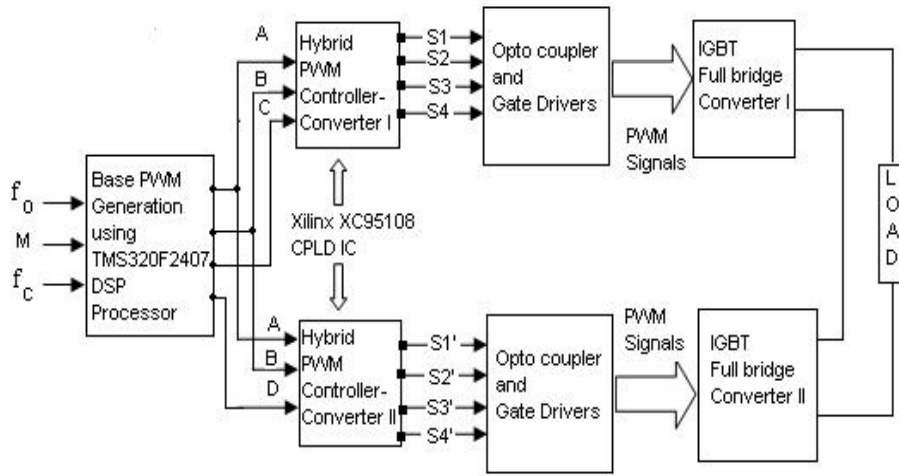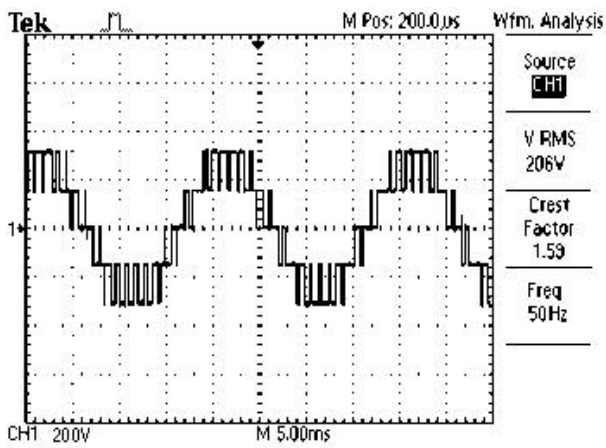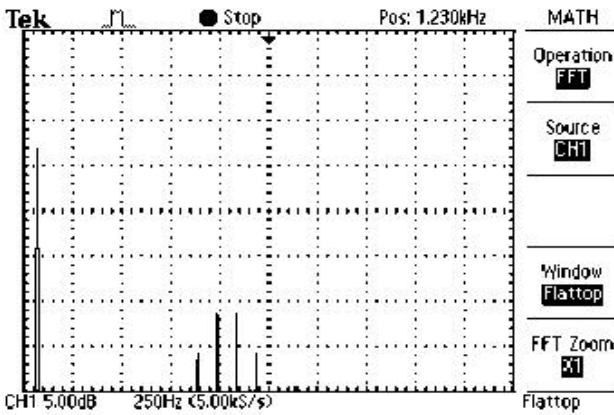
Fig. 11.   Functional block diagram of hybrid CBSVM implementation (one phase).
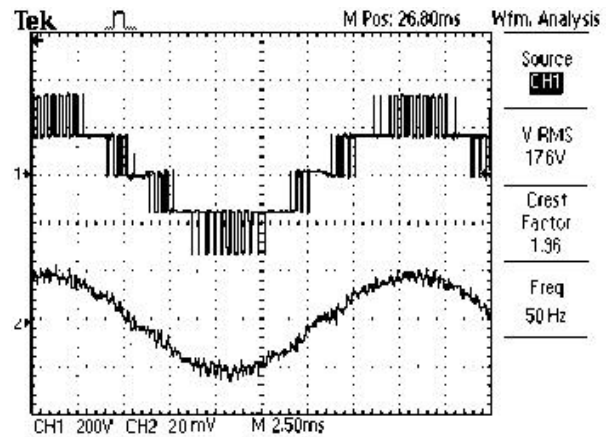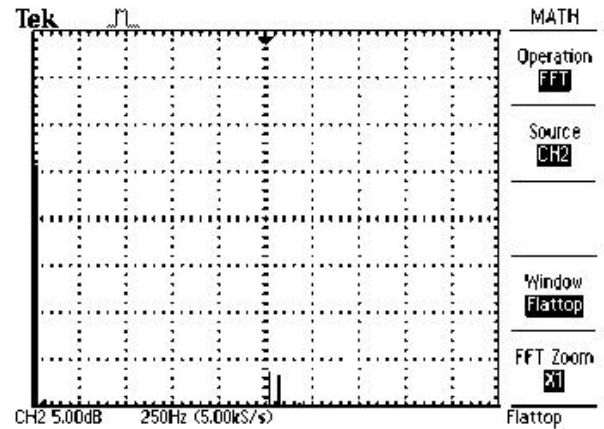

(a)

(b)

Fig. 12.   Experimental results of hybrid CBSVM operation in linear modulation (a) phase voltage waveform. (b) Spectrum of the phase voltage waveform.

(a)

(b)

Fig. 13.   Experimental results of the hybrid CBSVM in linear modulation range with RL load. (a) Output phase voltage and curent waveform. (b) Spectrum of the phase current waveform.

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