JPE 10-4-1

Power Loss Analysis of Interleaved Soft Switching Boost Converter for Single-Phase PV-PCS

Jae-Hyung Kim*, Yong-Chae Jung**, Su-Won Lee***, Tae-Won Lee‡, and Chung-Yuen Won†

†* School of Information and Communication Eng., Sungkyunkwan University, Suwon, Korea
** Department of Electronic Eng., Namseoul University, Cheonan, Korea
*** EN technologies Inc., Gunpo, Korea
‡ SAMSUNG ELECTRO-MECHANICS Co. Ltd., Suwon, Korea

Abstract

In this paper, an interleaved soft switching boost converter for a Photovoltaic Power Conditioning System (PV-PCS) with high efficiency is proposed. In order to raise the efficiency of the proposed converter, a 2-phase interleaved boost converter integrated with soft switching cells is used. All of the switching devices in the proposed converter achieve zero current switching (ZCS) or zero voltage switching (ZVS). Thus, the proposed circuit has a high efficiency characteristic due to low switching losses. To analyze the power losses of the proposed converter, two experimental sets have been built. One consists of normal devices (MOSFETs, Fast Recovery (FR) diodes) and the other consists of advanced power devices (CoolMOSs, SiC-Schottky Barrier Diodes (SBDs)). To verify the validity of the proposed topology, theoretical analysis and experimental results are presented.

Key Words: Interleaved converter, Loss analysis, Photovoltaic system, Power conditioning system, Soft switching

I. INTRODUCTION

In recent years, one of the trends in power electronics converters has been to reduce power losses for high efficiency. There are two key methods to decrease the power losses of power electronic converters. The one is to apply advanced power devices into the converters. The other way is a development in their topologies, such as soft switching converters. Also, for high efficiency converters design, it is important to make the improvements through an analysis of loss factors and loss distribution[1],[2].

This paper proposes an interleaved soft switching (ISS) boost converter with a soft switching method for high efficiency PV-PCS. The interleaved boost converter (IBC) is advantageous in terms of its efficiency, since it can reduce conduction loss by means of a distribution of the input current.

In addition, an IBC has some merits, such as low current stress, reduction of the passive components dimension, and small input current ripple and output voltage ripple.

However, the switching loss of an IBC increases according to the increase in the number of switching devices such as MOSFETs and diodes. To solve this problem, this paper adopts the soft switching method. The proposed converter can reduce the switching loss because the switches are turned on and off with zero current switching (ZCS) and zero voltage switching (ZVS), respectively. As a result, the proposed ISS boost converter can achieve better energy transfer.

This paper presents the operational principle and a theoretical analysis of the proposed converter in section 2. In section 3, we calculate the power loss of the proposed ISS boost converter in detail. Then, to verify the validity of the proposed circuit, a 3kW prototype was built, and a test was performed to compare the efficiency before and after using advanced power devices in the proposed converter.

II. INTERLEAVED SOFT SWITCHING BOOST CONVERTER [3],[4]

Fig. 1 shows a schematic of the proposed ISS boost converter, which is based on a 2-phase interleaved boost converter with soft switching cells that consists of switches (S_2, S_4), resonant diodes (D_3, D_4, D_5, D_6), resonant inductors (L_{r1}, L_{r2}) and resonant capacitors (C_{r1}, C_{r2}).

The interleaving technique requires that each converter connected in parallel operates at the same switching frequency, and that the switch of each converter be shifted with respect to the others by 360°/N. Owing to these features, the input current ripple, output voltage ripple and dimension of the passive components can be reduced. However, due to the parallel structure, the switching losses of this topology increase according to the increase in the number of switching devices. We use soft switching cells to decrease the switching losses. Therefore, the proposed converter has the advantages of both

Manuscript received Feb. 24, 2010; revised Apr. 23, 2010
† Corresponding Author: won@yurim.skku.ac.kr
Tel:+82-31-290-7115, Fax:+82-31-299-4623, Sungkyunkwan Univ.
* School of Information and Communication Eng., Sungkyunkwan University, Korea
** Dept. of Electronic Eng., Namseoul University, Korea
*** EN technologies Inc., Korea
‡ SAMSUNG ELECTRO-MECHANICS Co. Ltd., Korea

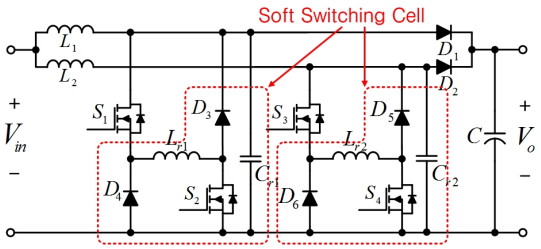


Fig. 1. The proposed ISS boost converter.

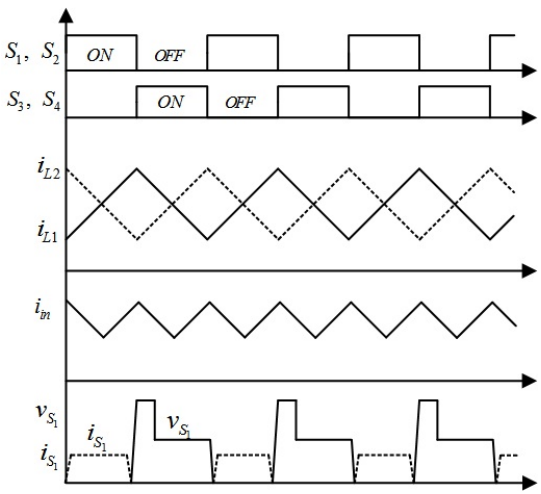


Fig. 2. Switching patterns and theoretical voltage and current waveforms.

the interleaving topology and soft switching cells. Fig. 2 illustrates the switching patterns along with the theoretical voltage and current waveforms. Two switches of each phase, such as (S_1, S_2) or (S_3, S_4), are turned on and off, simultaneously. Each phase has a phase difference of 180 degrees. Thus, the main inductor current of each phase linearly increases or decreases with a phase difference of 180 degrees according to the switching patterns. As seen in Fig. 2, the input current ripple is reduced and the input current ripple frequency becomes 2 times higher than the switching frequency. The operation modes of the proposed ISS boost converter are divided into 6 stages in a single phase.

Fig. 3 depicts the operation modes according to the different current paths.

Fig. 4 shows the key waveforms of the proposed converter during one switching period.

MODE 0 $[t_0 \leq t < t_1]$

Switches (S_1, S_2) are in the off state. The main inductor current (i_{Ll}) flows to the load through the main diode D_1 and decreases linearly.

MODE 1 $[t_1 \leq t < t_2]$

At time t_1, switches (S_1, S_2) are simultaneously turned on with ZCS, due to the resonant inductor L_{r1}. The resonant inductor current (i_{Lr1}) begins to increase linearly. This mode is finished when iLr1 has become equal to i_{L1}.

MODE 2 $[t_2 \leq t < t_3]$

Mode 2 is a resonant mode. The output diode (D_1) is turned off. L_{r1} and the resonant capacitor (C_{r1}) begin to resonate. The resonant capacitor voltage (v_{Cr1}) decreases resonantly from the output voltage V_0 to zero.

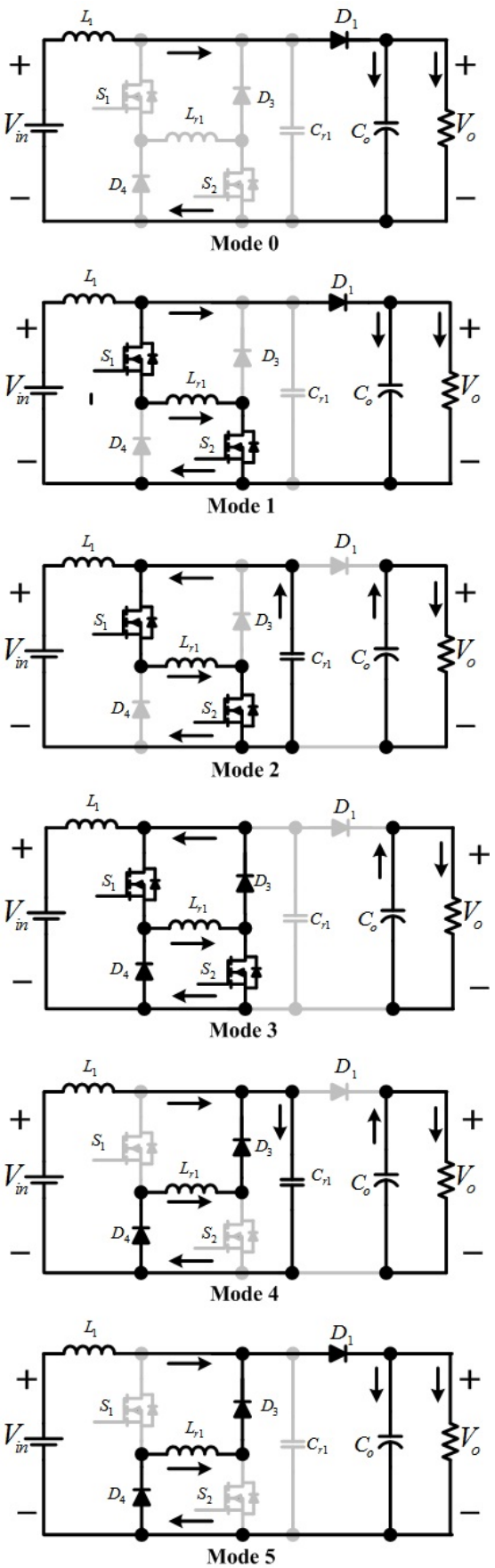


Fig. 3. Operation modes of the proposed converter.

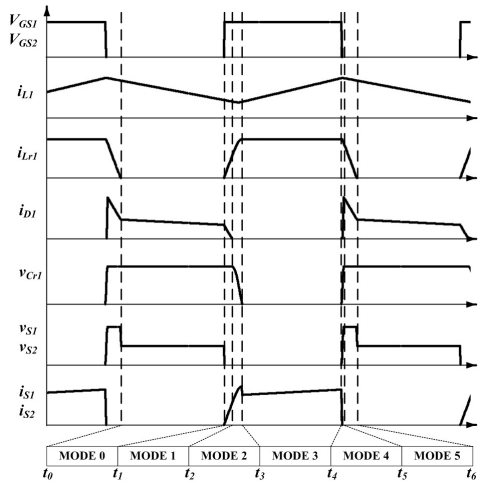


Fig. 4. Key waveforms of the proposed converter.

MODE 3 $[t_3 \leq t < t_4]$

At time t_3, the resonant diodes (D_3, D_4) are turned on. i_{Lr1} flows through the two freewheeling paths, $S_1 \rightarrow L_{r1} \rightarrow D_3$ and $S_2 \rightarrow D_4 \rightarrow L_{r1}$. The i_{L1} begins to increase linearly and the path of the i_{L1} is $L_1 \rightarrow S_1 \rightarrow L_{r1} \rightarrow S_2$. The v_{Cr1} maintains zero voltage.

MODE 4 $[t_4 \leq t < t_5]$

This mode is started when S_1 and S_2 are turned off with ZVS, due to C_{r1}. L_{r1} and C_{r1} begin to resonate. The i_{Lr1} decreases resonantly and v_{Cr1} begins to increase resonantly from zero to V_0.

MODE 5 $[t_5 \leq t < t_6]$

The i_{L1} and i_{Lr1} are added together and the resulting current flows to the output through D_1. i_{Lr1} decreases to zero during this mode, which is finished when i_{Lr1} has become equal to zero.

III. POWER LOSS ANALYSIS OF THE ISS BOOST CONVERTER [5]-[9]

The specifications used in the power loss analysis are given in Table I. The power loss analysis of the proposed converter is performed with two types of sets. Set A consists of normal devices (MOSFETs, fast recovery (FR) diodes) while set B consists of advanced power devices (CoolMOSs, SiC-Schottky barrier diodes (SBDs)).

TABLE I
SPECIFICATIONS OF PROPOSED CONVERTER

Parameter	Value	Unit
Rated Output Power (P_o)	3	[kW]
Input Voltage (V_{in})	DC 200∼350	[V]
DC-Link Voltage (V_{DC})	DC 380	[V]
Switching Frequency (f_{Csw})	30	[kHz]
Boost Inductor (L_1, L_2)	500	[μH]
Resonant Inductor (L_{r1}, L_{r2})	40	[μH]
Resonant Capacitor (C_{r1}, C_{r2})	20	[nF]

The calculation of the results for the power losses are based on the following conditions:

- Input voltage : DC 200[V]
- Output voltage : DC 380[V]
- Load rate : 100[%]

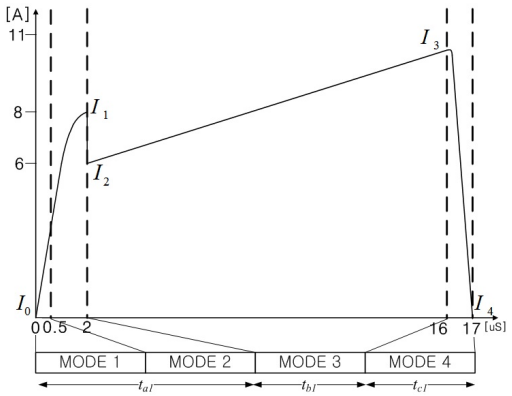


Fig. 5. FET drain current waveform.

A. POWER LOSS OF FET

Fig. 5 illustrates the FET current (I_{Drain}) waveform during each mode.

The $I_{2(Drain(rms))}$ is as follows:

$$I^2_{Drain(rms)} = \frac{I_0^2 + I_1^2 + I_0 I_1}{3} \cdot \frac{t_{a1}}{T} + \frac{I_2^2 + I_3^2 + I_2 I_3}{3} \cdot \frac{t_{b1}}{T} + \frac{I_3^2 + I_4^2 + I_3 I_4}{3} \cdot \frac{t_{c1}}{T} \quad (1)$$

where, the $I_{Drain(rms)}$ is the root-mean-square (rms) value of the I_{Drain}. A MOSFET (IXFN48N60P) and a CoolMOS (IPW60 R045CS) were used as the switching device of set A and set B, respectively. The characteristics of the CoolMOS are that the drain-source on the resistance ($R_{DS(on)}$) is about 1/5th and the output capacitance (C_{OSS}) is about 3/5th of a general MOSFET's. Therefore, the CoolMOS can reduce the conduction loss and the output capacitance loss.

The loss of FET (P_{FET}) consists of the switching loss ($P_{SW(FET)}$) and the conduction loss ($P_{COND(FET)}$).

$$P_{FET} = P_{SW(FET)} + P_{COND(FET)}. \quad (2)$$

The $P_{SW(FET)}$ is calculated on the basis of the overlap area of the drain-source voltage (V_{DS}) and drain current (I_{Drain}).

$$P_{SW(FET)} = (E_{ON} + E_{OFF}) \times f_{Csw}. \quad (3)$$

Not all the FETs of the proposed converter generate E_{ON} and E_{OFF} due to ZCS and ZVS, respectively. The drain-source on the resistance of FET ($R_{DS(on)}$) increases about 1.5 times at an operating temperature of 80°C. Therefore, the $P_{COND(FET)}$ is as follows:

$$P_{COND(FET)} = I^2_{Drain(rms)} \times (R_{DS(on)} \times 1.5@80[^\circ C]). \quad (4)$$

B. POWER LOSS OF THE DIODE

A FR-diode (DSE2x31-06C) and a SiC-SBD (IDT16S 60C) were used as the main and resonant diodes of set A and set B, respectively. The schottky barrier of the SiC-SBD is about 2 times higher than that of the FR-diode and the leakage current

TABLE II
POWER LOSS OF FET

FET Power Loss Parameter	Set A IXFN 48N60P (MOSFET)	Set B IPW60R045CS (CoolMOS)	Unit
$(E_{ON}) \times 4$	0	0	[W]
$(E_{OFF}) \times 4$	0	0	[W]
$(P_{COND(FET)}) \times 4$	39.492	12.795	[W]
$(P_{FET}) \times 4$	39.492	12.795	[W]

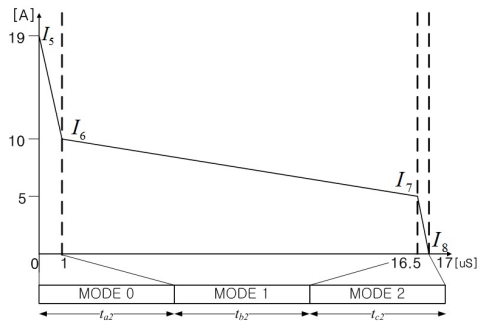


Fig. 6. Main diode current waveform.

of SiC-SBD is smaller than that of the FR-diode. The reverse recovery current is almost zero. Thus, although the f_{Csw} is increased, the switching loss is not increased. The power loss of the diode (P_{DIODE}) consists of the reverse recovery loss ($P_{trr(DIODE)}$) and the conduction loss ($P_{COND(DIODE)}$).

$$P_{DIODE} = P_{trr(DIODE)} + P_{COND(DIODE)}. \quad (5)$$

The $P_{COND(DIODE)}$ consists of the equivalent resistance loss (P_{RD}) and the forward voltage drop loss (P_{VF}).

$$P_{COND(DIODE)} = P_{RD} + P_{VF} \quad (6)$$
$$P_{RD} = R_D \times I_{rms}^2 \quad (7)$$
$$P_{VF(DIODE)} = V_F \times I_{avg} \quad (8)$$

where R_D is the equivalent resistance of the diode, V_F is the forward voltage drop, I_{rms} is the rms value of the diode current and I_{avg} is the average value of the diode current.

Fig. 6 shows the main diode current waveform during each mode. The $I^2_{M\_DIODE(rms)}$ and $I_{M\_DIODE(avg)}$ are as follows:

$$I^2_{M\_DIODE(rms)} = \frac{I_5^2 + I_6^2 + I_5 I_6}{3} \cdot \frac{t_{a2}}{T} + \frac{I_6^2 + I_7^2 + I_6 I_7}{3} \cdot \frac{t_{b2}}{T} + \frac{I_7^2 + I_8^2 + I_7 I_8}{3} \cdot \frac{t_{c2}}{T} \quad (9)$$

$$I_{M\_DIODE(avg)} = \frac{I_5 + I_6}{2} \cdot \frac{t_{a2}}{T} + \frac{I_6 + I_7}{2} \cdot \frac{t_{b2}}{T} + \frac{I_7 + I_8}{2} \cdot \frac{t_{c2}}{T} \quad (10)$$

where $I_{M\_DIODE(rms)}$ is the rms value of the main diode current and $I_{M\_DIODE(avg)}$ is the average value of the main diode current. Table III shows the power loss of the main diodes (P_{M_DIODE}) for each device. The R_D and V_F of the

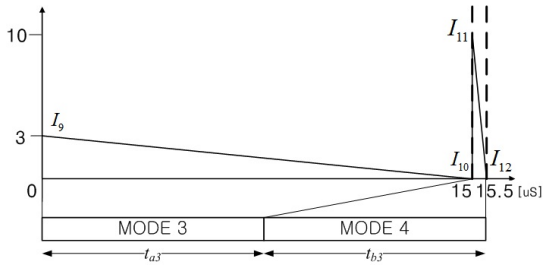


Fig. 7. Resonant diode current waveform.

SiC-SBD are larger than those of the FR-Diode. Therefore, the P_{M_DIODE} of set B is larger than that of set A.

TABLE III
POWER LOSS OF MAIN DIODE

Main Diode Power Loss Parameter	Set A DSEI 2x31-06C (FR-Diode)	Set B IDT16S60C (SiC-SBD)	Unit
$(P_{trr}) \times 2$	0	0	[W]
$(P_{RD}) \times 2$	0.803	3.290	[W]
$(P_{VF}) \times 2$	7.920	6.336	[W]
$(P_{M\_DIODE}) \times 2$	8.723	9.629	[W]

Fig. 7 shows the resonant diode current waveform during each mode.

The $I^2_{R\_DIODE(rms)}$ and $I_{R\_DIODE(avg)}$ are as follows:

$$I^2_{R\_DIODE(rms)} = \frac{I_9^2 + I_{10}^2 + I_9 I_{10}}{3} \cdot \frac{t_{a3}}{T} + \frac{I_{11}^2 + I_{11}^2 + I_{11} I_{12}}{3} \cdot \frac{t_{b3}}{T} \quad (11)$$

$$I_{R\_DIODE(avg)} = \frac{I_9 + I_{10}}{2} \cdot \frac{t_{a3}}{T} + \frac{I_{11} + I_{12}}{2} \cdot \frac{t_{b3}}{T}. \quad (12)$$

Table IV shows the power losses of the resonant diodes (P_{R_DIODE}).

TABLE IV
POWER LOSS OF RESONANT DIODE

Resonant Diode Power Loss Parameter	Set A DSEI 2x31-06C (FR-Diode)	Set B IDT16S60C (SiC-SBD)	Unit
$(P_{trr(DIODE)}) \times 4$	0	0	[W]
$(P_{RD}) \times 4$	88	361	[mW]
$(P_{VF}) \times 4$	3	2.4	[W]
$(P_{R\_DIODE}) \times 4$	3.088	2.760	[W]

From Table III and Table IV, the $P_{trr(DIODE)}$ is zero due to the soft switching cells and the SiC-SBD's $P_{COND(DIODE)}$ is larger than that of the FR-diode. Thus, the SiC-SBD does not necessarily need to use the proposed ISS boost converter for high efficiency.

C. POWER LOSS OF THE MAIN INDUCTOR

The power losses of the main inductors (P_{ML}) consist of the core losses (P_{Mfe}) and the copper losses (P_{Mcu}).

$$P_{ML} = P_{Mfe} + P_{Mcu}. \quad (13)$$

We used a high flux core [CH400060E20] for the main inductor. The main inductor ripple current is selected to be 60% of the main inductor average current.

Table V presents the specifications of the main inductor core.

TABLE V
SPECIFICATIONS OF MAIN INDUCTOR

Main Inductor Core Parameter	Value	Unit
Inductance (L_M)	250	[μH]
Cross section (A_{Me})	1.481	[cm2]
Volume (V_{Me})	14.6	[cm3]
Turn (N_M)	61	
Resistance (R_{ML})	0.02	[Ω]

$$\Delta B_{Mm}[G] = \frac{L_M[uH] \times \Delta I[A]}{N_M \times A_{Me}[cm^2]} \times 100 \quad (14)$$

$$B_{Mm}[kG] = \frac{\Delta B_{Mm} \times 0.001}{2} \quad (15)$$

where ΔB_{Mm} is the variation of the magnetic flux density and B_{Mm} is the ac magnitude of the magnetic flux density.

The core loss of the cross section (P_{MLcs}) and the P_{Mfe} of the main inductor core are as follows:

$$P_{ML_{cs}} = 0.32 \times B_m^{2.28} \times f_{Csw}^{1.72} = 72.69[mW/cc] \quad (16)$$

$$P_{Mfe} = P_{ML_{cs}} \times \frac{V_M e[cm^3]}{1000} = 1.061[W]. \quad (17)$$

The P_{Mcu} can be written as follows:

$$P_{Mcu} = I_{L(rms)}^2 \times (R_{ML} \times 1.3@80^\circ C). \quad (18)$$

Table VI presents the power loss of the main inductor. In order to reduce the core size, the main inductor of each phase is divided into two inductors connected in series.

TABLE VI
POWER LOSS OF MAIN INDUCTOR

Main Inductor Power Loss High Flux Core [CH400060E20]	Value	Unit
$(P_{Mfe}) \times 4$	4.25	[W]
$(P_{Mcu}) \times 4$	6.166	[W]
$(P_{ML}) \times 4$	10.412	[W]

D. POWER LOSS OF THE RESONANT INDUCTOR

We used a Molypermalloy Powder (MPP) core [CM270026] for the resonant inductor. The resonant inductor current appears as a square waveform during the switch turn on time. Table VII presents the specifications of the resonant inductor core.

Using (14) and (15), we can obtain the ΔB_m and B_m of the MPP core. The core loss of the cross section loss (P_{RLcs}) of the MPP core is as follows:

$$P_{RL_{cs}} = 0.22 \times B_m^{1.99} \times f_{Csw}^{1.68} = 103.02[mW/cc] \quad (19)$$

$$P_{Rfe} = P_{RL_{cs}} \times \frac{V_{Re}[cm^3]}{1000} = 0.433[W]. \quad (20)$$

TABLE VII
SPECIFICATIONS OF RESONANT INDUCTOR

Resonant Inductor MPP Core Parameter [CM270026]	Value	Unit
Inductance (L_R)	40	[μH]
Cross section (A_{Re})	0.654	[cm^2]
Volume (V_{Re})	4.2	[cm^3]
Turn (N_R)	37	
Resistance (R_{RL})	0.015	[Ω]

The equivalent resistance of the resonant inductor (R_{RL}) increases about 1.3 times at an operating temperature of 80. Therefore, the P_{Rcu} is expressed by (21).

$$P_{Rcu} = I_{L(rms)}^2 \times (R_{RL} \times 1.3@80^\circ C). \quad (21)$$

The power loss of the resonant inductor (P_{RL}) is represented in Table VIII .

TABLE VIII
POWER LOSS OF RESONANT INDUCTOR

Resonant Inductor Power Loss MPP Core [CM270026]	Value	Unit
$(P_{Rfe}) \times 2$	86.538	[mW]
$(P_{Rcu}) \times 2$	2.496	[W]
$(P_{RL}) \times 2$	2.859	[W]

E. TOTAL POWER LOSS OF THE ISS BOOST CONVERTER

Detailed values of the different power losses of set A and set B are given in Table IX.

TABLE IX
TOTAL POWER LOSS OF PROPOSED CONVERTER

Power Loss Parameter	Set A	Set B	Unit
P_{FET}	39.492	12.795	[W]
P_{M_DIODE}	8.723	9.629	[W]
P_{R_DIODE}	3.088	2.760	[W]
P_{ML}	10.412		[W]
P_{RL}	2.859		[W]
P_{CON}	64.575	38.457	[W]
Efficiency	97.848	98.718	[%]

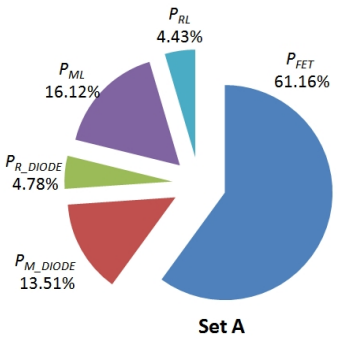
Compared to the MOSFET, the CoolMOS can reduce the power loss, 25.549 W, due to the low $R_{DS(on)}$ and C_{oss}. However, the SiC-SBD has an increased power loss, 0.578 W, in comparison to the FR-Diode. Thus, the SiC-SBD is not suitable for the soft switching topology, due to its high R_D.

Fig.8 shows the power loss distribution of set A and set B. The largest fraction of the power loss is the P_{FET}.

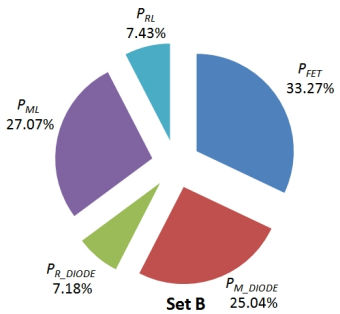
Therefore, switching devices should be considered in terms of the $R_{DS(on)}$ of FET in order to raise their efficiency. The diodes should be chosen for the smallest R_D and V_F. Also, the main inductor and resonant inductors should be selected for the smallest core loss. In addition, the winding wire should be considered in terms of the biggest available cross section.

IV. EXPERIMENTAL RESULTS

A 3kW prototype PV-PCS using an ISS boost converter was built to verify the theoretical analysis and then an efficiency



(a)



(b)

Fig. 8. Power loss distribution.

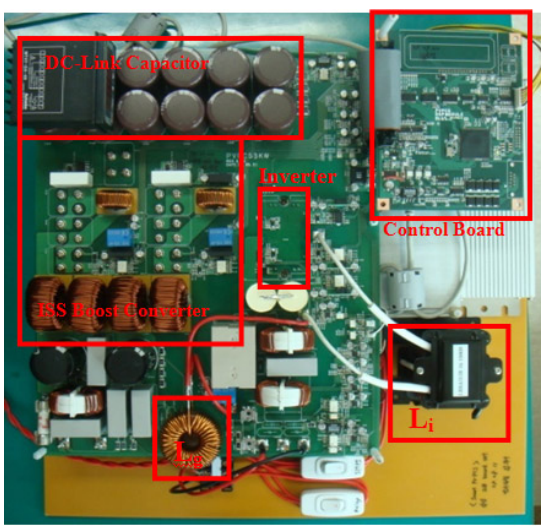


Fig. 9. Photograph of PV-PCS using proposed converter.

test was performed. The experimental parameters were applied under the same conditions as those of the power loss analysis. Fig. 9 shows a photograph of the PV-PCS using the proposed converter. A digital signal processor (DSP) TMS320F2812 of Texas Instruments (TI) was used to control the PV-PCS.

Fig. 10 shows the experimental results of the main inductor current waveforms and each phase gate signal when the input voltages are 250 V and 350 V, respectively. The devices used in Fig. 10 and Fig. 11 are for set A.

The output voltage is controlled to DC 380 V. The gate signals are supplied with a phase difference of 180 degrees. According to the gate signals, the main inductor currents increase and decrease linearly. Fig. 11 shows the experimental

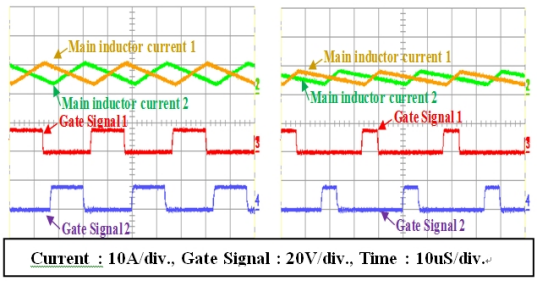


Fig. 10. Voltage, current of FET and gate signals waveforms.

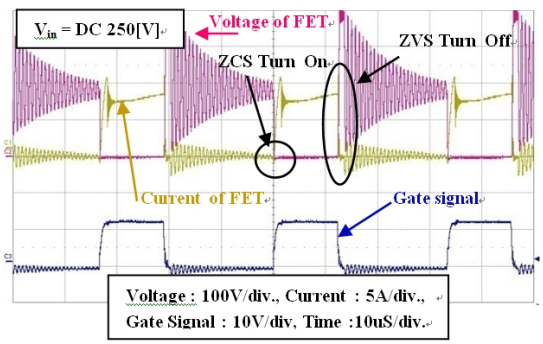


Fig. 11. Soft switching waveform and gate signal.

results of the switch's voltage and current as well as the gate signal. Because the voltage of the FET is affected by the capacitance (C_{OSS}), it includes a ringing waveform. The switch is turned on and off under ZCS and ZVS, respectively. Therefore, we can ensure that no switching loss of the proposed ISS boost converter is generated, because of the soft switching cells.

For the efficiency measurements, the experimental conditions of the proposed converter are given in Table I.

The input voltage ranges from 200-350 V and the load ratio ranges from 10-100%. A power analyzer (WT3000, YOKOGAWA) was used to measure the efficiency.

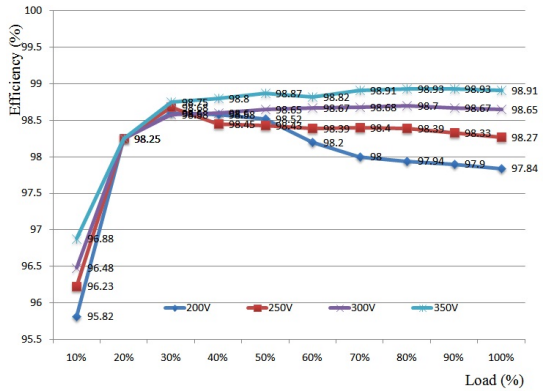
Fig. 12 shows the efficiency measurement results of set A and set B with respect to the variations in input voltage and load condition. The maximum efficiency of set A and set B is 98.93% at 350 V of input voltage. To compare the measured and calculated power loss, the same conditions as those mentioned in section III are applied.

Table X shows the difference between the measured and calculated power losses in the two sets. As can be seen in Fig. 12, the measured efficiencies of set A and set B are 97.84% and 98.2%, respectively.

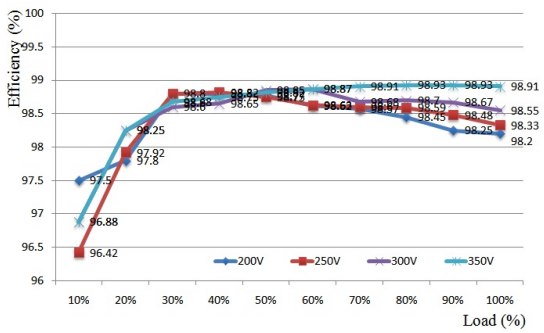
TABLE X
MEASURED AND CALCULATED POWER LOSSES OF THE CONVERTERS

Power loss	Set A	Set B	Unit
Measured value	64.8	54	[W]
Calculated value	64.575	38.457	[W]
Different power loss	0.225	15.543	[W]

The difference between the power losses is slight. This is considered to be due to unknown losses such as input EMI filter loss, PCB loss, connectors' loss, measurement equipment error and so forth.



(a) Set A.



(b) Set B.

Fig. 12. Efficiency of set A and set B.

V. Conclusions

In this paper, we proposed a high efficiency ISS boost converter for a PV-PCS. For this task, a 2-phase interleaved boost converter integrated with a soft switching cell was studied. The switches were turned on and off with ZCS and ZVS, respectively. This proposed topology can exploit both the IBC and the soft switching method. We analyzed the power losses of the proposed ISS boost converter in detail with respect to set A and set B, and then the efficiency tests were performed. We confirmed that a SiC-SBD is not suitable for the soft switching topology. The maximum efficiency of the proposed ISS boost converter is 98.93%. The experimental results verified the operational principle of the proposed converter and the theoretical power loss analysis. The result of the power loss analysis should be useful as a calculation guideline for soft switching converters.

References

[1] Masoud Jabbari and Hosein Farzanehfard, "A new soft switching step-down/up converter with inherent PFC performance," *Journal of Power Electronics*, Vol.9, No.6, pp.835-844, Nov. 2009.

[2] J.Ho. Kim, D.Y. Jung, S.H. Park, C.Y. Won, Y.C. Jung and S.W. Lee, "High efficiency soft-switching boost converter using a single switch," *Journal of Power Electronics*, Vol.9, No.6, pp.929-939, Nov. 2009.

[3] J.H. Lee, J.H. Kim, C.Y. Won, S.J. Jang and Y.C. Jung, "Soft switching multi-phase boost converter for photovoltaic system," *EPE-PEMC2008*, pp.1924-1928, Sep. 2008.

[4] Gang Yao, Alian Chen and Xianging, "Soft switching circuit for interleaved boost converters," *IEEE Transactions on Power Electronics*, Vol. 22, No. 1, pp.80-86, Jan. 2007.

[5] John Shen Z., Yali Xiong, Xu Cheng, Yue Fu and Kumar P., "Power MOSFET switching loss analysis: A new insight," *IEEE Industry Applications Conference Record*, Vol. 3, pp.1438-1442, Oct. 2006.

[6] Z. Liang, B. Lu, J. D. van Wyk and F. C. Lee, "Integrated coolMOS FET/SiC-Diode module for high performance power switching," *IEEE Trans. on Power Electronics*, Vol. 20, Issues 3, pp.679-686, May 2005.

[7] Infineon Technologies AG -White Paper_SiC.- http://www.infineon.com/

[8] Infineon Technologies AG -AN_CoolMOS_01_Rev1.2.- http://www.infineon.com/

[9] Infineon Technologies AG -ICE1PCS01/02.- http://www.infineon.com/

Jae-Hyung Kim was born in Pusan, South Korea in 1975. He received his B.S. and M.S. in Electrical Engineering from the University of Dong-Eui, Korea, in 1995 and 2002, respectively. Since 2008, he has been with the Department of Information and Communication Engineering, the University of Sungkyunkwan, South Korea, where he is currently working toward his Ph.D. His current research interests include the modeling and control of photovoltaic power conditioning systems.

Yong-Chae Jung was born in Korea in 1965. He received his B.S. from Hanyang University, Seoul, Korea, in 1989, and his M.S. and Ph.D. in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1991 and 1995, respectively. He is currently an Associate Professor in the Department of Electronic Engineering at Namseoul University. His research interests include the design and control of power converters, soft switching power converters, resonant power circuits, photovoltaic systems, power factor corrections, SMPS, induction heating circuits and EMI suppression. Dr. Jung is a member of the Korean Institute of Power Electronics (KIPE), and the Korean Institute of Electrical Engineering (KIEE).

Su-Won Lee received his B.S., M.S., and Ph.D. in Electrical Engineering from Chonbuk National University, Korea in 1991, 1993 and 1998, respectively. He was a Research Professor with BK21 Kunsan National University from 2001 to 2006. He was a Research Professor with the Institute of TMS Information Technology at Yonsei University from 2006 to 2008. He was a Research Professor with the Center for Advanced IT HRD with Close Industry Cooperation at Sungkyunkwan University from 2008 to 2010. Currently, he is working as a Senior Research Engineer with EN Technologies Inc. His current research interests include bi-directional dc/dc converters, inverter controls and renewable energy-based distributed generation systems.

Tae-Won Lee was born in Korea in 1971. He received his B.S., M.S. and Ph.D. in Electrical Engineering from Sungkyunkwan University, Suwon, Korea, in 1998, 2000, and 2007, respectively. He was a Postdoctoral Research Associate with Michigan State University in the U.S.A. from 2007 to 2008. Currently, he is a Senior Engineer of the Power Advanced Development Group Power Business Team at SAMSUNG ELECTRO-MECHANICS Co. Ltd.

Chung-Yuen Won was born in Korea in 1955. He received his B.S. in Electrical Engineering from Sungkyunkwan University, Suwon, Korea, in 1978, and his M.S. and Ph.D. in Electrical Engineering from Seoul National University, Seoul, Korea, in 1980 and 1988, respectively. From 1990 to 1991, he was with the Department of Electrical Engineering, University of Tennessee, Knoxville, as a Visiting Professor. Since 1988, he has been with the faculty of Sungkyunkwan University, where he is currently a Professor in the School of Information and Communication Engineering. He is also the President of the Samsung Energy Power Research Center. His current research interests include dc-dc converters for fuel cells, electro-magnetics modeling and prediction for motor drives, and control systems for rail power delivery applications. He is a president of the Korea Institute of Power Electronics (KIPE). Dr. Won is a senior member of the Institute of Electrical and Electronics Engineers (IEEE).