JPE 10-4-4

Carrier Based Single-State PWM Technique for Minimizing Vector Errors in Multilevel Inverters

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Abstract

In this paper, a novel analysis of a carrier based PWM method for multilevel inverters is presented. The space vector PWM and carrier based PWM correlations in multilevel inverters are investigated in a nominal two-level switching diagram. The obtained results can be applied to design various carrier PWM techniques. In this paper, a carrier based single-state PWM technique, which reduces the switching number and optimizes the active voltage errors, is presented. This PWM technique can be advantageous if there are a large number of levels. The proposed method is mathematically formulated and demonstrated by simulations and experimental results.

Key Words: Minimized voltage error, Multilevel inverter, PWM technique, Single-switching state

I. INTRODUCTION

Nowadays, multilevel inverters have become more attractive to researchers and industrial companies. There are two common types, which include NPC and cascaded as shown in Fig.1 and Fig.2 [1]-[5]. Recently, in an effort to reduce hardware construction cost, researchers have attempted to develop prospective hybrid topologies. There are basically three PWM schemes for their control. These include carrier based PWM, space vector PWM and selective harmonics elimination PWM methods [6]-[12]. In comparison to the space vector PWM methods, the carrier based PWM methods can be advantageously utilized in: 1) controlling common mode voltage, 2) controlling complicated inverter topologies such as 4-leg and 5-leg multilevel inverters, and 3) compensating unbalanced dc sources [13], [14]. The space vector modulation method presents a good tool for describing a balanced three phase system. However, its algorithm for implementation is rather difficult, particularly if common mode control is applied to improve PWM performance.

A comprehensive correlation between carrier based PWM and SVPWM has been derived in a recent work. This helps to realize a space vector method with carrier modulation [15]. As a result, a carrier PWM method is more advantageous because its algorithm can be applied to any multilevel inverter and a common mode control is available to improve the modulation performance.

The selected harmonic elimination PWM method (SHE) is a typical PWM method for reducing switching losses and harmonics distortion. In most cases, only the solutions from

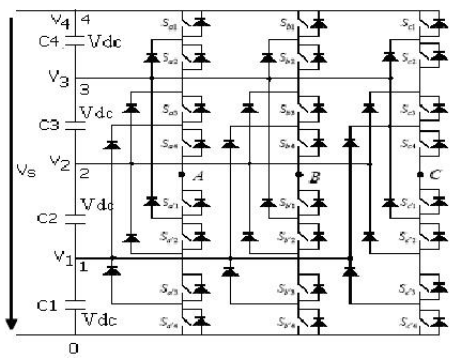

Fig. 1. The 3 phase 5-level NPC inverter.

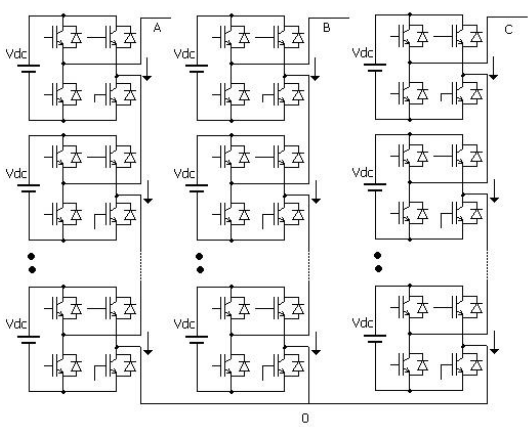

Fig. 2. The 3-phase cascaded multilevel inverter.

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the offline calculation are valid, particularly for each number of levels. If either the number of levels or the number of the eliminated harmonics is high, finding a solution may be impossible. There are other disadvantages such as the discontinuity of solutions for some output voltage ranges and the limitation on maximum output voltage. To have a similar characteristic, the step pulse modulation approximates the reference fundamental voltage and reduces most of the harmonic content [16]. However, there is still a complex calculation of the commutation angles and a limitation on the maximum output voltage.

A single-state PWM method presents a PWM technique, which produces only one voltage state at the output for a sampling period. In practice, direct torque control and hysteresis current loop control for AC motor drive systems are typical and well-known applications of the single state PWM technique.

As the first approach of a single-state PWM method with the smallest voltage error, a space vector modulation was introduced in recent work [18]. It requires a look-up table, whose data needs to be calculated for each inverter circuit. Another drawback is the limitation on the output voltage. Minimum common mode was set for the implementation but without any discussion on the influence of common mode changing.

In this paper, a carrier based approach to single-state PWM modulation for minimizing voltage errors will be proposed. The deduction is from a NPC inverter analysis, but its proper modification can also be applied to cascade topologies. The carrier based PWM scheme of a multilevel inverter can be centered in a nominal two-level switching state diagram. This makes the PWM study more advantageous and comfortable. The previously described problems can be avoided in the proposed carrier modulation, which is easily realized for any number of levels. As will be shown, the operating range can be extended up to the maximum voltage of the six step mode.

In addition to the fundamental voltage, the common mode voltage control presents a degree of freedom, which can be utilized for setting an optimized modulation, with respect to the THD factor and the switching loss balancing. Besides that, it can be favorably considered for some applications in a four wire unbalanced system. However, that will require further investigation.

II. TERMINOLOGY AND NOMINAL SWITCHING DIAGRAM FOR MULTILEVEL INVERTERS FOR BALANCED DC VOLTAGE SOURCES

Assumption: each dc voltage cell is constant and equal to the unit ($V_{dc} = 1$). Define the reference leg voltages between the outputs (A, B, C) and the dc-neutral point "0" (Fig.1), consisting of the active voltages $v_{x12},\ x = a, b, c$ and the reference common mode v_{0ref} [15] as:

$$v_{xref} = v_{x12} + v_{0ref}. \tag{1a}$$

Or in the vector form as:

$$\vec{v}_{ref} = \vec{v}_{12} + v_{0ref}\vec{I} \tag{1b}$$

where $\vec{v}_{ref} = [v_{aref}, v_{bref}, v_{cref}]^T,\ \vec{I} = [1, 1, 1]^T$ is a unit vector, and:

$$\vec{v}_{12} = [v_{a12}, v_{b12}, v_{c12}]^T. \tag{2}$$

The active voltages or the fundamental voltages can be described as follows:

$$\begin{aligned} v_{a12} &= v_{ref}\cos\theta \\ v_{b12} &= v_{ref}\cos(\theta - 2\pi/3); \\ v_{c12} &= v_{ref}\cos(\theta - 4\pi/3) \end{aligned} \tag{3}$$

where V_{ref} and θ are the amplitude and the phase argument of the reference voltage vector.

Define Max and Min as the maximum and minimum values from the three phase voltages as:

$$\begin{aligned} Max &= Max(v_{a12}, v_{b12}, v_{c12}) \\ Min &= Min(v_{a12}, v_{b12}, v_{c12}) \end{aligned} \tag{4}$$

The reference common mode voltage can be proposed in the range of v_{0Max} and v_{0Min} as:

$$\begin{aligned} v_{0Max} &= (n-1) - Max \\ v_{0Min} &= -Min \end{aligned} \tag{5}$$

The active Low$L_{(x)}$ and High $H_{(x)}$ levels correspond to the two dc voltages nearest to the reference leg voltage v_{xref} as shown in Fig.3(a). This can be described as:

$$L(x) = \begin{cases} n_{(x)} & if \quad 0 \le v_{ref} < (n-1) \\ n_{(x)} - 1 & if \quad v_{ref} = (n-1) \end{cases} \tag{6}$$

$$H_{(x)} = L_{(x)} + 1$$

$$\text{where } n_{(x)} = Int(v_{xref}); x = a, b, c. \tag{7}$$

The components of the vector $\vec{L} = [L_a, L_b, L_c]^T$ present three lower levels of the leg voltages in the considered switching state sequence.

Nominal switching time diagram: Investigation of the commutation process in a triangle period can be followed in Fig.3(b). The commutation instants are determined by comparing the active carrier waves with the modulating signals $\xi_x, x = a, b, c$, defined as:

$$\xi_x = v_{xref} - L(x); 0 \le \xi_x \le 1; \tag{8}$$

or

$$\vec{\xi} = \vec{v}_{ref} - \vec{L}$$

where $\vec{L} = [L_a, L_b, L_c]^T$.

Nominal switching state sequence: As seen in Fig.3(b) the switching time diagram for a multilevel inverter is similar to that for a two-level inverter. Define the nominal switching states as:

$$\begin{aligned}\vec{s}_1 &= [0,0,0]^T \\ \vec{s}_2 &= [S_{2a}, S_{2b}, S_{2c}]^T \\ \vec{s}_3 &= [S_{3a}, S_{3b}, S_{3c}]^T \\ \vec{s}_4 &= [1,1,1]^T.\end{aligned} \tag{9}$$

The first and the last states $\vec{s}_1; \vec{s}_4$ remind the two zero redundant states in a two-level inverter. The two remaining states $\vec{s}_2; \vec{s}_3$ can be determined from the relative positions of the signals ξ_x and the two nearest corresponding dc levels.

Define the maximum, medium and minimum values of the signals ξ_a, ξ_b, ξ_c as:

$$\begin{aligned}\xi_{Max} &= Max(\xi_a, \xi_b, \xi_c) \\ \xi_{Mid} &= Mid(\xi_a, \xi_b, \xi_c) \\ \xi_{Min} &= Min(\xi_a, \xi_b, \xi_c).\end{aligned} \tag{10}$$

The components of the vectors $\vec{s}_2; \vec{s}_3$ can be derived as follows:

$$\begin{aligned}s_{2x} &= \begin{cases}1 & if \quad \xi_x \geq \xi_{Max} \\ 0 & else\end{cases} \\ s_{3x} &= \begin{cases}1 & if \quad \xi_x \geq \xi_{Mid} \\ 0 & else\end{cases}.\end{aligned} \tag{11}$$

The switching state sequences in a multi-carrier multilevel inverter $\vec{S}_1, \vec{S}_2, \vec{S}_3, \vec{S}_4$ can be easily deduced by:

$$\vec{S}_j = \vec{L} + \vec{s}_j. \tag{12}$$

Conventional space vector modulation is based on the implementing of the three nearest vectors for the corresponding switching time duties as (K_{14}, K_2, K_3), respectively and is described as:

$$\vec{v}_{ref} = K_1\vec{S}_1 + K_2\vec{S}_2 + K_3\vec{S}_3 + K_4\vec{S}_4. \tag{13}$$

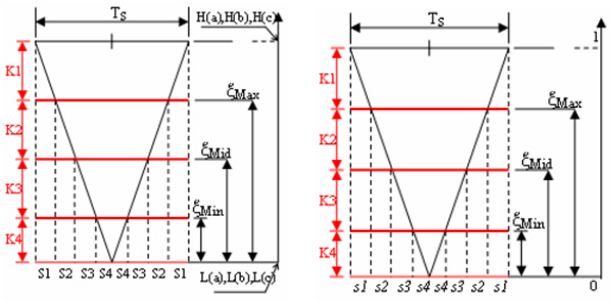
For example, the vector $\vec{S}_1 = [2,1,0]^T$ corresponds to the three phase leg voltages as $2V_{dc}, V_{dc}$ and 0. It can be deduced from Fig.3 by:

$$\begin{aligned}&K_1 = 1 - \xi_{Max}; K_2 = \xi_{Max} - \xi_{Mid}; \\ &K_3 = \xi_{Mid} - \xi_{Min}; K_4 = \xi_{Min} \\ &K_{14} = 1 - \xi_{Max} + \xi_{Min} \\ &K_1 + K_2 + K_3 + K_4 = 1.\end{aligned} \tag{14}$$

III. PROPOSED SINGLE STATE PWM METHOD

The principle behind the single-state PWM method: The proposed modulation can be described as a further step of the conventional SVPWM defined by (13). As shown in Fig.5, the PWM generator will set only one switching state for an entire sampling period:

$$\vec{v}'_{ref} = \vec{S}_j; j \in 1,2,3,4. \tag{15}$$



(a) (b)

Fig. 3. (a) Switching time diagram deduced in (b) new defined coordinates and (b) nominal switching time diagram.

The selected vector can be any of the 4 relevant switching states $\vec{S}_1, \vec{S}_2, \vec{S}_3$ and $\vec{S}_4$. The remaining states from the switching sequence are rejected.

The proposed modulation for minimized voltage error is based on the implementation of the nearest vector. The condition for selecting the switching state is shown in Fig.4(a) and (b) and can be described as:

$$\vec{v}'_{ref} = \vec{S}_j \ for \mid \vec{e} \mid = \mid \vec{v}_{ref} - \vec{S}_j \mid \rightarrow Min. \tag{16}$$

For example, the switching state $\vec{S}_3$ is implemented because the vector $\vec{V}_3$ is closest to the reference.

Determination of the nearest vector: two possible redundant states generate the same voltage vector, and they can be presented by one pivot vector, whose resulting switching time duty is equal to the sum of their switching time duties.

Each pivot vector $\vec{V}_j$ characterizes a certain contribution to the reference with its time duty $\vec{K}_j$. The influence is stronger if it is closer to the reference vector. It can be easily deduced that from the space vector modulation, the vector nearest to the reference vector will have the highest value of switching time duty. As a result, for implementing the proposed PWM method, it is necessary to set the reference vector of the maximum time duty, derived in the conventional PWM method, i.e.:

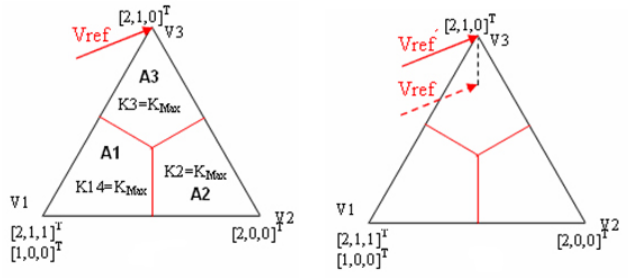
$$K_j = K_{Max} = Max(K_{14}, K_2, K_3). \tag{17}$$

For any reference vector, the influence of the individual pivot vectors on the function of K_{Max} defines three symmetrical sub-areas A_j, j=1,2,3 in the triangle, as shown in Fig.4(a). For example, if the reference vector $\vec{V}_{ref}$ is located in the sub-area A3, where the condition $K_3 = K_{Max}$ is valid, the active error will be minimized if the output voltage is produced by the vector $\vec{v}'_{ref} = \vec{S}_3$ (Fig.4(b)). Particularly, if it happens that $K_{Max} = K_{14}$ while both of the vectors $\vec{S}_1$ and $\vec{S}_4$ have the same error $\mid \vec{e}_{12} \mid$.

The criterion for a minimized offset error e_0 can be taken into account for setting the reference $\vec{V}'_{ref}$. For example, the vector $\vec{S}_1$ is selected if:

$$\mid Offset(\vec{S}_1 - \vec{V}_{ref}) \mid < \mid Offset(\vec{S}_4 - \vec{v}_{ref}) \mid \tag{18}$$

or, if after derivation, the condition is:



(a) (b)

Fig. 4. The single-state PWM method with a minimized voltage error (a) the function K_{max} in a triangle area, and (b) explanation of the principle.

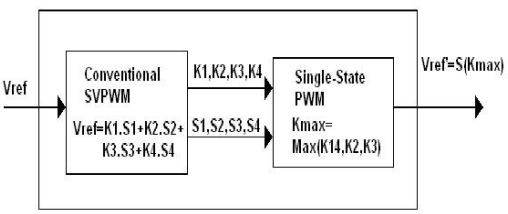


Fig. 5. The principle of the single-state PWM generator.

$$K_2 + 2K_3 + 3K_4 < 1.5\ . \tag{19}$$

The algorithm for the minimum voltage error based single-state PWM can be deduced in relation to the switching time duties as described in Table 1. If the reference vector appears at the center of the triangle, i.e. $K_{14} = K_2 = K_3 = 1/3$, the active error can achieve a maximum value of:

$$e_{12Max} = 2/(3\sqrt{3}). \tag{20}$$

TABLE I
ALGORITHM OF THE SINGLE-STATE PWM METHOD

Conditions in the conventional PWMs	Selected vectors and the error e_{12}
$K_{14} > K_2; K_{14} > K_3$ $K_2 + 2K_3 + 3K_4 < 1.5$	$\vec{v}'_{ref} = \vec{S}_1$ $e_{12} = \frac{2}{3}\sqrt{K_2^2 + K_3^2 + K_2K_3}$
$K_2 > K_3; K_2 > K_{14}$	$\vec{v}'_{ref} = \vec{S}_2$ $e_{12} = \frac{2}{3}\sqrt{K_{14}^2 + K_3^2 + K_{14}K_3}$
$K_3 > K_2; K_3 > K_{14}$	$\vec{v}'_{ref} = \vec{S}_3$ $e_{12} = \frac{2}{3}\sqrt{K_{14}^2 + K_2^2 + K_{14}K_2}$
$K_14 > K_2; K_{14} > K_3$ $K_2 + 2K_3 + 3K_4 > 1.5$	$\vec{v}'_{ref} = \vec{S}_4$ $e_{12} = \frac{2}{3}\sqrt{K_2^2 + K_3^2 + K_2K_3}$

Over-modulation in the single-state PWM method

For the single-state PWM method, the control characteristic is non-linear. The low order harmonics appear for any modulation index. This differs from the conventional PWM methods, and the term of over-modulation in the proposed method losses its original meaning. However, over-modulation can be seen as an approach to extend the reference fundamental voltage

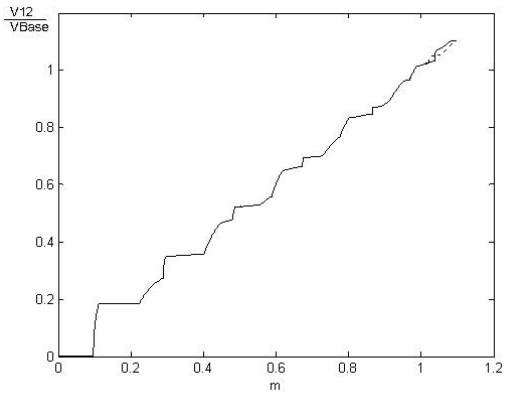


Fig. 6. The control characteristic of 7-level inverter.

$V_{(1)mref}$ in the range of $(V_s/\sqrt{3}, 2V_s/\pi)$, where Vs is the total voltage on the dc side. The active voltages in single-state over-modulation can be deduced from the control principle between the two-limit trajectories [15], for which the signals $v_{x12,m}$ related to the modulating index of m ($m_A \le m \le m_B$) can be deduced from the active signals of the corresponding limit modulation indexes of m_A, m_B as:

$$v_{x12,m} = (1-\eta)v_{x12,A} + \eta v_{x12,B} \tag{21}$$

$$where\ \eta = (m - m_A)/(m_B - m_A). \tag{22}$$

Compared to the limit deduced in [2], the proposed over-modulation method has a wider range and it can reach a maximum modulation index up to that of the six-step method. A simple two-mode over-modulation can be applied, using the three limit modulation indexes of 1, 1.055 and 1.1.

The control characteristic

A diagram of the nonlinear control characteristic of a seven-level inverter is calculated and drawn in Fig.6.

Single-state PWM demonstrates its benefit in reducing the switching losses for a higher number of levels and for higher modulation indexes. The existing error for the non-linearity of the control characteristic in an open-loop control may be reduced with an increase in the number of levels, or it may be compensated for in a close-loop control system.

Optimized switching loss single-state PWM method

The relationship between the number of switchings (N) per period of the output voltage and the THD factor was deduced for 4 PWM cases from Table 1. These are: 1) Conventional PWM with minimum common mode; 2) Conventional PWM with medium common mode; 3) Single-state PWM with minimum common mode and 4) Single-state PWM with medium common mode.

The number of switchings for the single-state PWM method depends on the modulation index, the common mode voltage and the number of levels. To compare the switching loss, the minimum and the medium common mode PWM methods have been investigated. A detailed study for a 7-level inverter is shown in Fig.7. The second method has a lower number of switchings for the narrow modulation index range of (0.68<m<0.72), while the first one is advantageous for a

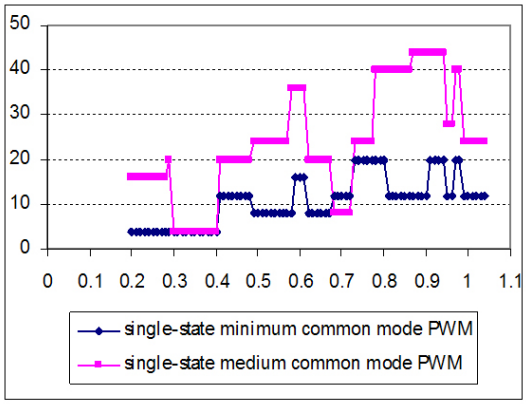


Fig. 7. Single-state PWM method in 7-level inverter - diagrams of number of switching for two different common mode functions.

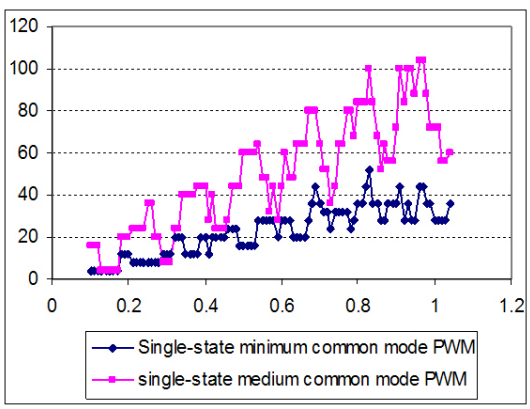


Fig. 8. Single-state PWM methods in a 15-level inverter - diagrams of the number of switching for two different common mode functions.

smaller number of switchings for nearly the entire modulation index range (m<0.68) and (0.72<m<1.1). A combination of both methods can set up an optimized PWM method. Furthermore, the minimum common mode method introduces a better distribution of switching loss among the switching devices. It is possible to have a conclusion for a 15-level inverter topology that is similar to the way shown in Fig.8.

Harmonic distortion factor

Comparing the THD factors of a conventional PWM method and the single-state PWM for an 11-level inverter, the first approach causes distortion given mainly by carrier sideband harmonics, while the second one mostly gives rise to the low-order harmonics. A detailed study of the characteristics of the 4 mentioned methods was realized and shown in Table 1. For an output frequency of 50Hz, a modulation index of m=1, and a carrier frequency f_{sw} of 1080Hz, the conventional PWM modulation for the minimum common mode gives 28 switchings. For comparison, the single-state PWM has the same number of switchings, but it gains a reduction in the THD factor (4.1% against 5.7%). In principle, there is no difference in the THD factors from both single-state PWM methods. For the entire modulation index, the THD factor diagrams of the 11-level inverter for the corresponding cases were drawn in Fig.9. The carrier frequencies of the first two methods were selected to be 600Hz.

TABLE II
COMPARISON OF THD FACTORS AND NUMBER OF SWITCHING FOR DIFFERENT PWM METHODS

m	0.4	0.5	0.6	0.7	0.8	0.9	1
f_{sw}	300	300	450(300)	600	720	600	900(1080)
N1	10	14	20	26	28	20	24(28)
THD1	15.2	9.3	8.7	9.4	7.0	5.9	5.4(5.7)
N2	10	18	24(14)	30	33	30	38(45)
THD2	13.3	12.0	9.2(8.4)	8.5	6.7	5.9	5.6(5.8)
N3	8	12	20	24	28	20	28
THD3	10.2	7.7	6.3	5.9	5.0	4.4	4.1
N4	20	40	24	60	32	64	52
THD4	10.2	7.7	6.3	5.9	5.0	4.4	4.1

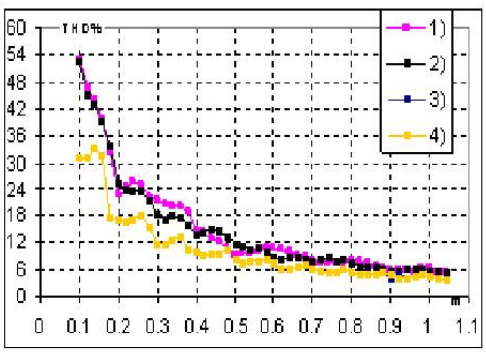


Fig. 9. The 11-level inverter - diagrams of THD factors for conventional PWM methods, f_{sw}=600Hz with 1) minimum common mode; 2) medium common mode. The THD diagrams for single-state PWM methods with 3) minimum common mode and 4) medium common mode.

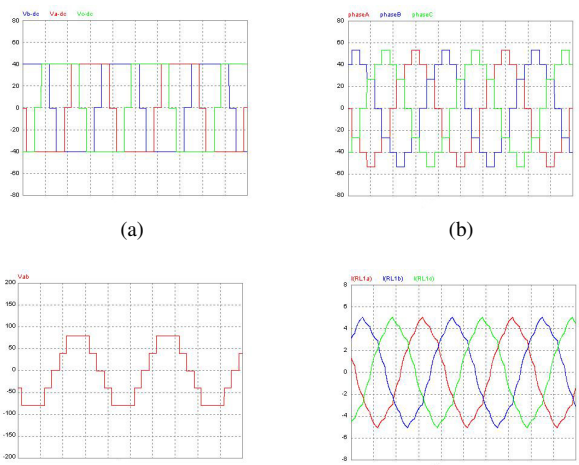
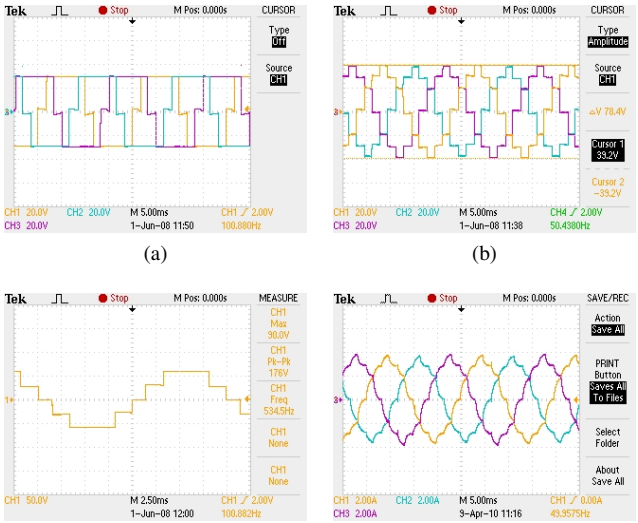


Fig. 10. Simulation results for m=0.4 - diagrams of (a) the inverter voltage, (b) the load voltage, (c) the line-line voltage and (d) the load currents.

The optimized single-state PWM algorithm was advantageously applied to a very high level inverter. In this case, the control linearity can be approximately extended to both the limits of a near zero modulation index and the maximum modulation index of the six-step mode. The THD factor is negligible. In a 31-level inverter, for m=0.2, the THD is 6.32% while for m>0.3, the THD is less than 4.35%.

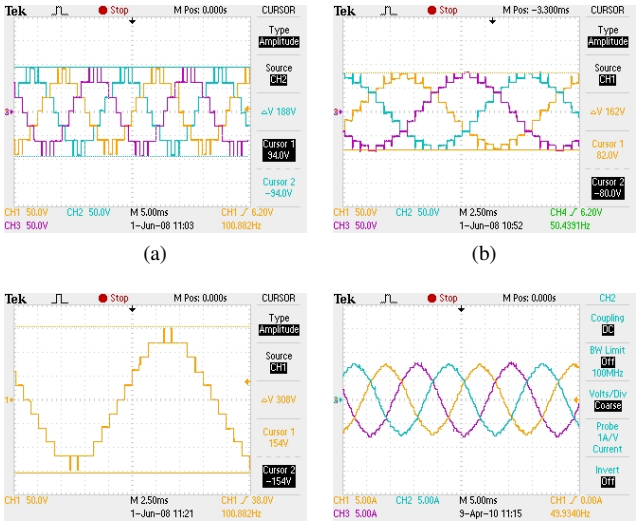
IV. SIMULATION AND EXPERIMENTAL RESULTS

To validate the theoretical analysis, simulations and experiments were implemented for a hybrid and cascaded seven-level inverter. Each phase consists of two-H bridge inverters



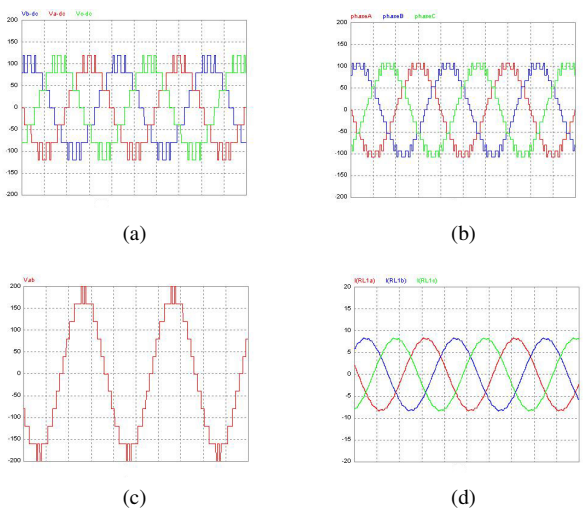
(a) (b) (c) (d)

Fig. 11. The experimental results for m=0.4 - diagrams of (a) the inverter voltage, (b) the load voltage, (c) the line-line voltage and (d) the load currents.



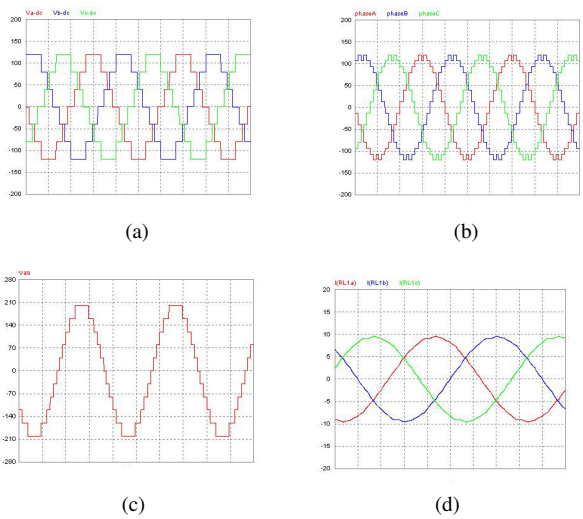
(a) (b) (c) (d)

Fig. 13. The experimental results for m=0.85 - diagrams of (a) the inverter voltage, (b) the load voltage, (c) the line-line voltage and (d) the load currents.



(a) (b) (c) (d)

Fig. 12. Simulation result for m=0.85 - diagrams of (a) the inverter voltage, (b) the load voltage, (c) the line-line voltage and (d) the load currents.

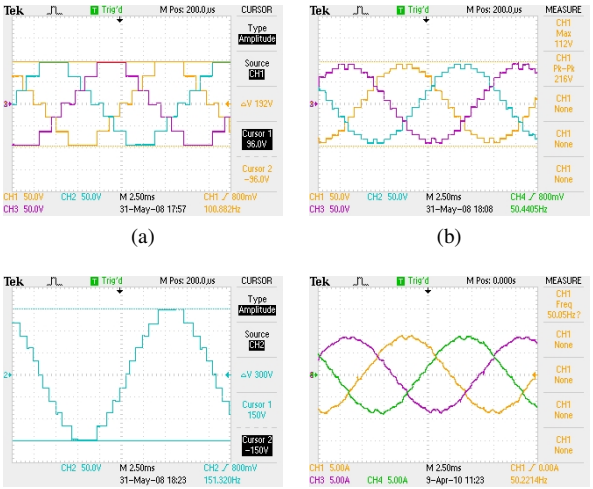


(a) (b) (c) (d)

Fig. 14. The simulation results for m=1 - diagrams of (a) the inverter voltage, (b) the load voltage, (c) the line-line voltage and (d) the load currents.

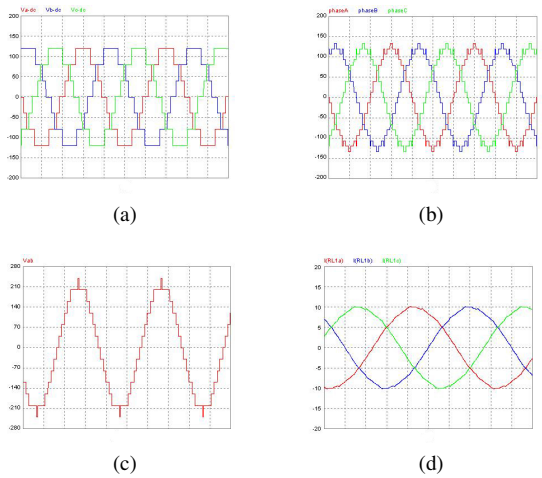
in series. The first H-bridge is supplied by a DC source of 40Vdc and the second is supplied by a source of 80Vdc. A three-phase RL load is set as $R = 10\Omega, L = 180mH$. The simulations were implemented using PSIM 6.0. The diagrams of the leg voltage, the phase voltage, the line-line voltage and the current were calculated and drawn in Fig.10, 12, 14 and 16. They correspond to several modulation indexes as 0.4, 0.85 and 1 in under-modulation and to 1.04 in over-modulation. The single-state PWM method is advantageously operated in a medium and high modulation index, where the harmonic amplitude distortion is normally small and the control characteristic is nearly linear. The hardware parameters are as follows: an IGBT FG60N100BNTD H20, an IGBT driver with a photo-couple PC123, a dead-time of $3\mu S$ set by hardware, a measuring oscilloscope TDS2014b, a control kit eZdsp TMS320F2812 and software CCStudio V3.1. The switching frequency was selected as 1050Hz. The diagrams of the leg voltage, the phase-load voltage, the line-line voltage and the phase current for modulation indexes of 0.4, 0.85, 1 and 1.04 were measured and shown in Fig.11, 13, 15 and 17. The current quality was evaluated through FFT analysis as shown in Fig.18 and 19.

The obtained experimental results, which are similar to the simulation results, prove the effectiveness of the proposed PWM algorithm. It is clearly seen that the output voltage/current is of a lower quality for a low modulation index. The harmonic distortion can be improved for the higher voltage range. The harmonic distortion of single-state PWM in the over-modulation range is similar to that of the conventional PWM methods. The situation is still good for the lower range (near m=1). At around six-step mode, the harmonic content is abruptly increased.



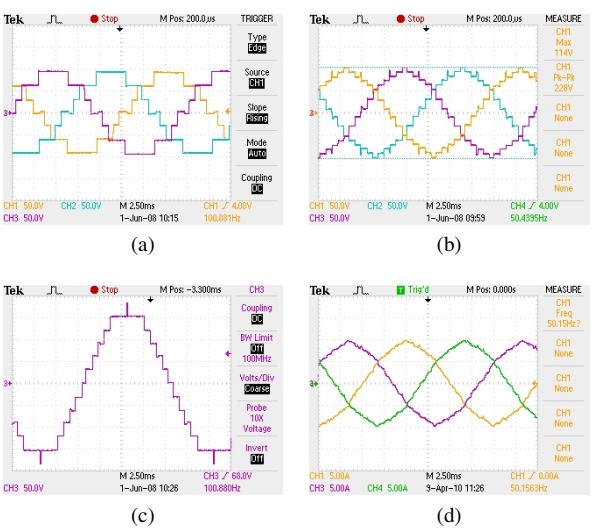
(a) (b) (c) (d)

Fig. 15. Experimental result for m=1 - diagrams of (a) the inverter voltage, (b) the load voltage, (c) the line-line voltage and (d) the load currents.



(a) (b) (c) (d)

Fig. 16. The simulation results for m=1.04 - diagrams of (a) the inverter voltage, (b) the load voltage, (c) the line-line voltage and (d) the load currents.

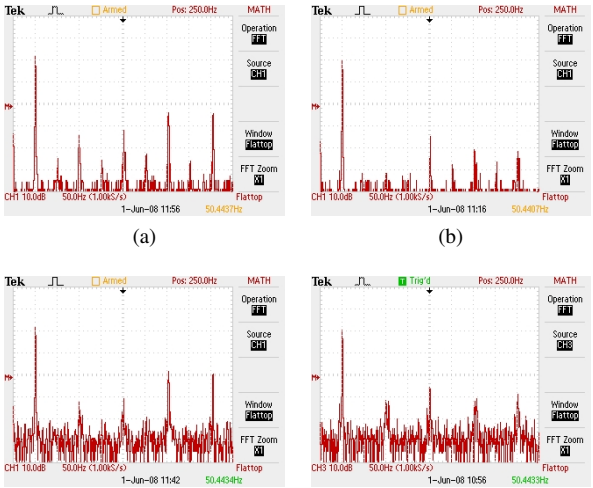


(a) (b) (c) (d)

Fig. 17. The experimental results for m=1.04 - diagrams of a) the inverter voltage, b) the load voltage, c) the line-line voltage and d) the load currents.

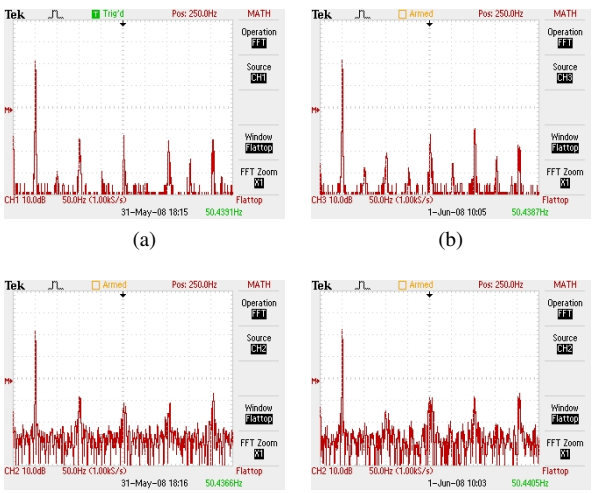
V. CONCLUSIONS

In this paper, a new single-state PWM method with minimum voltage error for multilevel inverters has been proposed.



(a) (b) (c) (d)

Fig. 18. Experimental results - diagrams of FFT analysis of the load current and the voltage for m=0.4 (diagrams (a) and (c)) and m=0.85 (diagrams (b) and (d)).



(a) (b) (c) (d)

Fig. 19. Experimental results - diagrams of FFT analysis of the load current and the voltage for m=1 (diagrams (a) and (c)) and m=1.04 (diagrams (b) and (d)).

Using the proper voltage model of an inverter circuit, it can transform the switching state diagram of multi-carrier modulation into that of a conventional two-level inverter. The parameters from the deduced nominal switching diagram can be used to propose a single-state PWM with minimum voltage error. The proposed method has been verified by simulation and experimental results. The benefit of the method can be more effective if a large number of levels is considered. The non-linear control characteristic becomes negligible with an increase in the number of levels. As a result, the carrier based single-state PWM method with the smallest common mode presents a preferable PWM solution for high power and high number-level inverters. For a small number of levels, the drawback of the single state PWM for small voltages can be solved with a combined PWM algorithm.

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