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A Novel Pulse-Width and Amplitude Modulation (PWAM) Control Strategy for Power Converters

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Abstract

Typical power electronic converters employ only pulse width modulation (PWM) to generate specific switching patterns. In this paper, a novel control strategy combining both pulse-width and amplitude modulation strategies (PWAM) has been proposed for power converters. The Pulse Amplitude Modulation (PAM), used in communication systems, has been applied to power electronic converters. This increases the degrees of freedom in eliminating or mitigating harmonics when compared to the conventional PWM strategies. The role of PAM in the novel PWAM strategy is based on the control of the converter's dc sources values. Software implementation of the conventional PWM and the PWAM control strategies has been applied to a five-level inverter for mitigating selective harmonics. Results show the superiority of the proposed strategy from the THD point of view along with a reduction in the inverter power dissipation.

Key Words: Multilevel inverters, PAM, PWAM, PWM, Selective harmonic mitigation, Total harmonic distortion

I. INTRODUCTION

Recently, there has been an increase in number of industrial applications that require medium voltage and megawatt power apparatus. Since using two level inverters causes problems under medium voltage and high power conditions, multilevel structures have been introduced. Having different advantages including low distortion output voltage, dv/dt stresses reduction, semiconductor switches stresses reduction and common mode voltage reduction, multilevel inverters have gained popularity in medium voltage and high power applications [1], [2]. On the other hand, in high power ratings and inverter power dissipation during the switching and conduction modes limits the switching frequency. Under this condition, the main object of the control strategy is to generate a switching pulse pattern in such a way that a desired output fundamental is produced while specific selective harmonic levels are eliminated or mitigated. This PWM strategy is called Selective Harmonic Elimination/Mitigation Pulse Width Modulation (SHE/M-PWM) [3]–[9] [12]–[16]. It requires finding a solution to a set of nonlinear transcendental equations.

However, setting the low order harmonics equal to zero in the SHE-PWM strategy may leave the first non-eliminated harmonics contents uncontrolled. This is a great disadvantage, which makes the results unsuitable for use in actual applications. In [12], a selective harmonic mitigation strategy is proposed. Instead of setting them equal to zero, each harmonic level is mitigated in this strategy and as a result the main disadvantages of the SHE-PWM can be eliminated [15], [16].

The order of the harmonics that can be mitigated in the SHM-PWM strategy is proportional to the number of pulses. In other words, mitigating more harmonics needs more pulses and consequently more power dissipation. This is due to the fact that only the pulse-width parameter is involved in this strategy.

In this paper, a novel Selective Harmonic Mitigation control strategy combining both pulse-width and pulse-amplitude modulations (SHM-PWAM) in multilevel inverters is introduced. The SHM-PWAM uses the multilevel inverter's dc sources values as degrees of freedom in addition to the switching angles. By solving a set of nonlinear transcendental equations, the optimized values of the dc sources along with the optimized switching angles are found for different output fundamentals. In this way, more low order harmonics are mitigated when compared to conventional SHM-PWM.

Section II introduces the novel SHM-PWAM control strategy and section III proposes its circuit realization. Simulation and results analysis are discussed in section IV.

II. THE SHM-PWAM CONTROL STRATEGY

The overall waveform of low frequency multilevel inverter output voltage is shown in Fig. 1.

The $\alpha_{i(i=1,2,\ldots,n)}$ is the ith switching angle and the $V_{i(i=1,2,\ldots,n)}$ is the ith voltage level amplitude. The Fourier series presentation of the shown waveform is:

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$$v(t) = \frac{1}{2}a_0 + \sum_{n=1}^{\infty}(a_n \cos\omega_n t + b_n \sin\omega_n t) \quad (1)$$

where ω_n is $n\frac{2\pi}{T}$ and the a_n and b_n coefficients are calculated as:

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(\omega t)\cos(n\omega t)d\omega t \quad (2)$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(\omega t)\sin(n\omega t)d\omega t. \quad (3)$$

Due to the half-wave symmetry of the waveform, all a_n and even-numbered b_n coefficients are zero. The nth harmonic can be mitigated if its related b_n coefficient is set equal to its minimum value. In addition, for a three-phase system, the triple-n harmonics in the phase voltage are canceled out in the line voltage. Therefore, the low order harmonics to be mitigated are odd, non-triple-n harmonics starting as 5, 7, 11, 13, 17…

The b_n odd coefficients are:

$$b_n = \frac{4}{n\pi}(V_1\cos(n\alpha_1) + (V_2 - V_1)\cos(n\alpha_2) + \ldots + (V_n - V_{n-1})\cos(n\alpha_n)). \quad (4)$$

In the conventional SHM-PWM strategy, the V_i values are kept constant and are mainly defined as $V_{i(i=1,2,\ldots,n)} = iV_{dc}$ where V_{dc} is the dc link voltage. Therefore, the b_n coefficients are:

$$b_n = \frac{4V_{dc}}{n\pi}(\cos(n\alpha_1) + \cos(n\alpha_2) + \ldots + \cos(n\alpha_n)). \quad (5)$$

From (5), the (n) equations are obtained in terms of the unknown $\alpha_1, \alpha_2, \ldots, \alpha_n$ angles. Each unknown angle is a degree of freedom in solving the proposed equations. Naturally, the first equation is for setting the output voltage fundamental to a desired value and the other (n-1) equations are for mitigating the low order harmonics to their minimum values. Solving these equations, the output voltage fundamental is controlled and the low order, odd, non-triple-n harmonics are mitigated to the order of (3n-1) for the even (n) and (3n-2) for the odd (n).

In the proposed SHM-PWAM control strategy, the inverter's dc sources values have been used as degrees of freedom along with the switching angles. In other words, keeping the V_i values constant is no longer a limitation bond in solving the equations obtained from (4). On the contrary, each $V_{i(i=1,2,\ldots,n)}$ value can vary between $(i-1)V_{dc}$ and iV_{dc} increasing the number of equations and the degrees of freedom from (n) to (2n). It means that by solving the resultant equations, (n) optimized V_i values can be found along with the optimized angles. In this way, more low order, odd, non-triple-n harmonics are mitigated when compared to the conventional SHM-PWM control strategy (6n-1 for the odd and even (n)) without any additional costs.

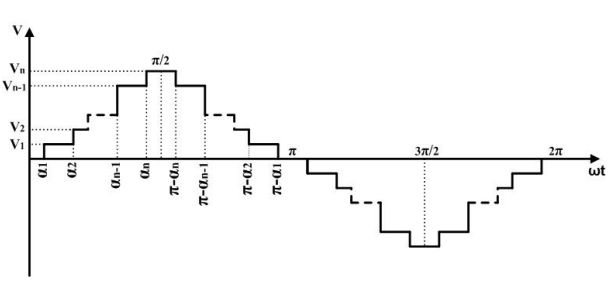


Fig. 1. Low frequency multilevel output voltage.

It is of worth noting that these extra degrees of freedom do not increase the switching frequency. This is due to the number of switching angles (or pulses) which is kept constant. In other words, the novel SHM-PWAM strategy does not impose any extra power dissipation on the inverter. However, it has been shown in section 4 that using the SHM-PWAM leads to less power dissipation when compared to SHM-PWM.

Although increasing the number of nonlinear transcendental equations from (n) to (2n) in the proposed SHM-PWAM, causes more complexity in solving them, the computational burden of the genetic algorithm (GA) used in this strategy, is independent of the number of equations.

The GA solves these equations in the form of an optimization problem with an objective function defined as:

$$F(\alpha_1, \alpha_2, \ldots, \alpha_n, V_1, V_2, \ldots, V_n) = (B_1 - A_1)^2 + B_5^2 + B_7^2 + \ldots + B_{(6n-1)}{}^2 \quad (6)$$

where $A_1 = m_a V_n \times \pi/4$ and m_a is the amplitude modulation index. (6) describes a measure of the selective harmonic mitigation effectiveness of the proposed strategy. Using optimization techniques, the answers from (6) containing the values of the inverter voltage levels and the switching angles, are found to be subjected to the following limitations:

$$\alpha_1 > \delta/2 \quad (7)$$

$$\pi/2 - \alpha_n > \delta/2 \quad (8)$$

$$\alpha_{i+1} - \alpha_i > \delta \quad \text{(i = 1, 2, ..., n-1)} \quad (9)$$

$$V_i \geq (i-1)V_{dc} \quad \text{(i = 1, 2, ..., n)} \quad (10)$$

$$V_i \leq iV_{dc} \quad \text{(i = 1, 2, ..., n).} \quad (11)$$

δ is the switch's minimum permissible pulse width and it is assumed to be 0.01 rad. The optimized answers are then saved in a look up table (LUT). Using a LUT for controlling a multilevel inverter is described in detail in section III.B.

III. CIRCUIT REALIZATION OF THE SHM-PWAM CONTROL STRATEGY

A. SHM -PWAM realization requirements

The SHM-PWAM circuit realization in multilevel inverters needs both PWM and PAM that are realized independently but at the same time. The PWM realization is the same as in the conventional SHM-PWM strategy. However, for the PAM realization, controllable dc sources are needed. In other words, the proposed sources' values should be capable of changing with a high dynamic at a specific time according to the SHM-PWAM basics.

On the other hand, in a variety of applications using low frequency control strategies, such as active power filters and electrical drives, power regeneration is inevitable. To satisfy these conditions the existence of controllable rectifiers, including thyristor rectifiers and PWM rectifiers, is necessary (Fig. 2).

However, the switching frequency in thyristor rectifiers is equal to the line frequency, which distorts the input current waveform. Also these rectifiers are not able to correct the input power factor to near unity values. Therefore, the most appropriate option for the realization of PAM is the use of a PWM rectifier configuration. Besides dc source control and power regeneration capabilities, PWM rectifiers also correct the input power factor and improve the input current waveform.

In this paper, the proposed SHM-PWAM control strategy is realized by a PWM-rectifier-inverter system as shown in Fig. 3. The multilevel inverter topology used in the proposed system is a five-level three-phase Cascaded H-Bridge (CHB) inverter that includes six H-bridge cells. The PWM rectifier realizing the PAM also includes six H-bridge cells. Each H-bridge cell contains four switches resulting in 48 switches for the overall system. Applying two other multilevel topologies, the Neutral Point Clamp (NPC) and the Flying Capacitor (FC), to the system in Fig. 3 requires the same number of switches. However, among the multilevel converters, the CHB topology is particularly attractive in high power applications since it requires the least number of components to synthesize the same number of voltage levels. Additionally, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than with the alternative multilevel converters [17].

The H-bridge cells on the rectifier side are connected to the input source through a three-phase three-winding transformer performing isolation.

In order to synthesize the five-level output voltage shown in Fig. 4(a), two h-bridge cells must be connected in series according to Fig. 4(b). The five-level inverter output voltage for one phase is shown as:

$$V_{an} = V_{a1} + V_{a2} \tag{12}$$

The dc sources in the system consist of six capacitors. These are controlled independently and at different values realizing the PAM. The three-phase source and load are balanced in the system shown in Fig. 3.

Again, it should be noted that the $V_{cu}(V_{cau} = V_{cbu} = V_{ccu} = V_{cu})$ and $V_{cl}(V_{cal} = V_{cbl} = V_{ccl} = V_{cl})$ voltages are constant in the conventional SHM-PWM strategy but that they get variable optimized values in the proposed SHM-PWAM strategy leading to more selective harmonics mitigation.

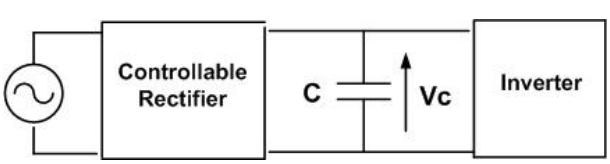


Fig. 2. Use of controllable rectifiers realizing PAM.

B. Realization procedures

The control block diagram of the PWM-rectifier-inverter system is shown in Fig. 5. The open loop volts/Hz control is used here for the induction motor which is a popular method of speed control because of its simplicity. The motor angular frequency $\omega_e{}^*$ is the primary control variable and m_a is directly generated from it. On the other hand, m_a is the LUT input parameter to choose the angles and the voltage level values. The selected angles along with the angle $\theta_e{}^*$ enter the PWM block where the times for the gate drive pulses are calculated and applied to the five-level inverter switches.

Referring to Fig. 5, the selected voltage level values are converted to the proper capacitor voltages references (V_{refu} and V_{refl}). These are then entered into the rectifier control section. The control of PWM-rectifiers is usually performed in the synchronous rotating frame converting the measured ac values into dc ones. This allows the use of conventional Proportional-Integral (PI) controllers achieving a zero steady state error.

The i_d reference value ($i_d{}^*$) can be calculated from the deviation of the capacitor voltages. By comparing the reference and actual values of the sum of the capacitor voltages, an error signal is generated. Passing this generated signal through a PI controller, the required $i_d{}^*$ value is obtained. The i_q reference value ($i_q{}^*$) is set equal to zero to achieve the unity input power factor. The construction procedure of the $V_d{}^*$ and $V_q{}^*$ reference voltages considering cross coupling effects is shown in Fig. 5. A Phase Locked Loop (PLL) has been employed for synchronization and it generates the angle information for the transformation.

The reference voltages ($V_{abc}{}^*$) will just ensure the balancing of the sum of the capacitor voltages. In order to assure that each separate capacitor voltage tracks its own reference, the amplitude of the $V_{abc}{}^*$ must have decomposed to generate separate reference voltage amplitudes for each cell. In this paper, a new control block named the Reference Decomposing Module (RDM) is added to the overall control block for generating the decomposed voltages ($V_{abcu}{}^*$ and $V_{abcl}{}^*$).

In the RDM, each separate capacitor voltage is compared to

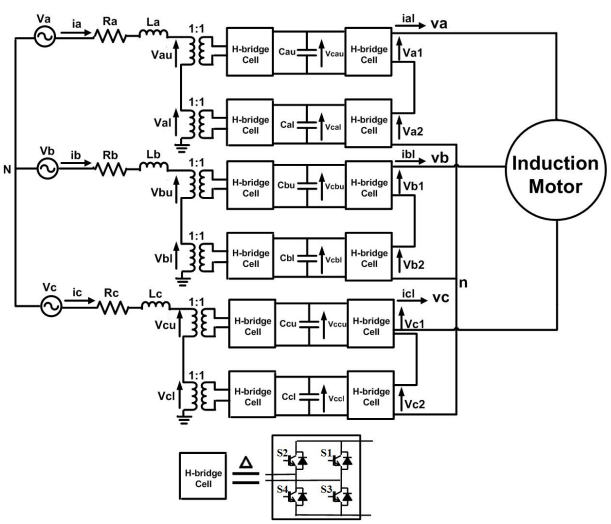


Fig. 3. Five-level three-phase PWM-rectifier-inverter system.

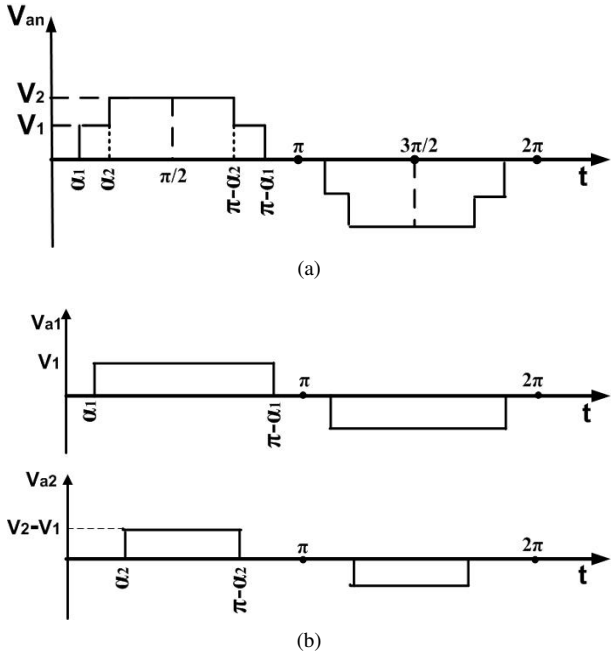


Fig. 4. The five-level output voltage and its separated waveforms.

its reference, producing a separate error signal. This error is then passed through a PI controller to generate an amplitude decomposing factor.

This means that for the six existing capacitors, there are six different amplitude decomposing factors (m_{au}, m_{bu}, m_{cu}, m_{al}, m_{bl}, m_{cl}). These values then decompose the reference voltages via the following equations:

$$V_{au}^* = m_{au} \times V_a^* \tag{13}$$
$$V_{bu}^* = m_{bu} \times V_b^* \tag{14}$$
$$V_{cu}^* = m_{cu} \times V_c^* \tag{15}$$
$$V_{al}^* = m_{al} \times V_a^* \tag{16}$$
$$V_{bl}^* = m_{bl} \times V_b^* \tag{17}$$
$$V_{cl}^* = m_{cl} \times V_c^* \tag{18}$$

where ${V_{abcu}}^*$ and ${V_{abcl}}^*$ are the three phase decomposed reference voltages for the upper and lower cells respectively. The corrected reference voltages from equations (13-18) enter a PWM block that uses the Phase Shifted PWM (PS-PWM) strategy in controlling the rectifier switches. This will ensure the balancing of the separate capacitor voltages with their own reference values. The new RDM control block is detailed in Fig. 6.

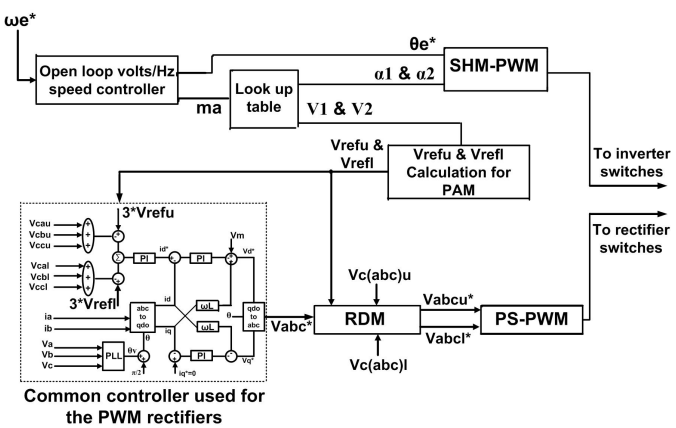


Fig. 5. The control block diagram of Fig. 3.

IV. SIMULATION RESULTS

In this section, a three-phase five-level CHB PWM-rectifier-inverter system (Fig. 2) is simulated, realizing both the novel SHM-PWAM (the novel mode) and the conventional SHM-PWM (the conventional mode) control strategies. It is of worth noting that due to the apparent advantages of the PWM-rectifier configuration mentioned in section 3-1, the conventional SHM-PWM is also realized with the system illustrated in Fig. 2. The two strategies are compared from the Total Harmonic Distortion (THD) point of view and in terms of power dissipation.

The objective functions of each mode are shown in table I. These objective functions are optimized subject to the limitations in (7-11).

To find the optimum values of V_1 and V_2 for the novel mode, the capacitors voltage references are calculated as:

$$V_{refu} = V_1 \tag{19}$$
$$V_{refl} = V_2 - V_1. \tag{20}$$

These values are constant in the conventional mode and their values are equal to the maximum dc link voltage in this paper. The three-phase load is a 2.3kv, 500hp, 50Hz induction motor. Its parameters, along with the simulated system parameters, are listed in Table II.

TABLE I
OBJECTIVE FUNCTIONS OF A FIVE-LEVEL WAVWFORM IN BOTH MODES

Control strategy	Objective function
SHM-PWM	$F(\alpha_1, \alpha_2) = (B_1 - A_1)^2 + B_5^2$
SHM-PWAM	$F(\alpha_1, \alpha_2, V_1, V_2) = (B_1 - A_0)^2 + B_5^2 + B_7^2 + B_{11}^2$

Fig. 7 shows the V_{refu} and V_{refl} voltage values versus m_a in both modes. Each m_a is a measure of the inverter output voltage fundamental.

The inverter output line voltage THD at no load in both modes are compared in Fig. 8. As can be seen from Fig. 8, extra degrees of freedom in the SHM-PWAM strategy, leads to a noticeable THD improvement without increasing the switching frequency or its related power dissipation.

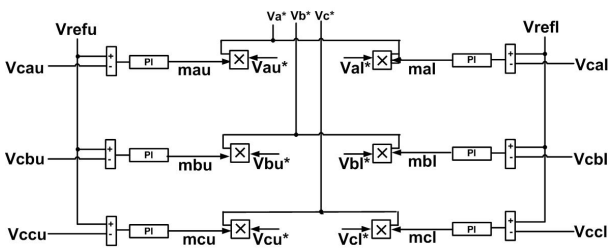


Fig. 6. The new RDM block to decompose the reference voltages.

TABLE II
THE SIMULATED SYSTEM PARAMETERES

Induction motor	
Stator, rotor winding resistance:	0.262Ω, 0.187Ω
Stator, rotor, mutual inductances:	0.1462H, 0.1462H, 0.143H
Number of pole pairs, moment of inertia:	2,11.06$kg.m^2$
Line voltage, current:	2300(rms), 93.6A
Nominal torque, nominal speed:	1650N.M, 1477.5rpm
Switching device	
3.3kv IGBT:	CM800HC-66H
Turn-on, turn-off time:	1μs, 1μs
Collector-emitter saturation voltage:	3.6v
Diode forward voltage, reverse recovery current, reverse recovery time:	2.7v, 500A, 1.4μs
Rectifier	
Switching frequency:	500Hz
DC link capacitors:	10mF
Maximum dc link voltage:	939v
Transformer turns ratio:	1:1
Source inductance, resistance:	1mH, 0.9Ω
Voltage source amplitude:	1000v

Assuming $\omega_e{}^*$ and the load torque values equal 100πrad/sec and 990 N.M respectively, the rotor speed and the electromagnetic torque are shown in Fig. 9. As can be seen from Fig. 9, the proposed speed and torque have reached their steady state values after about 1.5 sec.

Fig. 10 shows the motor line voltage (V_{ab}) in both modes. A THD comparison of Fig. 10(a) and 10(b) shows a 60% improvement with the SHM-PWAM strategy since the 7^{th} and the 11^{th} harmonics are mitigated in the novel mode.

Fig. 11 shows the stator current in both modes. In order to compare the most important harmonic contents of the proposed currents, Fig. 12 shows their 5^{th}, 7^{th} and 11^{th} harmonic magnitudes as percentages of the fundamental current. As can

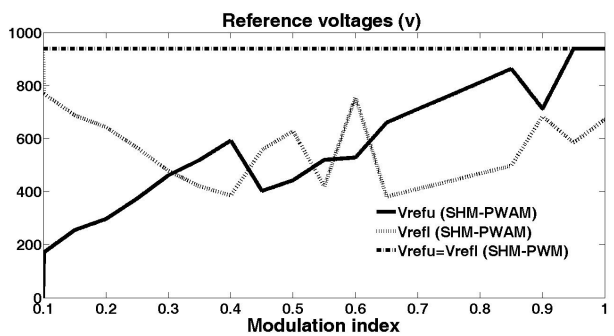


Fig. 7. The proposed and conventional reference voltage values.

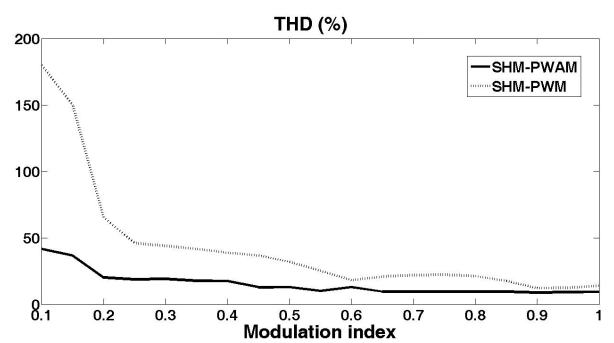


Fig. 8. The inverter output line voltage THD comparison at no load.

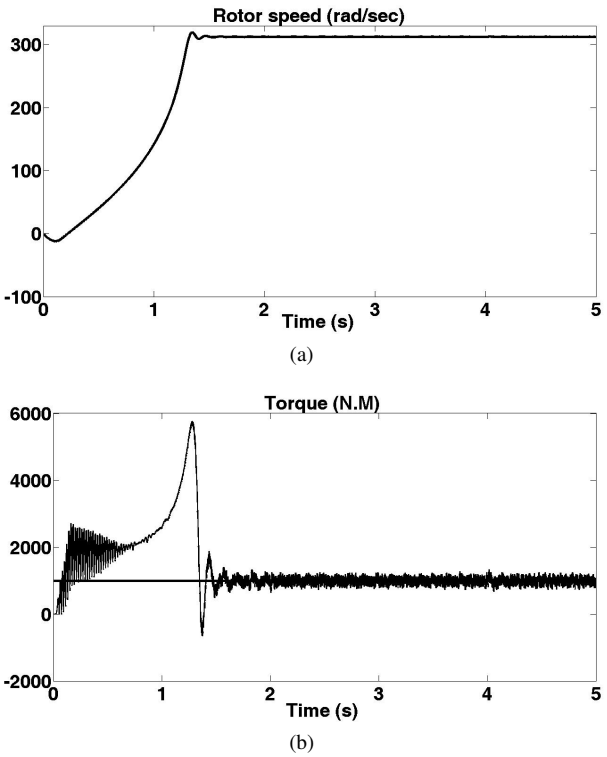


Fig. 9. (a) Rotor speed (b) Electromagnetic torque.

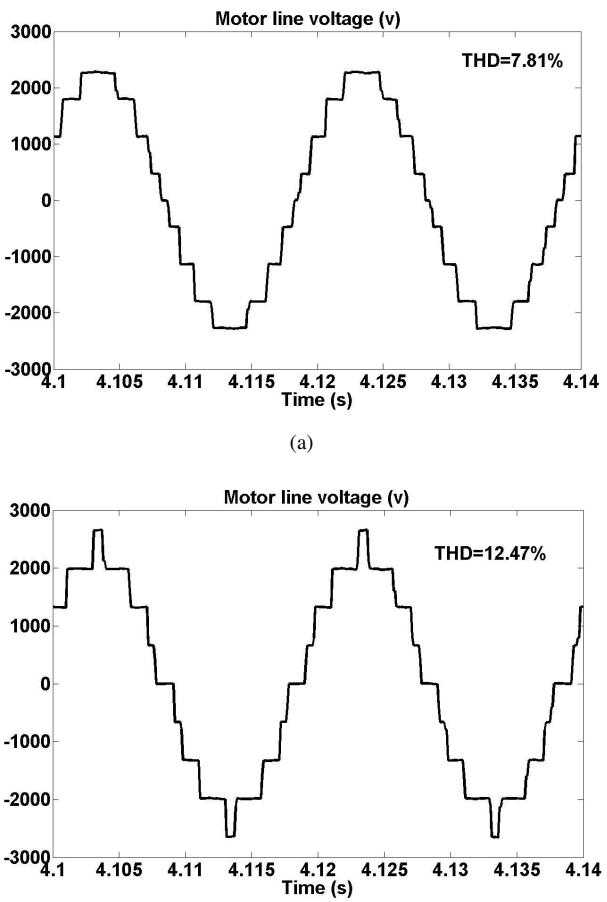
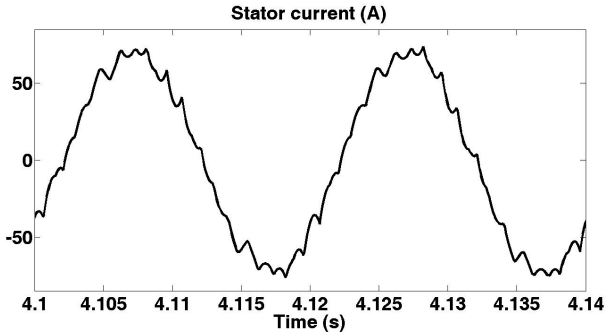
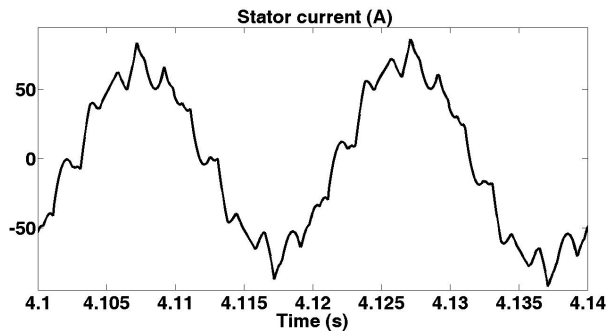


Fig. 10. motor line voltage (a) novel (b) conventional.



(a)



(b)

Fig. 11. Stator current (a) novel (b) conventional.

be seen from Fig. 12, the 7^{th} and 11^{th} harmonics in the novel mode are noticeably less than in the conventional mode. This improvement in the stator current stands for an improvement in the THD of the motor input voltage using the novel SHM-PWAM.

In order to compare the PWM-rectifier-inverter power dissipation in both modes under equal load conditions, their switching loss have been calculated according to [18]. The conduction loss in both modes are the same since it depends on the values of the IGBT collector-emitter saturation voltage drop, the diode forward voltage drop and the load current which do not differ in the two modes.

Fig. 13 shows the switching loss versus m_a in both modes. Each switching loss is the sum of both the rectifier and the inverter losses. As is depicted in the figure, the switching loss in the novel mode is less than in the conventional mode. This is apparent due to Fig. 7 since the optimized values of V_{refu} and V_{refl} in the novel mode are mainly less than the maximum dc link voltage used in the conventional mode.

In order to study the system transient in both modes, a simulation is performed for a step change in ${\omega_e}^*$. The value of ${\omega_e}^*$ was changed from 50π to 80πrad/sec at t=2s. According to the motor control strategy, this step change is proportional to a step change in m_a from 0.5 to 0.8. The solutions of the optimized equation (6) under these two different conditions have been shown for both modes in table III.

Fig. 14 shows the stator current transient at t=2s in the novel mode which reaches to its steady state value after about 0.25 sec.

Fig. 15(a) and 15(b) show the reference and actual values of the upper and lower capacitor voltages in the novel mode. The proposed voltages are changed at t=2s along with the step

TABLE III
SOLUTIONS OF THE OPTIMIZED EQUATION (6) UNDER TWO DIFFERENT CONDITIONS FOR BOTH MODES

m_a	$a_1(^\circ)$	$a_2(^\circ)$	$V_1(v)$	$V_2(v)$
0.5(novel)	23.6	58	446.7	618.6
0.5(Conventional)	47.61	83.61	939	939
0.8(novel)	11	35.24	812.2	468.5
0.8(Conventional)	30.65	66.65	939	939

change in ${\omega_e}^*$ and thus m_a. As can be seen from these figures, it takes about 15 ms for the upper capacitor and about 5 ms for the lower one to reach their steady state values.

Fig. 15(c) shows the sum of the capacitors' voltages from Fig. 15(a) and 15(b) and their related inverter output phase voltage (V_{an}). The PAM realization can be deduced from Fig. 15(c) as V_{an} changes due to the capacitors' voltages changing.

As mentioned earlier, the reference values of the upper and lower capacitor voltages in the conventional mode are constant. In other words, these values do not change due to a step change in ma. Fig. 16 shows these reference values and their related actual capacitors' voltages. Once these voltages

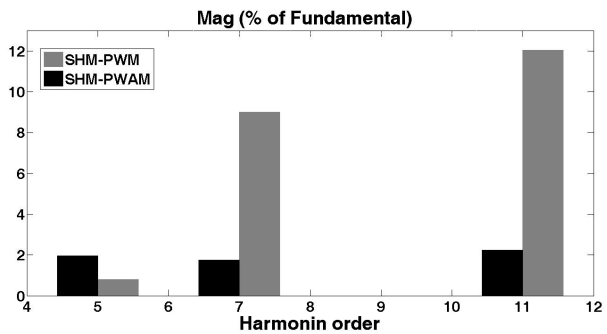


Fig. 12. 5^{th}, 7^{th} and 11^{th} harmonics magnitude in both modes.

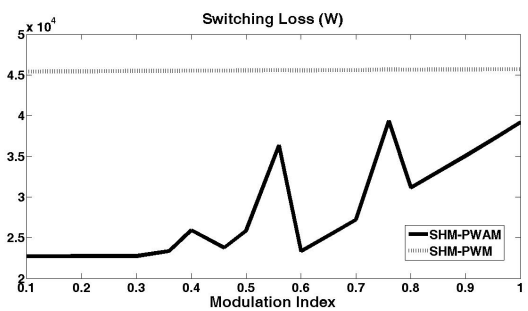


Fig. 13. Switching loss in both modes.

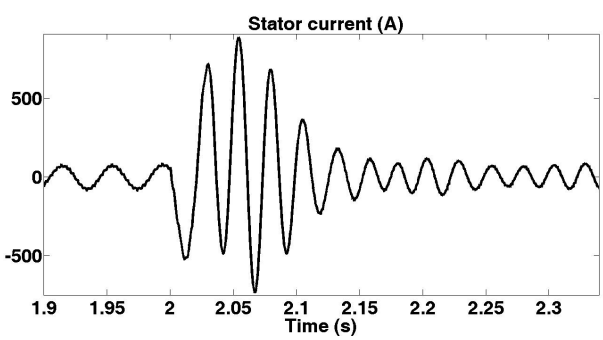
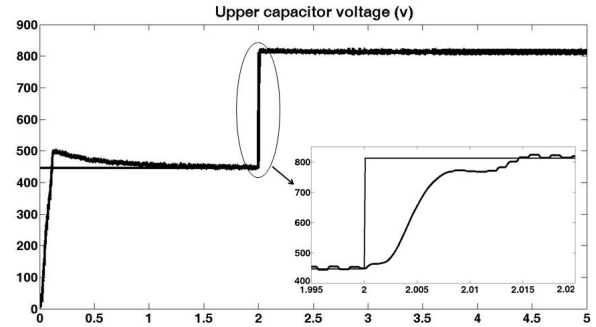
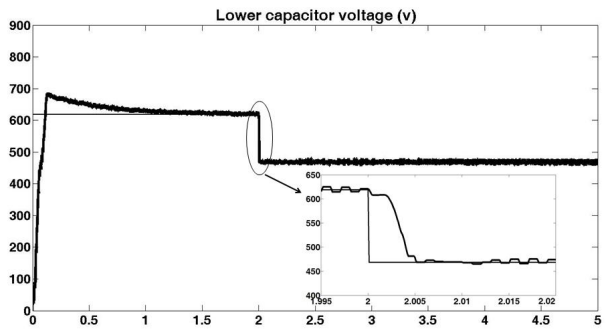


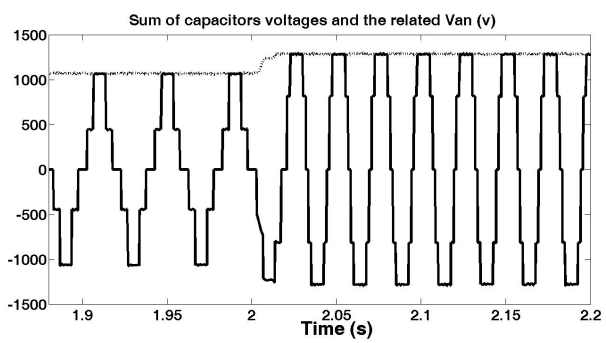
Fig. 14. The stator current transient at t=2s.



(a)



(b)

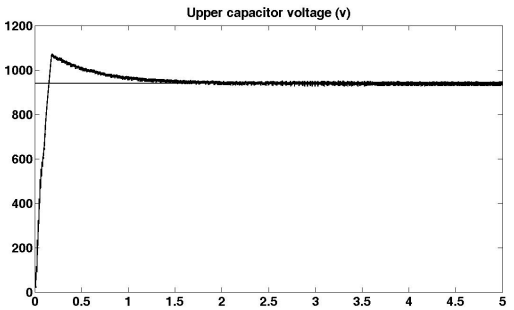


(c)

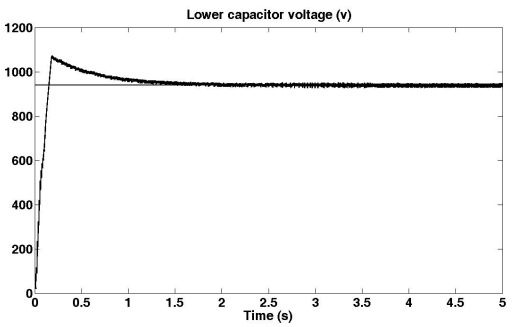
Fig. 15. (a) upper capacitor voltage (b) lower capacitor voltage (c) sum of capacitor voltages and the related V_{an}.

reach their steady state values, they are kept constant and non-flexible. Comparing Fig. 16 with Fig. 15(a) and 15(b) shows the better transient response of the capacitors' voltages in the novel mode at the beginning of the system's performance. This is due to this fact that the reference voltages have lower values according to Fig. 7 and table III.

Although only a five-level case is presented here, the novel SHM-PWAM control strategy can be equally applied to any



(a)



(b)

Fig. 16. (a) upper capacitor voltage (b) lower capacitor voltage.

number of levels.

V. CONCLUSIONS

A novel SHM-PWAM control strategy for multilevel inverters has been proposed in this paper. In the proposed SHM-PWAM the inverter's dc sources values have been used as degrees of freedom in addition to the switching angles, mitigating more selective harmonics when compared to the conventional SHM-PWM control strategy. This strategy uses PAM along with PWM. Simulation results show that a five-level inverter with SHM-PWAM has a better THD and also less power dissipation when compared to the same inverter with SHM-PWM. The SHM-PWAM control strategy can also be applied to more voltage levels.

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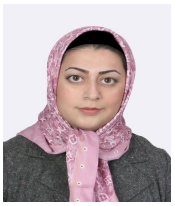

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