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New Reference Generation for a Single-Phase Active Power Filter to Improve Steady State Performance

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Abstract

This paper proposes a new algorithm to generate a reference signal for an active power filter using a sliding-window FFT operation to improve the steady-state performance of the active power filter. In the proposed algorithm the sliding-window FFT operation is applied to the load current to generate the reference value for the compensating current. The magnitude and phase-angle for each order of harmonics are respectively averaged for 14 periods. Furthermore, the phase-angle delay for each order of harmonics passing through the controller is corrected in advance to improve the compensation performance. The steady-state and transient performance of the proposed algorithm was verified through computer simulations and experimental work with a hardware prototype. A single-phase active power filter with the proposed algorithm can offer a reduction in THD from 75% to 4% when it is applied to a non-linear load composed of a diode bridge and a RC circuit. The active power filter with the proposed reference generation method shows accurate harmonic compensation performance compared with previously developed methods, in which the THD of source current is higher than 5%.

Key Words: DSP(Digital Signal Processor), FFT(Fast Fourier Transform), Harmonic Phase-angle Delay, PLL(Phase-Locked Loop), Sliding Window, THD(Total Harmonic Distortion)

I. INTRODUCTION

An active power filter can effectively remove the harmonics generated by a non-linear load [1]. Two control methods are commonly used as active power filters [2]. The source-current detection method requires indirect control of the compensating current, while the load-current detection method requires direct control of the compensating current [3]. In the early days both methods were implemented using analog control circuits.

As the DSP came into wide use, many researchers proposed a DSP controller for an active power filter which uses the FFT algorithm to generate the compensating current from the load current [4], [5]. A fixed-point DSP with the FFT algorithm was proposed for the controller. However, the performance of the proposed system was not so desirable due to the low accuracy of the FFT algorithm and the performance of the DSP itself [6], [7].

A floating-point DSP with the FFT algorithm was proposed for a controller. However, the proposed controller shows inaccurate performance due to the difficulty of obtaining stabilized results from the FFT operation for each cycle of the power frequency [8].

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The FFT result for each cycle is not the same due to an inaccurate starting point, inaccurate sampling, and the frequency change of the power system. This unevenness can be removed by the moving average technique for the magnitude and the phase of each order of harmonics obtained from the FFT operation.

In this paper the period of the moving average was determined for 14 periods of load current, in which the number of periods was determined considering the performance of the DSP, which carries out the proposed algorithm in real time. The phase-angle delay of the reference signal that occurs when it passes through the DSP controller is corrected in advance to obtain accurate compensation. The operation of the proposed algorithm was verified through computer simulations using a user-defined model coded in C-language and through experimental work with a hardware prototype.

II. SINGLE-PHASE ACTIVE FILTER

The digital loads include a rectifier to convert the single-phase AC power to DC power. The rectifier can be simply represented by the circuit shown in Fig. 1.

The voltage and current waveforms of a single-phase rectifier are shown in Fig. 2. The DC filter capacitor is very effective at obtaining a constant voltage on the DC side. However, it makes the input AC current distorted, due to many

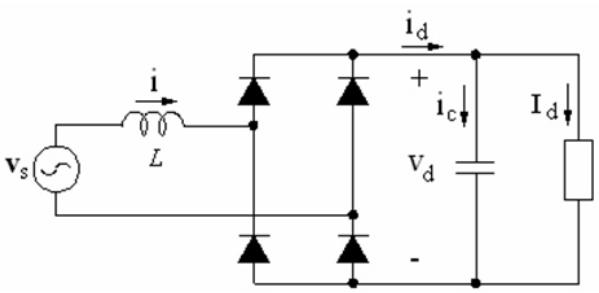


Fig. 1. Simplified circuit of rectifier for digital load.

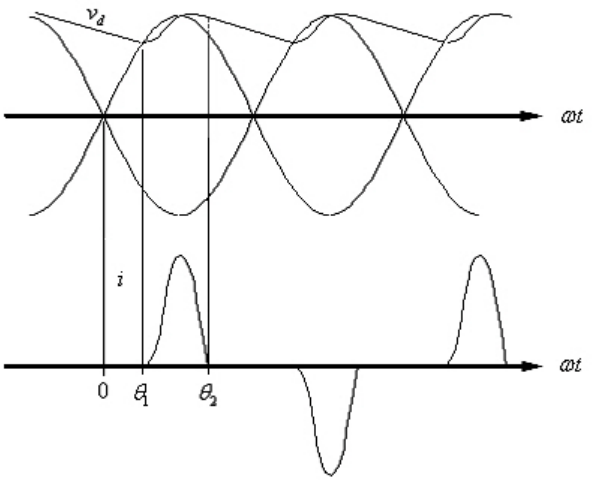


Fig. 2. DC voltage, AC input current.

low order harmonics. Therefore, the rectifier is considered as a non-linear load when it is looked at from the source side.

The input AC current has a frequency spectra obtained through the Fourier transform and shown in Fig. 3. The magnitudes of the 3rd, 5th, 7th, and 9th harmonics are respectively about 68%, 28%, 9%, and 7% of the fundamental component. This value is very high compared with the level of the higher order harmonics. In order to make the input AC current sinusoidal, these low order harmonics should be effectively removed. In this paper it is assumed that the active power filter removes the harmonics of the 3rd to 19th order.

Fig. 4 shows the operational principle of the active power

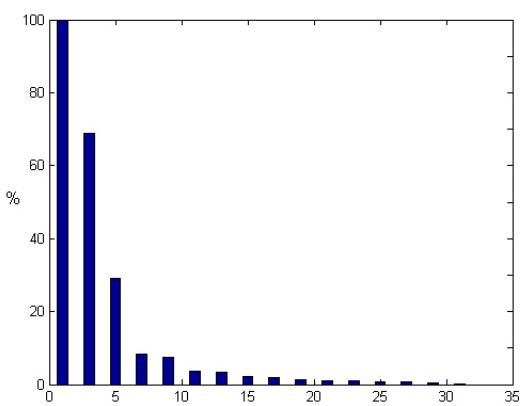


Fig. 3. Frequency characteristic of input AC current.

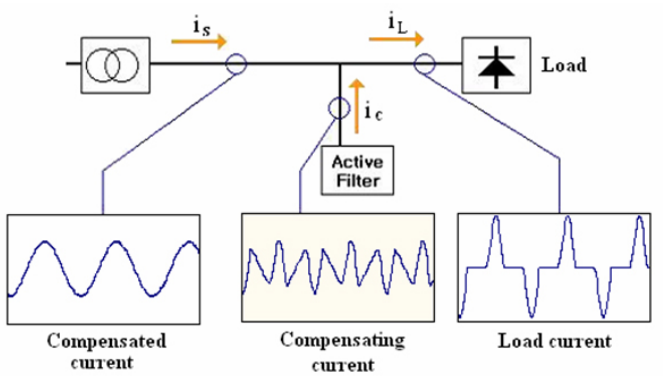


Fig. 4. Principle of active power filter.

filter which makes the source current sinusoidal by injecting a harmonic current to the non-linear load.

The input current through the non-linear load can be expressed by equation (1) or equation (2).

$$i_L(t) = \sum_{n=1}^{\infty} (a_n \cos n\omega_0 t + b_n \sin n\omega_0 t) \quad (1)$$

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega_0 t + \theta_n) \quad (2)$$

Where, $I_n = \sqrt{a_n^2 + b_n^2}$ and $\theta_n = \tan^- 1 \frac{a_n}{b_n}$

In order to make the source current sinusoidal, the harmonic components with a higher order than the fundamental component should be removed by injecting the same components from the active power filter.

The load-current detection method measures the load current and extracts the harmonic components from it with a negligible phase-angle delay. These harmonic components are used for the reference signal of the compensating current. The active power filter is controlled so that the output current tracks the reference signal. This enables it to make the source current sinusoidal.

The load-current detection method is easily implemented using a DSP controller. When an analog filter is used to extract the reference signal from the load current, the compensation of the phase delay is not easy. However, the DSP can offer easy extraction of the reference signal through the FFT operation and independent compensation of the harmonic phase-angle delay.

The FFT operation for every cycle of the power frequency produces uneven values of the magnitude and phase-angle due to an inaccurate starting point, sampling inaccuracy, and the frequency change of the power system. This unevenness can be removed by the moving average technique for the magnitude and the phase-angle of each order of harmonics obtained from the FFT operation.

III. PROPOSED REFERENCE GENERATION METHOD

Fig. 5 shows the configuration of a single-phase active power filter including a DSP controller with the proposed

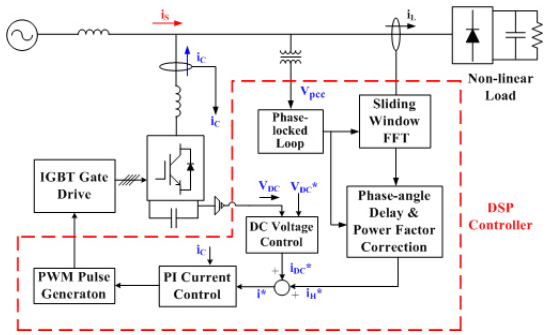


Fig. 5. Controller structure with proposed algorithm.

algorithm. The inverter of the active power filter has a full-bridge configuration, and the controller is implemented with software based on the DSP. The controller has two current sensors for measuring the load current and the active power filter current, and two voltage sensors for measuring the voltage at the common connection point and the DC voltage of the active power filter.

The voltage at the common connection point measured with a PT (potential transformer) is converted into a digital value and sent to the PLL (phase locked loop) module in the DSP. The load current measured with a CT (current transformer) is converted into a digital value and sent to the FFT module in the DSP. The harmonic components are extracted from the load current and its phase-angle delays are compensated to generate the reference signal.

A control algorithm balancing the DC voltage of the active power filter is included to cover the system losses. The output of this algorithm is added to the extracted reference signal to generate the final reference signal for the inverter output current. The final reference signal is compared with the actual inverter output current, and passed through the current control to generate the PWM pulses for gating.

A. SLIDING WINDOW FFT OPERATION

From a resource management point of view, the FFT operation can not be executed at each sampling period. Therefore, the FFT operation is performed once per cycle of power frequency. However, the FFT result for each cycle of power frequency is not same due to an inaccurate starting point, inaccurate sampling, and the frequency change of the power system. This unevenness can be removed by the moving average technique for the magnitude and the phase-angle for each order of harmonics obtained from the FFT operation. Fig. 6 shows the process of the sliding-window FFT operation. The period of the sliding-window was determined to be n times the period of the load current.

The magnitudes and phase-angles obtained from the FFT operation for the 1st to nth of the load current are averaged respectively to generate the (n+1)th period of the reference current. Those obtained from the FFT operation for the 2nd to (n+1)th of the load current are averaged respectively to generate the (n+2)th of the reference current. This process continues while the active power filter compensates the harmonic currents.

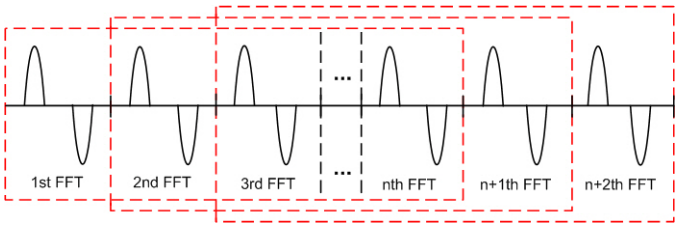


Fig. 6. Process of sliding-window FFT operation.

It is clear that the enlargement of the sliding window offers more accurate result, but slower transient response. Therefore, the width of the sliding window is carefully determined. In this paper the width of the sliding window is determined to be 14 periods of power frequency so as to improve the performance of the active power filter in the steady state. The unevenness of the FFT operation results due to inaccurate starting and sampling error can be mitigated through the moving average scheme, in which the width of the sliding window was decided considering the performance limit of the DSP.

The sliding-window FFT operation offers effective resource management to implement the control algorithm on the DSP. In this paper, a sampling frequency of 11520Hz was used, with samples 192=64*3 times per cycle of 60Hz power frequency. The ideal sampling period is 86.80555, but 86.8 was used in the actual DSP. Another technique for the reduction of execution time is to make the FFT algorithm run outside the main control routine. This helps to minimize the influence of the FFT operation on the other control algorithms.

Fig. 7 shows the execution time of the FFT and the time difference for the 64 samples from the starting time of execution. The value of $\triangle T_{FFT}$ is the required time to complete the FFT operation and the value of $\triangle T_{DLY}$ is the time difference between the zero-crossing point and the starting point of the FFT. Since the FFT starts at the point where the source voltage crosses over the zero point, the 64 samples are the data obtained during one period of the previous fundamental waveform. Therefore, the result of the FFT can be obtained at the instant after elapsing the zero-crossing point, $\triangle T_{FFT}$, and $\triangle T_{DLY}$. When the load current is restored, this delay should be considered correct.

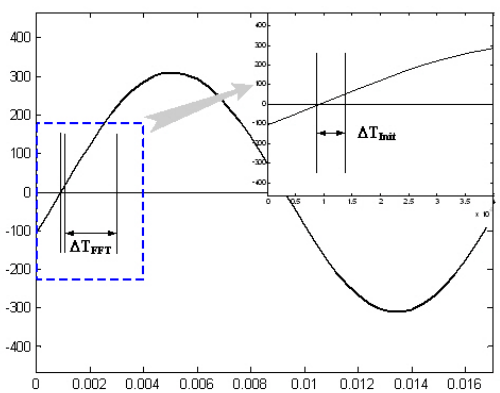


Fig. 7. Phase-delay compensation due to FFT starting point and FFT execution time.

B. PHASE-DELAY CORRECTION

The harmonic reference signal passes through the current controller, in which each order of harmonic components brings about a different phase-angle delay. In order to perform accurate compensation with the active power filter, the harmonic phase-angle delay of the reference signal should be corrected in advance. Table I shows the harmonic phase-angle delay for the 3rd to 19th order, calculated using Matlab software, which is composed of the phase delay and the sampling delay.

The reference signal is generated from the load current as shown in Fig. 5. The load current is measured with a sampling rate of 192 and selected with a sampling rate of 64 for the FFT operation. The harmonic reference signal is extracted though the sliding-window FFT operation. Its phase angle is corrected respectively considering the delay value described in Table I. After that, one sample delay due to the digital control is also considered. The phase-angle delay of fundamental component is added to the corrected reference signal to compensate the power factor using the output signal from the PLL [9].

TABLE I
HARMONIC PHASE-ANGLE DELAY

Order	Phase Delay (deg)	Sampling Delay (deg)
3rd	-12.6	-8.44
5th	-20.5	-14.06
7th	-27.5	-19.69
9th	-33.9	-25.31
11th	-39.4	-30.94
13th	-44.2	-36.56
15th	-48.3	-42.19
17th	-51.8	-47.82
19th	-54.8	-53.44

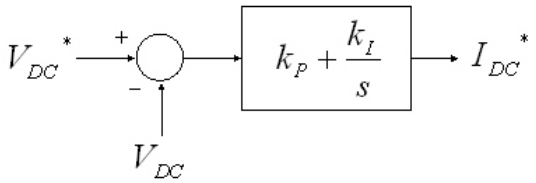
C. POWER FACTOR CORRECTION

The reference current obtained through the FFT operation experiences a harmonic phase-angle delay as explained in the previous section. Therefore, the reference current for compensating the load current harmonics is represented by the following equation:

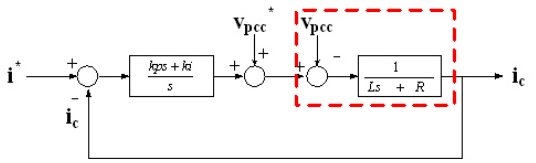
$$i_c^*(t) = \sum_{n=2}^{19} I_n \sin(n\omega_0 t + \theta_n + \phi_n). \quad (3)$$

The delay angle for each harmonic component is compensated respectively according to the delay angle shown in Table I. The power factor correction is to make the compensated source current in phase with the source voltage. The reference value of the compensating current should include a fundamental component which has the same magnitude of reactive component as a load current with the opposite phase angle. So, the reference signal for power factor correction and harmonics compensation is represented by the following equation:

$$i_c^*(t) = \sum_{n=2}^{19} I_n \sin(n\omega_0 t + \theta_n) - (I_1 \sin\theta_1)\sin(\omega_0 t - 90^\circ). \quad (4)$$



(a) DC voltage control.



(b) Output current control.

Fig. 8. Control Structure for DC Voltage and Current Control.

D. DC VOLTAGE CONTROL AND CURRENT CONTROL

Fig. 8(a) shows the configuration of the DC voltage control, which is composed of PI control. The reference value of the DC voltage is compared with the measured DC voltage, and the error is sent to the PI control to calculate the iDC current, which is represented by equation (5).

$$i_{DC}^*(t) = (k_p + \frac{k_I}{S})(v_{DC}^* - v_{DC}). \quad (5)$$

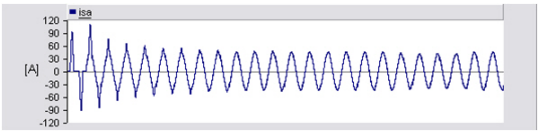
Fig. 8(b) shows the current control which is the key item for the performance of a single-phase active power filter. The current control is composed of PI control and a plant model for the inverter, which is represented by the dotted lines.

The measured inverter current is compared with the reference value and passed through the PI control. The output of the PI control is added to the nominal voltage at the point of common connection and generates the reference voltage at the point of common connection. This value is compared with the measured voltage at the point of common connection, and sent to the transfer function of the coupling reactor. The bandwidth of the proposed current control is approximately determined to be 7200rad/sec by using a frequency response analysis. This bandwidth is enough to cover up to the 19th harmonics.

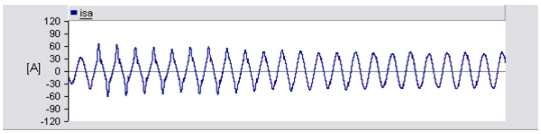
IV. COMPUTER SIMULATION

Various computer simulations with PSCAD/EMTDC have been carried out to analyze the performance of the proposed controller including the single-phase active filter. The power circuit is represented using a built-in model in the PSCAD/EMTDC, while the control circuit is represented using a user-defined model programmed in C-code. The major circuit parameters are described in Table II.

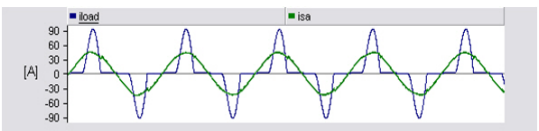
Fig. 9 shows the simulation results based on the developed simulation model. Fig. 9(a) shows the variation of the source current when the active power filter starts up. It takes about 14 periods to compensate the source current perfectly, which is the width of the sliding-window FFT. Fig. 9(b) shows the variation of the source current when the load changes in the step manner. It also takes about 14 periods to compensate the source current perfectly. Fig. 9(c) shows the waveforms of the



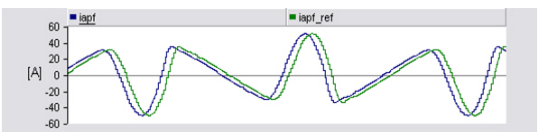
(a) Transient analysis for Start-up.



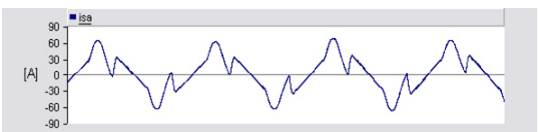
(b) Transient analysis for step load change.



(c) Source current and load current.



(d) Reference with and without harmonic phase-angle delay.



(e) Source current without harmonic phase delay.

Fig. 9. Simulation results of active power filter.

TABLE II
CIRCUIT PARAMETERS FOR POWER CIRCUIT

Parameter	Values
Source Voltage	220V, 60Hz
Source Impedance	$L_s = 1mH$
Non-linear Load	$C = 600\mu F$, $R = 13.3\Omega$
DC capacitor	$C = 1650\mu F$
Filter reactor	4mH
Switching Frequency	11.52KHz

source current and the load current. It is confirmed that the load current is compensated by the active power filter to make the THD of the source current less than 3%. Fig. 9(d) shows two reference signals with and without compensation of the harmonic phase-angle delay. Fig. 9(e) shows the source current without compensation of the harmonic phase-angle delay. Its distortion level is too high due to inaccurate compensation.

V. HARDWARE PROTOTYPE

A 3kVA hardware prototype was built and tested to confirm the simulation results and to verify the feasibility of hardware implementation. Fig. 10 shows a picture of the prototype, which is composed of a full-bridge inverter and the developed controller with a DSP. The active power filter is connected in shunt with the non-linear load, which is connected with the source of 220V. The full-bridge inverter consists of two dual IGBTs with 1200V/100A ratings. The switching frequency of the inverter is 11.52 kHz, which is exactly the same as that used in the simulation.

The DSP control board shown in Fig. 11 was designed using a TMS320vc33 chip for real time operation and an EPLD chip for PWM logic implementation. There are two external memory chips, two A/D converter chips, and one D/A chip. Two current sensors, one DC voltage sensor, and one PT for measuring the AC voltage are included in the prototype. A non-linear load is represented by a 3kVA full-wave diode rectifier with a shunt-connected RC. The source impedance is also considered using a series-connected reactor.

Fig. 12 shows the experimental results produced with the prototype. Fig. 12(a) shows the variation of the source current when the active power filter starts up. It takes about 14 periods to compensate the source current perfectly, which is the width of the sliding-window FFT. However, the transient value is not so high. This means that the controller operates in a stable manner in the steady state even though the transient response is slow. Fig. 12(b) shows the variation of the source current when the load changes in a step manner. It also takes about 14 periods to compensate the source current perfectly. Fig. 12(c) shows the typical waveform of a non-linear load composed of a diode bridge with a RC circuit. The compensating current shown in Fig. 12(d) is added to the load current, then the source current becomes sinusoidal as shown in Fig. 12(e).

Fig. 13 shows the harmonic analysis results for the load current and the source current. It is confirmed that the active power filter with the proposed controller accurately compensates the harmonic current in the non-linear load. The THD of the source current is less than 4%, while the THD of the load current is 75%. The fundamental component after compensation is slightly increased by the power factor correction.

The active power filter with the proposed reference generation method shows accurate harmonic compensation compared with methods described in [2], [4], [6]–[8], in which the THD of the source current is higher than 5%. Particularly, the non-linear load with a RC circuit is higher than that with a RL circuit because the former has a more severer distortion than the latter. Considering this fact, it is confirmed that the active power filter with the proposed method offers accurate harmonic compensation for the non-linear load.

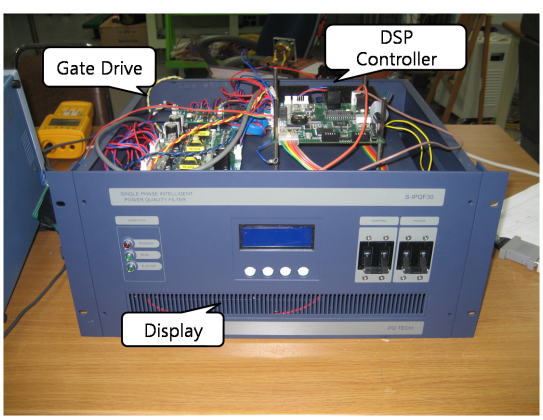


Fig. 10. Single-phase Active Power Filter Prototype.

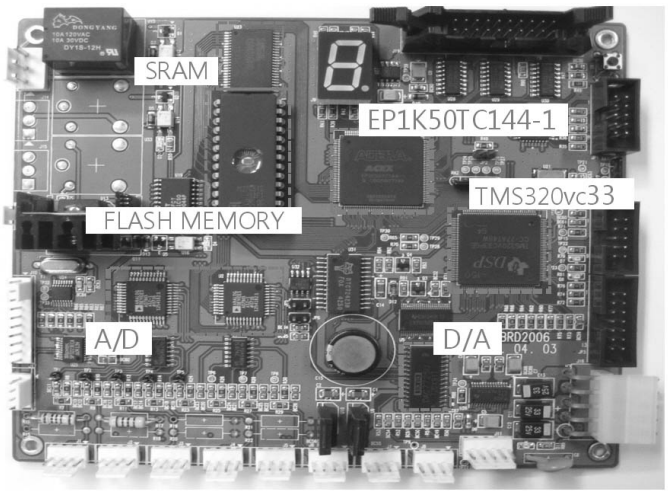
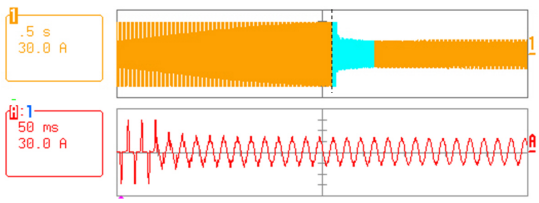
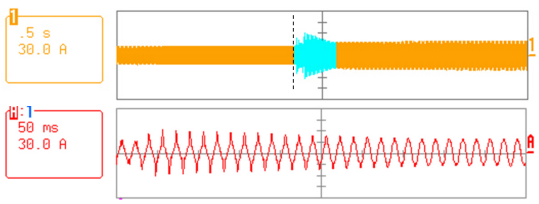


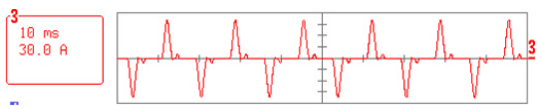
Fig. 11. DSP Control Board based on TMS320vc33.



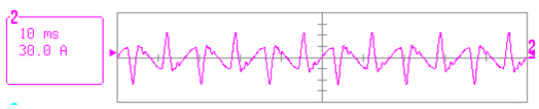
(a) Source current for start-up.



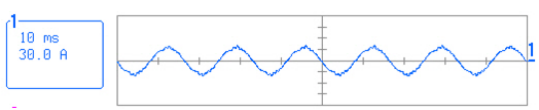
(b) Source Current for step load change.



(c) Load current.



(d) Compensating current from active power filter.

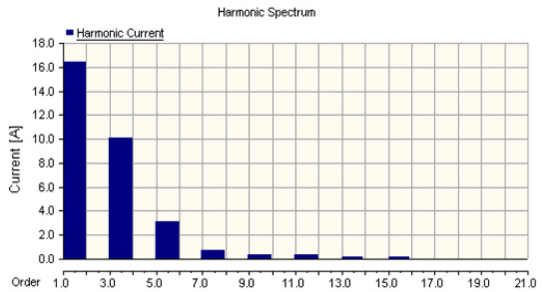


(e) Source current (compensated current).

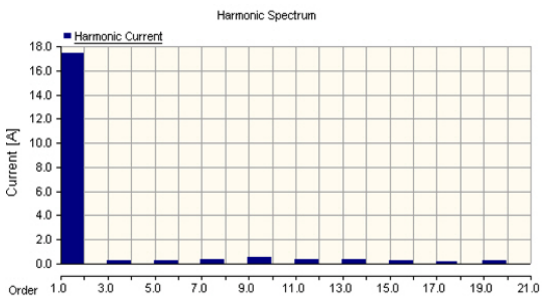
Fig. 12. Waveforms of experimental result.

VI. CONCLUSIONS

In this paper a new algorithm to generate a reference signal for an active power filter was proposed. In the proposed algorithm the sliding-window FFT operation is applied to the load current to generate the reference value of the compensating current. The magnitude and phase-angle of each order of harmonics are respectively averaged for 14 periods. The phase-angle delay for each order of harmonics passing through the controller is corrected in advance to improve the compensation performance.



(a) Load current.



(b) Source current.

Fig. 13. Harmonics analysis results.

The proposed algorithm requires 14 periods of stabilizing time against the start-up and a sudden load change due to the width of the sliding window. The steady-state and transient performance of the proposed algorithm was verified through computer simulations and experimental work with a hardware prototype. A single-phase active power filter with the proposed algorithm can offer a reduction in THD from 75% to 4% when it is applied to a non-linear load composed of a diode bridge and a RC circuit.

The active power filter with the proposed reference generation method shows accurate harmonic compensation performance compared with other previously developed methods, in which the THD of the source current is higher than 5%. When considering that the non-linear load with a RC circuit is higher than that with a RL circuit, the active power filter with the proposed reference generation method offers particularly accurate harmonic compensation for the non-linear load.

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REFERENCES

[1] Byung-Moon Han, Byung-Yeol Bae, and Seppo J. Ovaska, "Reference signal generator for active power filters using improved adaptive predictive filter," *IEEE Trans. on Industrial Electronics*, Vol. 52, No. 2, Apr. 2005.

[2] J. C. Wu and H. L. Jou, "Simplified control method for the single-phase active power filter," *IEE Proc. on Electric Power Application*, Vol. 143, No. 3, pp. 219-234, May 1996.

[3] S. Huang and J. Wu, "A control algorithm for three-phase three-wired active power filters under non-ideal main voltage," *IEEE Trans. On Power Electronics*, Vol. 14, No. 4, pp. 753-760, Jul. 1999.
[4] W. Shireen, L. Tao, and M. Arefeen, "Implementation of a DSP based active filters for electric power distribution systems suppling nonlinear load," *IEEE Applied Power Electronics Conference and Exposition APEC 2000*, Vol. 1, pp. 438-442, Feb. 2000.
[5] S. George and V. Agarwal, "A novel DSP based algorithm for optimizing the harmonics and reactive power under non-sinusoidal supply voltage conditions," *IEEE Trans. On Power Electronics*, Vol. 20, No. 2, pp. 2526-2534, Oct. 2005.
[6] R. Oliviera, F. Libano, R. Braga, and J. Lima "Low cost single-phase active power filter controlled by DSP," *IEEE 10th International Conference on Harmonics and Power Quality*, Vol. 2, pp. 524-528, 2002.
[7] D. Lindeke, S. Mussa, F. De Souza, and I. Barbi "Single-phase active power filter with a digital signal processor-DSP," *IEEE Power Electronics Specialist Conference PESC 2004*, Vol. 2, pp. 1024-1027, Jun. 2004.
[8] L. Asiminoaei, F. Blaabjerg, and S. Hansen, "Evaluation of harmonic detection methods for active power filter applications," *IEEE Applied Power Electronics Conference and Exposition, APEC 2005*, Vol. 1, pp. 635-641, Mar. 2005.
[9] B. M. Han, B. Y. Bae, and Y. S. Jeong, "Load simulator with power recovery capability based on voltage source converter-inverter set," *IEE Proc. on Electric Power Application*, Vol. 153, No. 6, Nov. 2006.

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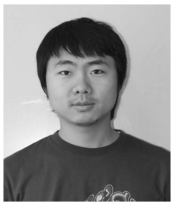

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