JPE 10-5-1

Digital Control Methods of Two-Stage Electronic Ballast for Metal Halide Lamps with a ZVS-QSW Converter

Yijie Wang†, Xiangjun Zhang*, Wei Wang*, and Dianguo Xu*

†* Dept. of Electrical and Electronics Engineering, Harbin Institute of Technology, Harbin, China

Abstract

This paper presents a new kind of digital control metal halide lamp electronic ballast. A zero-voltage-switch quasi-square-wave (ZVS-QSW) dual Buck converter is adopted here. In this paper, a digital control method is proposed to achieve ZVS for the converter. This ZVS can be realized during the whole working condition. Single-cycle-peak-current control is proposed to solve the problem of excessive inductor current during a low-frequency reversal transient. Power loop control is also realized and its consistency for different lamps is good. An AVR special microcontroller for a HID ballast is used to raise the control performance, and the low-frequency square-wave control method is adopted to avoid acoustic resonance. A 70W prototype was built in the laboratory. Experimental results show that the electronic ballast works reliably. Furthermore, the efficiency of the ballast can be higher than 92%.

Key Words: Single-cycle-peak-current control, Square-waveform, ZVS, ZVS-QSW

I. Introduction

As one kind of gas discharge lamp (HID), the metal halide lamp has developed very fast since it has many advantages such as long life and good color rending. The low power metal halide lamp which is mainly used for interior illumination has developed rapidly because it is closely bound up with modern life. Because HID lamps have a negative resistance characteristic, they must be used with a ballast. The main point for a ballast is to avoid acoustic resonance. General methods to avoid acoustic resonance are the low frequency square wave method, the high frequency method, the frequency selection method, the frequency or phase modulation method and the ultrahigh frequency method[1]–[9].

Compared to other gas discharge lamps, a low power metal halide lamp with a smaller discharge tube has a more serious acoustic resonance problem, and the low-frequency square-wave method is commonly used in practical applications. Paper [10] presents a topology with a two-stage full bridge inverter, and it simplifies the circuit since it combines the voltage step down circuit and the full bridge inverter. Paper [11] presents a two-stage topology, which simplifies the circuit even further. Papers [12] and [13] present topologies with a lot fewer components, but their power factor is lower than others and their power is not constant in a low-frequency cycle. Single-stage topologies with a lot fewer components have developed rapidly in recent years. However they reduce the power factor and increase the stress of the power switches.

The key factor affecting the power density is the passive elements. The most effective way of enhancing the power density is to increase the operating frequency. However, a buck converter operating in CCM mode is not applicable when the operating frequency is beyond 100 kHz because of the reverse recovery of the diode and EMI problems. Furthermore, the MOSFET is in hard switch mode and the turn-on loss is significant. To solve these problems, a ZVS dual Buck quasi-square-wave (QSW) dual buck converter is adopted here. The principle of QSW is explained in detail. The adaptive ZVS control strategy guarantees zero voltage turn-on of the switch during the entire process of lamp operation and it is effective on various lamps from different manufactures. A microcontroller AT90PWM2 for lighting helps to improve the performance and to simplify the hardware circuit. The prototype of a 70W digital electronic ballast for metal halide lamps proves the validity of the control strategy. The operating frequency is beyond 100 kHz and the whole system efficiency is 92%.

The transition process is complex because of the characteristics of metal halide lamps. The corresponding control method is applied to a lamp according to the features of each stage. The one-cycle-peak-current control strategy is proposed to limit the excessive current during the commutation period and the transition stage. The one-cycle-peak-current control strategy and the adaptive ZVS control strategy play

Manuscript received Apr. 2, 2010; revised Jul. 18, 2010
† Corresponding Author: wangyijie1982@gmail.com
Tel: +86-451-86413420, Fax: +86-451-86413420, Harbin Institute of Tech.
* Dept. of Electrical and Electronics Engineering, Harbin Institute of Technology, China

Fig. 1. Configuration of the ballast.

an important role in each stage. The average input power control method based on the adjustment of the turn-on time is simple and effective. Experiments with different lamps prove the feasibility and accuracy of the constant power control strategy.

II. Configuration of the Ballast

It can be seen from Fig. 1 that the single entry AC passes through the filter circuit to curtail the electromagnetic interference. Then the voltage signal passes through the rectifying bridge and it changes into a single entry DC. Then the signal passes through the power-factor correction (PFC) circuit, so that a 400V dc bus voltage is produced. The last part of the circuit is the main circuit which is a dual-buck inverter circuit and its functional mode is controlled by a chip microprocessor. Here a MC33262 Chip is chosen to realize the power factor correction.

III. ZVS-QSW Converter

Fig. 2 shows the dual buck converter adopted in this paper. The bus voltage is 400V provided by a PFC circuit. The power field effect tube S_1 and the ultra-fast-recovery diode VD_1 form one bridge arm, and S_2 and VD_2 form the other bridge arm. D_{s1} and C_{s1} are the body diode and the output capacitance of S_1. D_{s2} and C_{s2} are the body diode and the output capacitance of S_2.L_1 and L_2 are the filtering inductance of the buck circuits. C_1 and C_2 are the filtering capacitance of the buck circuits. C_3 and C_4 are not only the half bridge capacitance, but also the output capacitance of the PFC circuit.R_{lamp} is the equivalent resistance of the lamp in the steady state. In the circuit, S_1, VD_1, L_1, C_1 and C_2 form one buck circuit while S_2, VD_2, L_2, C_1 and C_2 form the other buck circuit.

Fig. 2. Novel two stage dual Buck topology.

The circuit has two working modes, and the drive signals of the switches are shown in Fig.3 and Fig.4. When the switch S_1 works with a high working frequency and S_2 is turned off, the circuit works in mode1. When the switch S_2 works with a high working frequency and S_1 is turned off, the circuit works in mode2. Therefore, the converter works in two modes in a low frequency and the load gets a low-frequency square waveform.

In mode1, there are four working modes with a high working frequency, which are shown in Fig.5.

Mode1(a): This mode starts at time t_0. The capacitor C_{s1} resonates with the buck inductorL_1, and the voltage between the drain pole and the source pole of S_1 increases linearly,

Fig. 3. Working modes of the switches.

Fig. 4. Drive signal of the switch.

Fig. 5. Equivalent circuits for each mode.

until it equals the bus voltage. Here we define that $v(t)$ is the voltage between the drain pole and the source pole of S_1, and that $i(t)$ is the inductor current. Then the equations can be obtained as in (1).

$$\begin{cases} L_1 \dfrac{di}{dt} + v = V_g - V_0 \\ C_{s1} \dfrac{dv}{dt} = i \end{cases}. \tag{1}$$

Since $v(0) = 0$, (2) and (3) can be obtained from (1).

$$v\,(t) = (V_{bus} - V_0)(1 - \cos\omega_r t) + Z_r i(0) \sin\omega_r t \tag{2}$$

$$i\,(t) = i(0)\cos\omega_r t + \frac{V_g - V_0}{Z_r}\sin\omega_r t. \tag{3}$$

Here:
V_{lamp}——lamp voltage, $V_{lamp} = V_0 - V_g/2$.
V_g——bus voltage.
V_0——output voltage of the converter.
ω_r——resonance angular frequency, $\omega_r = 1/\sqrt{L_1 C_{s1}}$.
Z_r——characteristic impedance, $Z_r = \sqrt{L_1/C_{s1}}$.
Q_p——quality factor, $Q_p = R_{lamp}/Z_r$.
M——voltage transmission rate, $M = V_0/V_g$.
θ_n——angle, $\theta_n = \omega_0(t_n - t_{n-1})$, where $n = 1, 2, 3$ or 4.

Because the working frequency is about 100kHz, the time from $t0$ to $t1$ is about 100ns. Therefore, the last time of this mode is very small compared to the whole period, so $\theta_1 \approx 0$, and $i(t_0) = i(t_1) = i_{\max}$.

Mode1(b): When $v\,(t)$ reaches the bus voltage, the diode VD_1 is turned on, the voltage $v\,(t)$ is clamped to 400V, the inductor current runs through the diode and decreases linearly until it reaches zero. Then the equation can be obtained from (4).

$$i(t) = -\frac{V_0}{L_1}(t - t_1) + i(t_1). \tag{4}$$

At time t_2, the current $i(t)$ reaches zero. Then equation (5) can be obtained.

$$-\frac{V_0}{L_1}(t_2 - t_1) + i(t_1) = 0 \rightarrow \theta_2 = \frac{Z_r i(t_1)}{V_0}. \tag{5}$$

Mode1(c): At time t_2, the inductor current decreases to zero, the diode VD_1 is turned off, L_1 resonates with C_{s1}, and the current of the inductor changes its direction, so that the voltage of C_{s1} begins to decrease from the bus voltage. When the voltage decrease to zero, this mode ends. In this mode, the equation can be obtained from (6) and (7).

$$v\,(t) = V_g - V_0 + V_0 \cos\omega_r\,(t - t_2) \tag{6}$$

$$i\,(t) = -\frac{V_0}{Z_r}\sin\omega_r\,(t - t_2)\,. \tag{7}$$

Since this model ends at time t_3, and $v(t_3) = 0$, the equation can be obtained as follows:

$$\begin{aligned} &\cos\omega_r\,(t_3 - t_2) = \frac{V_0 - V_g}{V_0} \\ \rightarrow\ &\cos\theta_3 = \frac{M-1}{M} \\ \rightarrow\ &\theta_3 = \cos^{-1}\frac{M-1}{M}. \end{aligned} \tag{8}$$

It is obvious that, to achieve ZVS for the converter, the voltage transmission ratio must satisfy the equation as follows:

$$\frac{\pi}{2} < \theta_3 < \pi \rightarrow -1 < \cos\theta_3 < 0 \rightarrow 0.5 < M < 1. \tag{9}$$

In this paper, V_0 is always higher than $V_g/2$ during the whole low frequency period. Therefore the circuit can not only satisfy the ZVS condition in the transition stage, but also in the steady stage.

In this stage, the minimum inductor current can be described as (10).

$$I_{\min} = -\frac{V_0}{Z_r} = -\frac{V_g/2 + V_{Lamp}}{\sqrt{L_1/C_{S1}}}. \tag{10}$$

With (6) and (7), the current at time $t_3$can be described as follows:

$$i(t_3) = -\frac{V_0}{Z_r}\sin\theta_3 = -\frac{V_g}{Z_r}\sqrt{2M-1}. \tag{11}$$

Mode1(d): At time t_3, the voltage $v\,(t)$decreases to zero, the inductor current runs through the body diode of S_1, and the voltage between the drain pole and the source pole of S_1 is clamped in the ZVS state. At this time, if the turn-on signal of S_1comes before the inductor current changes its direction, S_1 will be turned on in the ZVS state, and the inductor current will run through $S_1$and increase linearly. When $S_1$is turned off, the inductor current reaches its maximum value. In this mode, the equation can be obtained as follows:

$$i(t) = \frac{V_g - V_0}{L_1}(t - t_3) + i(t_3). \tag{12}$$

With (11) and (12), the time between v(t) decreases to zero and the negative inductor current decreases to zero, which can be described as follows:

$$t_{delay} = \frac{1}{\omega_r} \times \frac{\sqrt{2M-1}}{1-M}. \tag{13}$$

In practical use, when $v\,(t)$ is detected to decreased to zero, the MCU will send a logical drive signal to the drive circuit. Because there must be some delay time for the drive signal sent to the drive circuit until the switches are turned on, the parameters must be correctly designed to make sure that the delay time is less than t_{delay} to make the switches work in the ZVS state.

At time t_4, S_1 is turned off and the next cycle begins. The inductor current at this moment can be described by the following:

$$i(t_4) = i(t_0) = \frac{V_g}{Z_r}\left[\theta_4(1-M) - \sqrt{2M-1}\right]. \tag{14}$$

Fig. 6. Conversion-ratio characteristic of buck quasi-square-wave converter.

As described above, $\theta 1$ is very small, and can be neglected in this analysis. The equation can be obtained as follows:

$$i(t_4) = i(t_1) \rightarrow \frac{V_0\theta_2}{Z_r} = \frac{V_g}{Z_r}\left[\theta_4(1-M) - M\sin\theta_3\right] = I_{\max}. \tag{15}$$

Here we define the maximum inductor current $I_{\max}$ and the average output current I_0. Then the equations can be obtained as follows:

$$I_0 = \frac{V_0 - V_g/2}{R} = \frac{V_0 - V_g/2}{Q_p Z_r} = \frac{I_{\max} + I_{\min}}{2} \tag{16}$$

$$I_{\max} = 2I_0 - I_{\min} = 2 \times \frac{V_0 - V_g/2}{Q_p Z_r} + \frac{V_0}{Z_r}. \tag{17}$$

With (14) and (17), we can get:

$$\theta_4 = \frac{1}{1-M}\left[\frac{2}{Q_p}(M - \frac{1}{2}) + M + \sqrt{2M-1}\right]. \tag{18}$$

Here t_{on} is defined as the turn-on time of the switch, then:

$$\theta_4 = \omega_0(t_4 - t_3) = \omega_r t_{on}. \tag{19}$$

Here u is defined as the voltage gain of the converter, then:

$$u = \frac{V_{lamp}}{V_g} = \frac{V_0 - V_g/2}{V_g} = M - \frac{1}{2}. \tag{20}$$

With (18), (19) and (20), the output voltage gain can be described as follows:

$$u = \left[\frac{-1 + \sqrt{1 - 1 \times \left(\frac{2}{Q_p} + 1 + \omega_r t_{on}\right) \times (1 - \omega_r t_{on})}}{\left(\frac{2}{Q_p} + 1 + \omega_r t_{on}\right)}\right]^2 \Big/ 2. \tag{21}$$

Fig.6 shows the voltage gain characteristic of the ZVS-QSW converter. It is obvious that, when the load is constant, the voltage gain is one-to-one mapping with t_{on}, the output voltage increase with t_{on}, and when t_{on} is constant, the voltage gain changes with t_{on}. Therefore, it is reasonable to control t_{on} to change the working conditions of the converter.

Fig.7 shows the equivalent circuits for mode2 in one high frequency cycle. Mode1 and mode2 work alternately with a low frequency, then the low frequency square waveform can be obtained. As can be seen in the circuit, the working principle of mode2 is the same as mode1. Therefore, mode2 is not analyzed in detail in this paper.

IV. ADAPTIVE ZVS CONTROL

Fig.8 is the test circuit which is used to test the ZVS state of the converter. In the positive buck circuit, S_1 is not connected to the power ground, so the voltage of $VD_1$is tested indirectly to reflect the voltage between the drain pole and the source pole of S_1. In the period $t2 \sim t3$, the voltage $V(t)$decreases from the bus voltage, and because the bus voltage is constant, the voltage of VD_1 will increase from zero to the bus voltage. In Fig.8, the voltage of (a) point is sampled by the MCU, and its rising edge is tested by the MCU. The voltage of S_2 can be directly sampled since the drain pole of S_2 is connected to the power ground. The falling edge of the voltage between the

Fig. 7. Equivalent circuits for mode2 in one high frequency cycle.

Fig. 8. Voltage sampling circuit.

Fig. 9. PWM modified by edge retrigger signal.

drain pole and the source pole of S_2 is also tested by the MCU. In the converter, the voltage of VD_1 and S_1 both range from 0V to the bus voltage, and the maximum voltage that the I/O pins of the MCU chosen here can afford is 5.5V. As a result, the parameters are chosen as follows: $R_1 = R_3 = 330\text{k}\Omega$, $R_2 = R_4 = 4.7k\Omega$, $C_1 = C_2 = 20\text{pF}$.

A chip microprocessor AT90PWM2 produced by ATMEL was chosen. It has a module called a PSC whose clock frequency is as high as 64MHz. It still has a very high distinguishing ability when the PWM signal frequency reaches 100 kHz. It also has many triggering functions which can be used to do zero cross detection and processing failure checking. Here we use its edge control function to realize the ZVS for the converter. Just as Fig.9 shows, when there is no triggering signal, the MCU sends the PWM signal as usual, but when the trigging signal comes, the MCU can amend the PWM signal to make a high level come in advance. In practical use, when the voltage between the drain pole and the source pole of the switches for a ZVS-QSW converter comes to zero, the test circuit will send the message to the MCU, and the MCU will pause the current period, and send the PWM signal for the drive circuit in next cycle to make the switches turn on before the inductor current reaches zero oppositely.

V. One cycle peak current control

In the transition stage, because the lamp voltage is very low and the lamp current is very high, the inductor voltage is much higher than it is in the steady state. If the peak circuital current is very high, then some control theory for constant current control or limiting current must be used. In addition, the ZVS-QSW converter adopted here can also cause a high peak current in the circuital loop when in the commutation time of the low working frequency. The voltage of L_1 or L_2 can vary from $V_g/2 - V_{lamp}$ to $V_g/2 + V_{lamp}$ or from $V_g/2 + V_{lamp}$ to $V_g/2 - V_{lamp}$. Therefore, the dV/dt of the inductor is very high which causes a high peak current. Especially, when the load is in the open-circuit state, the voltage of L_1 or L_2 varies from 0V to the bus voltage or from the bus voltage to 0V. If we do not control the turn-on time of the converter to limit the peak current, the peak current will be even higher. Paper [15] proposes one control method to limit the over-

Fig. 10. Modified waveform of IR2104_IN control signal.

Fig. 11. Control circuit used to limit peak current of inductor.

current for commutation of the low frequency, but it is too complicated and does not have comprehensive flexibility. This paper proposes a control method to limit the peak current in the whole working condition of the ballast, which has a simple circuit and a fast response. Fig.10 is the modified waveform of an IR2104_IN control signal and Fig.11 is the control circuit of the converter to limit the peak current. When the inductor current has reached the amplitude limiting value, the MCU will get an interrupt signal. Then the MCU will pause the high level control signal for the drive circuit, so that the switch will be turned off to limit the peak current of the circuital loop.

Fig.11 shows a circuit diagram for the one-cycle peak-current limit. Here we use an IRS2104 to drive S_1 and S_2. In one high frequency cycle, the inductor voltage can be seen as constant, and the variable ratio of the inductor current is approximately constant as well. Here, we define the inductor current of L_1 as $i(t)$ and the voltage of L_1 as U_1, so that the voltage of the secondary side for L_1 is U_1/n, and $u_2(t)$ is the voltage between (b) point and the control ground. Then the equation can be obtained $u_2(t) = U_1(1 - e^{-t/RC})/n$, $i(t) = U_1 t/L_1$, so that it is obvious that the voltage $u_2(t)$ has one-to-one mapping with the inductor current. Here we can just sample the voltage of the secondary side, and when the voltage between (b) point and the control ground is higher than the amplitude limiting voltage, we turn off the corresponding switch, and the peak current can be limited.

Fig. 12. Turn on time vs lamp power when lamp impendence is constant.

Fig. 13. Lamp impendence vs turn on time when lamp power is constant.

VI. Closed Loop Control

From (21), the lamp power can be calculated.

$$P_{lamp} = V_g^2 \times \left[\frac{-1 + \sqrt{1 - 1 \times \left(\frac{2}{Q_p} + 1 + \omega_r t_{on}\right) \times (1 - \omega_r t_{on})}}{\left(\frac{2}{Q_p} + 1 + \omega_r t_{on}\right)} \right]^4 \Big/ (4 \times R_{lamp}). \tag{22}$$

For the 70W HID lamp used here, the lamp voltage $V_{lamp} =$ 100V, the lamp current $I_{lamp} = 0.7$A, and the equivalent impedance is 142Ω. Fig.12 shows the relationship between the lamp power in steady state and the turn-on time of the converter. It is obvious that if the equivalent impedance is constant in the steady state, the lamp power is linear with respect to the turn-on time. Therefore, it is reasonable to control the turn-on time to change the lamp power. Besides, the lamp impedance varies with the use time, and the lamp impedance used here varies from 80Ω to 160Ω. Fig.13 shows the relationship between the lamp impedance and the turn-on time in the steady state with full power. It is obvious that the lamp impedance is linear with respect to the turn-on time. Above all, the turn-on time can be used to control the lamp power.

Normally, there are two methods to reach the power loop. One is to multiply the lamp current by the voltage or to adopt approximate addition. However, this has a large amount of calculations and a relatively complicated circuit. Furthermore, with this method it is hard to reach consistency for different lamps. The other method is to control the average bus current to reach the power loop on the assumption that the losses of the inverter are constant. This method is very easy to

Fig. 14. Current of sampling resistance R_{sense} in mode1.

Fig. 15. Current of sampling resistance R_{sense} in mode2.

control, but when the losses of the inverter change with the working conditions of the circuit, it is hard to keep the lamp power constant. This paper presents a new method to reach the power loop with the prior condition that the output voltage of the PFC is constant. It can be seen in Fig.1 that R_{sense} is not used to sample the average bus voltage. Its current waveform in a high frequency cycle is shown in Fig.14 and Fig.15, and the reference direction is shown in fig.1. To analyze succinctly, here approximate linearization is done to the inductance current, as I_{L1} in Fig.14 and Fig.15.

In mode1, I_{sense} is the summation of I_{C2} and I_{VD1}, so that it is easy to get the average current of I_{sense} from the figure.

$$I_{Rense,avg-} = -I_{lamp}\frac{T_{off}}{T_s} = -I_{lamp}\frac{U_{dc}/2 - U_{lamp}}{U_{dc}}. \tag{23}$$

I_{lamp}—— average lamp current.
U_{lamp}——average lamp voltage.
U_{dc}——bus voltage.
T_s——period of the switches.
T_{off}——turn-off time of the switches.

In mode2, I_{sense} is the summation of I_{C2} and I_{s2}, and it is also easy to get the average current of I_{sense} from the figure.

$$I_{Rense,avg+} = I_{lamp}\frac{T_{on}}{T_s} = I_{lamp}\frac{U_{dc}/2 + U_{lamp}}{U_{dc}}. \tag{24}$$

T_{on}——on time of the switches.

Since the working time of mode1 and mode 2 are the same, it is easy to get the current of R_{sense} in the low frequency cycle.

$$I_{Rense,avg} = \frac{U_{lamp}I_{lamp}}{U_{dc}/4} = \frac{P_{lamp}}{U_{dc}/4}. \tag{25}$$

P_{lamp}——lamp power.

It is obvious that if the bus voltage is constant, the lamp power is constant, too.

TABLE I
PARAMETERS OF THE CONVERTER

Raged power	70W
High working frequency	100kHz∼200kHz
Low working frequency	150Hz
L_1, L_2	300uH
C_1, C_2	220nF
C_3, C_4	68nF
VD_1, VD_2	MURS160T3
S_1, S_2	SPD07N60C3
MCU	AT90PWM2

Fig. 16. Waveforms of drive signal, $V(t)$ and the current of L_1 in simulation.

VII. Simulation and Experimental Results

Fig.16 and Fig.17 show the simulation results of the converter. As can be seen in Fig.16, the green line is the current of L_1, the red line is the voltage between the drain pole and the source pole for S_1, and the blue line shows the drive signal of S_1. The duty cycle is 0.52, and it is obvious that, S_1 works in the ZVS state. In Fig.17, the green line is the lamp voltage while the red line is the lamp current, then the lamp works in the square-waveform mode.

A prototype was built in the laboratory. The parameters of the components used in the converter are shown in table I.

TABLE II
MEASURED RESULTS OF THE 70W PROTOTYPE WITH VARIOUS LAMPS

Lamp	Lamp voltage (V)	Lamp current (A)	Lamp power (W)
OSRAM HQI-E 70W/NDL	76.7	0.913	70
PHILIPS CDM-T 70W/830	83.1	0.841	69.8
PHILIPS CDM-TD 70W/830	85.2	0.822	70
PHILIPS CDM-R 70W/942 PAR30L	84.6	0.824	69.7
GE CMH70/TD/UVC/942	79.8	0.872	69.5
GE CMH70/T/UVC/942	84.1	0.831	69.88
PHILIPS MHC70/C/U/MP/3K	102.3	0.678	69.4

Fig. 17. Output voltage and current in simulation.

(a) Sampling signals of VD1.

(b) Sampling signals of S2.

Fig. 18. Sampling signals of VD1, S2 and input of IR2104_SD.

Fig.18 shows the sampling signals of VD_1 and S_2, and the dive signals from the IR2104 which is used to drive the switches of the converter. Fig.18 (a) shows that when the rising edge is tested, the PWM signal turns to a high level immediately, then the switch S_1 is turned on in the ZVS state. Fig.18 (b) shows that when the falling edge is tested, the PWM signal turns to a high level immediately, then the switch S_2 is turned on in the ZVS state.

Fig.19 shows the test waveforms of S_1 in the steady state. It is obvious that, when the current of L_1 reaches 0A, L_1

Fig. 19. ZVS of buck quasi-square-wave converter and inductor current.

resonates with C_{s1}. Then the voltage between the drain pole and the source pole of S_1 decreases to 0V. Then the drive signal comes, S_1 is turned on in the ZVS state, which proves the control theory.

Fig.20 shows the waveforms for the test circuit of the on-cycle-peak-current control, Fig.20 (a) shows the test results when in the open-circuit state, Fig.20 (b) shows the test results when in the transition state, and Fig.20 (c) shows the test results when in the steady state. It is obvious that when (b) point reaches the amplitude limiting value during the whole working condition, the PWM signal can be corrected immediately, and the peak current can be limited. This proves the correction of the proposed theory. Here 3.5A is chosen to be the amplitude limiting value.

As can be seen in Fig.21, the voltage of the center point is a square waveform, and the amplifier is $\frac{V_g}{2} \pm V_{lamp}$, which satisfies the analysis in this paper. I_{L1} only has a waveform in half of the low frequency cycle. The envelop waveform is shown in Fig.22. It can be seen in that figure that L1 is in the high working frequency mode in mode1.

Table II shows the test results for different kinds of lamps with the power-loop method proposed in this paper. It is obvious that the power-loop method for the ballast used here has favorable consistency.

The working condition from igniting to the steady state is shown as follows. Fig.23 (a) shows the igniting state. When the high voltage pulse comes, the lamp can be ignited immediately. Since the lamp equivalent impedance is very small, the lamp current and voltage are both very small. Fig.23 (b) shows the transition state waveforms of the lamp current and voltage. The lamp current and voltage increase along with an increase in the lamp equivalent impedance. In the steady state, as shown in Fig.23 (c), the lamp current and voltage are both low-frequency square waveforms. As can be seen in Fig.23 (c), the lamp voltage and current are not the same. The

(a) Open load state.

(b) Transition state.

(c) Steady state.

Fig. 20. Experimental results of peak current control strategy with one cycle control.

Fig. 21. The voltage V_0 and the current of L_1.

reason for this is that the lamp is no longer seen as a resistor in

Fig. 22. The envelope waveforms.

(a) Igniting state.

(b) Transition state.

(c) Steady state.

Fig. 23. Waveform of lamp voltage and lamp current.

the low-frequency square waveform mode. In the laboratory, there is no acoustic resonance phenomenon occurring. Fig.24 shows the prototype.

VIII. CONLCUSION

This paper proposes a digital control two-stage electronic ballast based on a ZVS-QSW converter. Through tests on a

Fig. 24. Prototype used in the lab.

prototype, it is observed that it can avoid acoustic resonance, and that the switches of the converter work in the ZVS state. It can also be seen that the efficiency is as high as 92%. Meanwhile, the one-cycle-peak-current control proposed here makes sure that the excessive current during the commutation period and the transition stage can be limited to a safe value for the converter. This improves the reliability of the system a lot. Tests with different lamps prove the correction of the closed-loop method proposed here.

REFERENCES

[1] J. Garcia-Garcia, J. Cardesin, J. Ribas, A.J. Calleja, E.L. Corominas, M. Rico-Secades, J. M. Alonso, "Using high frequency current square waveforms to avoid acoustic resonances in low wattage metal halide lamps," *in Proceedings of IEEE Power Electronics Specialists Conference*, pp. 2799–2804, Jun. 2004.

[2] J. Garcia, J. Cardesin, J.M. Alonso, J. Riba, A. Calleja, "New HF square-waveform ballast for low wattage metal halide lamps free of acoustic resonances," *in Proceedings of IEEE Industry Applications Conference*, pp.655–662, Oct. 2004.

[3] Tiago B. Marchesan, Douglas Pappis, Murilo Cervi, Alexandre Campos, Ricardo Nederson do Prado, "An electronic ballast to supply automotive HID lamps in a low frequency square waveform," *in Proceeding of IEEE Industry Applications Society Conference*, pp. 1598–1602, Oct. 2005.

[4] R. Osorio, M. Ponce, M. A. Oliver, "Analysis and design of a dimming control using sliding mode control strategy for electronic ballast free of acoustic resonances," *in Proceeding of IEEE Applied Power Electronics Conference and Exposition*, pp.159˜163, Feb. 2004.

[5] C.R. Lee, K.H. Chen, C.S. Moo, "Operating characteristics of small-wattage metal halide lamps with square wave current from 50Hz to 50kHz," *in Proceeding of IEEE Industry Applications Conference*, pp. 1030–1035, Oct. 2003.

[6] Hua Li, Miaosen Shen, Zhaoming Qian, "A novel low frequency electronic ballast for HID lamps," *in Proceeding of IEEE Industry Applications Conference*, pp. 668–673, Oct. 2004.

[7] X. Cao, W. Yan, S.Y.R. Hui, H. Chung, "Lamp arc resistance modeling of high-intensity-discharge (HID) lamps," *Proceeding of the IEE Measurement and Technology*, Vol. 149, No. 1, pp. 45-48, Jan. 2002.

[8] Jianqiang Wang, Dianguo Xu, Hua Yang, "Low-frequency sine wave modulation of 250W high-frequency metal halide lamp ballasts," *in Proceedings of IEEE Applied Power Electronics Conference and Exposition*, pp.1003-1007, Feb. 2004.

[9] Ray-Lee Lin, Zhi-Qiang Wang, Yan-Der Lee, Feng-Yin Chen, "2.65-MHz self-oscillating complementary electronic ballast with constant-lamp-current control for a metal halide lamp," *IEEE Trans. Power Electron*, Vol. 22, No. 6, pp. 2097-2105, Nov. 2007.

[10] Miaosen Shen, Zhaoming Qian, Fang Z Peng, "Design of a two-stage low-frequency square-wave electronic ballast for HID lamps," *IEEE Transactions on Industry Application*, Vol. 39, No. 2, pp. 424-430, Mar. 2003.

[11] Jun Zhao, Miaosen Shen, Min Chen, "A noval low-frequency square wave electronic ballast for low-wattage HID lamps," *Industry Applications Conference*, pp.321˜324, Oct. 2003.

[12] Hiralal M. Suryawanshi, Vijay B. Borghate, Manojkumar R. Ramteke, Krishna L. Thakre, "Electronic ballast using a symmetrical half-bridge inverter operating at unity-power-factor and high efficiency," *Journal of Power Electronics*, Vol. 6, No. 4, pp.330–339, Oct. 2006.

[13] Li H, Shen M, Jiang Y, "A novel low-frequency electronic ballast for HID lamps," *IEEE Trans. On Industry Applications*, Vol. 41, No. 5, pp. 1401-1408, Oct. 2005.

[14] Majid Dehghani, Seid Mortaza Saghaiannejad, Hamid Reza Karshenas, "Electronic ballast for HPS lamps with intrinsic power regulation over lamp life," *Journal of Power Electronics*, Vol. 9, No. 4, pp.526–534, Jul. 2009.

[15] Jianbing Xu, Min Chen, Zhaoming Qian, "New control strategy for a two-stage low-frequency square-wave electronic ballast for MHD lamp," *in Proceeding of IEEE Applied Power Electronics Conference and Exposition*, pp. 1028–1032, Mar. 2006.

Yijie Wang was born in Heilongjiang Province, China, in 1982. He received his B.S. and M.S. in Electrical Engineering from Harbin Institute of Technology, China, in 2005 and 2007, respectively, where he is currently pursuing his Ph.D. His interests include DC-DC converters, soft-switching power converters, power factor correction circuits, digital control of electronic ballasts, and LED lighting systems.

Xiangjun Zhang was born in Shandong Province, China, in 1971. He received his B.S. from Xi'an Jiaotong University, Xian, China, in 1993, his M.S. from Harbin Welding Institute, Harbin, China, in 1999, and his Ph.D. in Electrical Engineering from Harbin Institute of Technology, Harbin, China, in 2006. Since 2004, he has been a Lecturer in the Department of Electrical and Electronics Engineering, Harbin Institute of Technology. His research interests are in the areas of electronic ballast, power factor correction circuits, high power converters, and LED lighting systems.

Wei Wang was born in Heilongjiang Province, China, in 1963. She received her B.S. in Automatic Test and Control from Harbin Institute of Technology, Harbin, China, in 1984, her M.S. in Electrical Engineering from Harbin Institute of Technology, Harbin, China, in 1990, and her Ph.D. in Mechanical Electronic Engineering from Harbin Institute of Technology in 2002. Since 2003, she has been a Professor with the Department of Electrical Engineering, Harbin Institute of Technology. She is engaged in research on soft-switching converters, digital control of electronic ballast, and regenerative energy converter techniques.

Dianguo Xu was born in Heilongjiang Province, China, in 1960. He received his B.S. in Control Engineering from Harbin Shipbuilding Engineering Institute, Harbin, China, in 1981, and his M.S. and Ph.D. in Electrical Engineering from Harbin Institute of Technology, Harbin, in 1984 and 1990, respectively. Since 1994, he has been a Professor with the Department of Electrical Engineering, Harbin Institute of Technology. His current research interests include robotics, lighting electronics, power quality mitigation, consumer electronics, power electronics, and motor drives. Dr. Xu is a member of the China Electrotechnical Society and the China Power Supply Society.