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Analysis and Design of a Soft-Switched PWM Sepic DC-DC Converter

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Abstract

This paper proposes a new soft-switched Sepic converter. It has low switching losses and low conduction losses due to its auxiliary communicated circuit and synchronous rectifier operation, respectively. Because of its positive and buck/boost-like DC voltage transfer function (M=D/(1-D)), the proposed converter is desirable for use in distributed power systems. The proposed converter has versions both with and without a transformer. The paper also suggests some design guidelines in terms of the power circuit and the control loop for the proposed converter.

Key Words: DC-DC Converter, Sepic Converter, Soft switching, ZVS (Zero Voltage Switching)

I. INTRODUCTION

In terms of converters with both buck and boost functions, there exist several converters such as basic the buck-boost converter and the Cuk, Zeta, and Sepic converters [1]–[8]. In other words these converters have in common the fact that their DC voltage transfer characteristics are equal to:

$$\frac{V_O}{V_i} = \frac{D}{1-D}$$

where V_i, V_O, and D are the DC input voltage, the DC output voltage and the duty cycle, respectively.

Among them the Sepic converter has the relatively good features that follow:

1) The polarities of the input and output voltage are the same from the same ground reference.
2) The input current riple is low due to the existence of large input inductor.
3) A version with a transformer exists so that the galvanic isolation between the input and output side is possible.

Thanks to these good characteristics, the Sepic converter seems to be a good candidate for the use in power factor correction, solar cell converters, fuel cell converters, etc.

Therefore, this paper proposes a new soft-switched Sepic converter. The proposed converter not only has low switching losses but also low conduction losses due to its zero voltage switching and its synchronous rectifier operation. Furthermore, thanks to the positive and buck/boost-like DC voltage transfer function (M=D/(1-D)), the proposed converter is desirable for use in distributed power systems. The proposed converter also has versions both with and without a transformer.

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II. PROPOSED ZVS PWM SEPIC DC-DC CONVERTER

A power stage circuit diagram of the proposed converter is shown in Fig. 1.

The circuit can be divided into two parts, that is, the hard-switched Sepic dc-dc converter and the auxiliary resonant commutated pole circuit [9]. The hard-switched Sepic dc-dc converter is the skeleton of the proposed converter. Fig. 1 includes a MOSFET switch S_2 only to achieve synchronous rectification, but not for a backward power flow like a Zeta converter. The main switches S_1 and S_2 switch on and off with the anti-parallel connected diodes D_1 and D_2, respectively, carrying out synchronous rectifier operation. The inductor current through L_1 and L_2 are positive for the forward power flow.

The auxiliary resonant commutated pole circuit (ARCPC) is composed of a small MOSFET Sa, and a resonant inductor L_r. The ARCPC circuit provides the hard-switched Sepic dc-dc

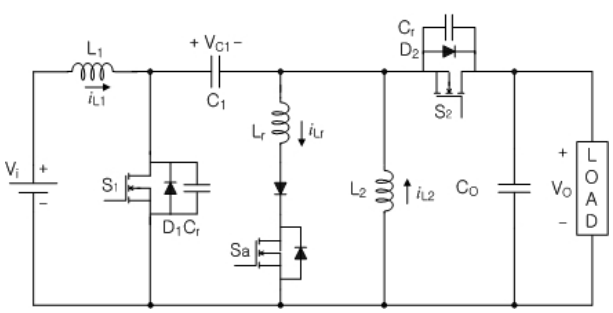

Fig. 1. Proposed ZVS PWM Sepic DC-DC converter.

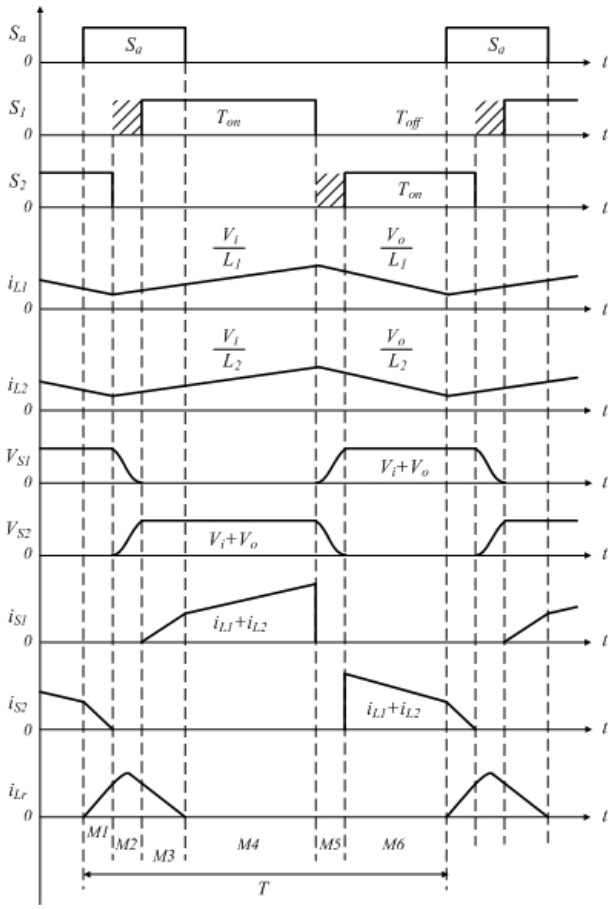

Fig. 2. Operating waveforms of the proposed converter.

converter with ZVS operation, and it is rated for a small power when compared with the output power. The ZVS operation for both the main MOSFET devices and the diodes results in improved circuit efficiency. Furthermore, since the ZVS switching occurs during a short time when compared to the switching period, it does not have a significant influence on the overall output characteristics of the basic DC/DC converter such as the PWM control and the linear input and output conversion characteristics.

The proposed converter has its operating waveforms as shown in Fig. 2.

When looking into the operation of the proposed converter in greater detail, its operation can be divided into 6 operation modes for one switching period, as shown in Fig. 3.

III. DESIGN OF THE PROPOSED ZVS PWM SEPIC DC-DC CONVERTER

In order to verify the effectiveness of the proposed converters and to suggest design guidelines for real applications, a prototype converter is properly designed with a rated power of 1.0[kW], a controlled output voltage of 100[V], an input voltage range of 40 60[V], and a switching frequency 40[kHz] above the acoustic noise frequency.

The proposed converter has an auxiliary resonant commutated pole circuit (ARCPC) composed of a small MOSFET S_a, and a resonant inductor L_r. However, the auxiliary circuit has little effect on the overall PWM operation characteristics

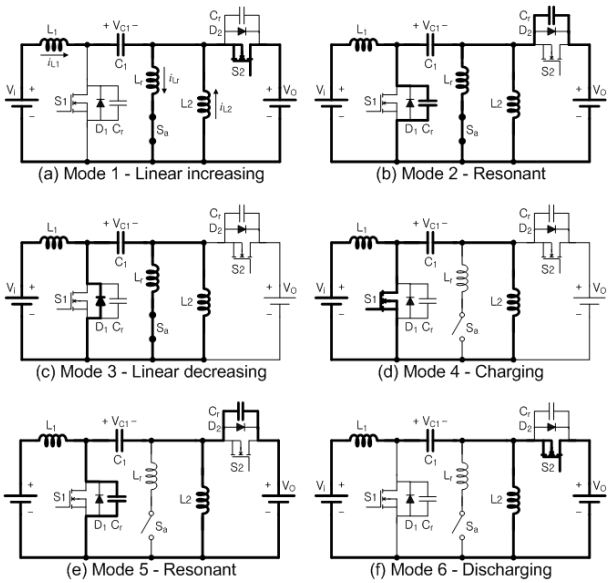

Fig. 3. Operating modes of the proposed converter.

of the hard switching PWM Sepic converter. Therefore, in the steady-state, the average values of the inductor voltages v_{L1} and v_{L2} are equal to zero, resulting in the following equation (1):

$$V_i = V_{C1}. \tag{1}$$

The voltage across the inductor L_2 during the on-state time T_{on} and the off-state time T_{off} of the switch S_1 is V_i and V_O, respectively. Since the flux increment of the inductor L_2 during the on-state time is equal to its flux decrement during the off-state time. Therefore, the following equation can be obtained:

$$dV_i = V_O(1-d). \tag{2}$$

Thus, the voltage conversion ration V_O/V_i of the proposed ZVS Sepic converter can be expressed as:

$$\frac{V_O}{V_i} = \frac{d}{1-d} \tag{3}$$

where the duty cycle d of the switch S_1 can be defined as $d = T_{on}/T$ where T_{on} and T are the on-state time and the switching period of the switch S_1, respectively.

In addition, as the steady-state power balance is satisfied:

$$V_i I_{L1} = V_O I_O. \tag{4}$$

Thus:

$$\frac{V_O}{V_i} = \frac{I_{L1}}{I_O}. \tag{5}$$

By combining equations (3) and (5), we can get the following equation (6):

$$\frac{I_{L1}}{I_O} = \frac{d}{1-d}. \tag{6}$$

On the other hand, when S_2 is in the on-state, the inductor currents I_{L1} and I_{L2} flow together through S_2 to the output side, and thus the following equation can be obtained:

$$I_O = (I_{L1} + I_{L2})(1-d). \tag{7}$$

From equations (6) and (7):

$$I_{L2} = \frac{1-d}{d} I_{L1} = I_O. \tag{8}$$

Since the input voltage ranges from 40[V] to 60[V] and the output voltage is to be controlled to 100[V], the variation range of the duty cycle d in the practical converter control is as follows:

$$0.63 < d < 0.71. \tag{9}$$

In this condition, the average current value $I_{L1.avg}$ through the inductor L_1 has its maximum value at $d = 0.71$, being expressed as:

$$I_{L2.avg} = \frac{1000[W]}{40[V]} = 25[A]. \tag{10}$$

By using the above derived equation (8), the maximum value of the average inductor current through L_2 is $I_{L2.avg} = 15[A]$. When considering a ripple factor of 25% in the inductor current through L_1 and L_2, the maximum current value $I_{s.max}$ of the switches S_1 and S_2 is given as:

$$I_{s.max} = 1.25(I_{L1.avg} + I_{L2.avg}) = 50[A]. \tag{11}$$

On the other hand, the switch voltage V_{S1} across S_1 is:

$$V_{S1} = V_i + V_O = 160[A]. \tag{12}$$

Thus, MOSFETs IXFN130N30 with a rated current of 130[A] and a rated voltage of 300[V] are selected for the experimental prototype by considering a design margin of 100%.

The current waveform through L_1 at a duty cycle d of 2/3 is shown in Fig. 4 and the peak-to-peak value ΔI_{L1} of the current ripple through L_1 is given as (13).

$$\Delta I_{L1} = \frac{V_i}{L_1} T_{on}. \tag{13}$$

When limiting the peak-to-peak current value ΔI_{L1} to within 25% of the rated current:

$$\Delta I_{L1} = \frac{50[V]}{L_1} \times 25[\mu sec] \times \frac{2}{3} = 25[A] \times 0.25. \tag{14}$$

Thus, by solving (14) and considering the design margin, the designed circuit parameter of the inductor L_1 is selected as 133[uH] with an average current of 25[A]. In addition, the circuit parameter of L_2 is also selected to be equal to that of L_1, but with an average current of 15[A]. The inductors should not be designed for the average current but for the peak current.

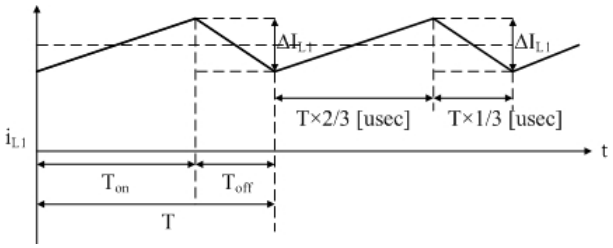

Fig. 4. Inductor current i_{L1} at d=2/3.

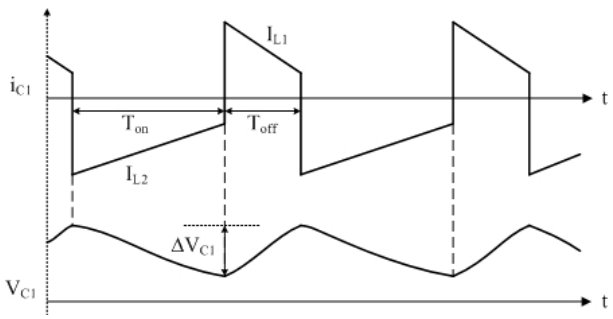

Fig. 5. Current waveform i_{C1} and voltage waveform V_{C1} of capacitor C_1.

When neglecting the circuit influence of the ARCPC, the voltage and current waveforms of C_1 are shown as Fig. 5 and the peak-to-peak voltage value ΔV_{C1} of capacitor C_1 can be given as (15).

$$\Delta V_{C1} = \frac{1}{C1} I_{L2} \times T_{on}. \tag{15}$$

To limit the peak-to-peak voltage value VC1 to within 25% of the input voltage, C_1 should be selected as a polypropylene capacitor of 40 [uF], 12 [Arms].

Fig. 6 shows the current waveform I_{S2} through the switch S_2 and the voltage waveform V_O across the output capacitor C_2. The peak-to-peak voltage value ΔV_O of the output capacitor C_2 is derived as (16).

$$\Delta V_O = \frac{1}{C_2}(I_{S2} - I_O)(T - T_{on}). \tag{16}$$

To limit the peak-to-peak value ΔV_O to within 1% of the predetermined output voltage, the output capacitor should be selected as C_2=470[uF].

The ripple current of the output capacitor C_2 can be calculated as (17).

$$I_{C2.ripple} = \sqrt{\frac{1}{T}\int_0^T i_{C2}^2 dt} = 17[A]. \tag{17}$$

Thus, the output capacitor C2 should be designed as 470 [uF], 17 [Arms].

To ensure ZVS operation of the switches S_1 and S_2, the auxiliary circuit parameters C_r and L_r of the ARCPC are

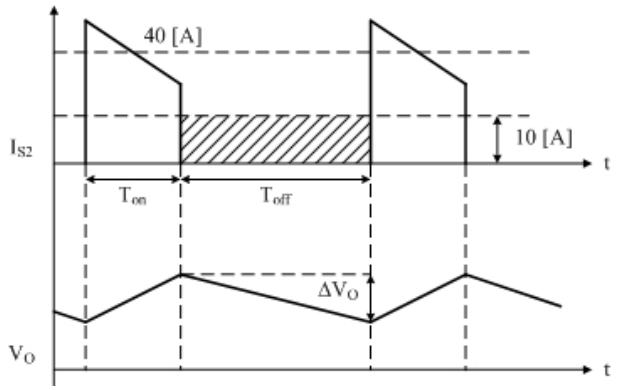

Fig. 6. Current waveform I_{S2} of MOSFET S_2 and voltage waveform V_O of capacitor C_2.

selected as 23.5 [nF] and 10 [uH], respectively, according to conventional design rules.

Upon turning on the auxiliary switch S_a the auxiliary inductor current i_{Lr} increases linearly with the rising slope of (18).

$$\frac{di_{Lr}}{dt} = \frac{V_O}{L_r} = \frac{100[V]}{10[\mu H]} = 10[A/\mu sec]. \tag{18}$$

When $i_{D2} = 40[A]$, the time interval Δt_1 of mode 1 is given as (19).

$$\Delta t_1 = \frac{40[A]}{20} = 2[\mu sec]. \tag{19}$$

On the other hand, the resonant period T_r of the auxiliary resonant parameters C_r and L_r is given as (20).

$$T_r = \frac{1}{f_r} = 2\pi\sqrt{L_r C_r}. \tag{20}$$

Thus, the time interval Δt_2 of mode 2 can be calculated as (21).

$$\Delta t_2 = \frac{T_r}{4} = 0.75[\mu sec]. \tag{21}$$

In addition, the rising increment Δi_{Lr} of the auxiliary inductor current i_{Lr} during mode 2 is equal to (22).

$$\Delta i_{Lr} = \frac{V_i + V_O}{\sqrt{\frac{L_r}{C_r}}} = \frac{160}{\sqrt{\frac{10[\mu H]}{23.5[\mu F]}}} = 7.75[A]. \tag{22}$$

At the beginning point t_3 of mode 3, the auxiliary inductor current i_{Lr} is equal to $i_{Lr}(t_3) = 45[A]$. It takes Δt_3 as (23) until the auxiliary inductor current i_{Lr} is reduced to zero.

$$\Delta t_3 = \frac{i_{Lr}(t_3)}{\frac{di_{Lr}}{dt}} = \frac{i_{Lr(t_3)}}{\frac{V_i}{L_r}} = \frac{45[A]}{60[V]/5[\mu F]} = 3.75[\mu sec]. \tag{23}$$

Switching timing diagrams of the main switches S_1, S_2. and the auxiliary switches S_a are shown as Fig. 7 to ensure the ZVS operation of the main switches and the ZCS operation of the auxiliary switches. The crossing point of the reference

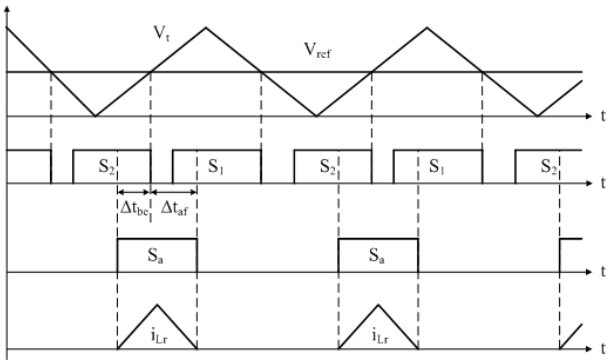

Fig. 7. Switching timing of switches S_a for ZVS Switching.

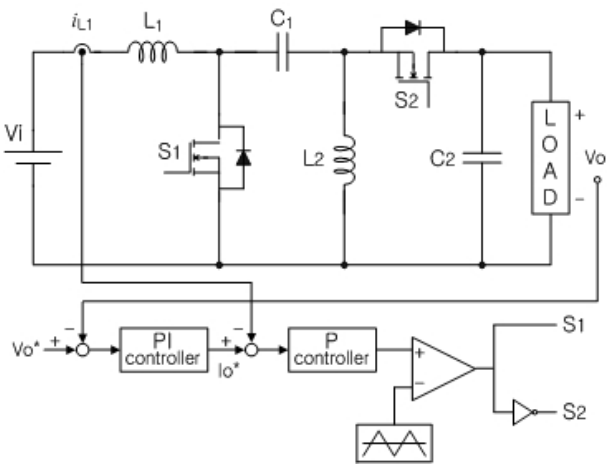

Fig. 8. Control block diagram of the proposed converter.

PWM signal and the triangular carrier is the criterion point to turn on and off the main and auxiliary switches.

As shown in Fig. 7, at the up slope of the triangular carrier, the auxiliary switch S_a is turned on Δt_{be} before the crossing point, thus increasing the stored energy in the auxiliary inductor. The stored inductor energy enables the ZVS turn-off operation of the switch S_2. After the resonant operation, it also enables the ZVS turn-on operation of the switch S_1.

Finally, after the stored energy is discharged to zero, the auxiliary switch S_a is turned off Δt_{af} after the crossing point. In the prototype, Δt_{be} and Δt_{af} are properly selected as 2[usec] and 4[usec] considering the time intervals $\Delta t_1, \Delta t_2, \Delta t_3$ of mode 1, 2, and 3.

IV. CONTROL LOOP DESIGN AND SIMULATION OF THE PWM SEPIC DC-DC CONVERTER

Fig. 8 shows an overall control block diagram of the proposed converter under the assumption that the auxiliary circuit has little effect on the overall PWM operation characteristics of the proposed PWM Sepic converter. The control block diagram consists of two feedback loops, that is, an inner current loop and an outer voltage loop.

The inductor current control loop as an inner control loop is composed of a P current controller, a PWM generator, a DC/DC converter, and an inductor L_1. It functions to control the inductor current I_{L1} and to generate the reference voltage

TABLE I
COMPONENT PARAMETERS FOR EXPERIMENTAL RESULTS

Power rating	1.0 [kW]	fs	40 [kHz]
V_1	40-60 [V]	V_2	100 [V]
C_1	40 [uF]	C_2	470 [uF]
L_1	133 [uH] 25 [A]	L_2	133 [uH] 15 [A]
MOSFET		IXYS IXFN130N30	

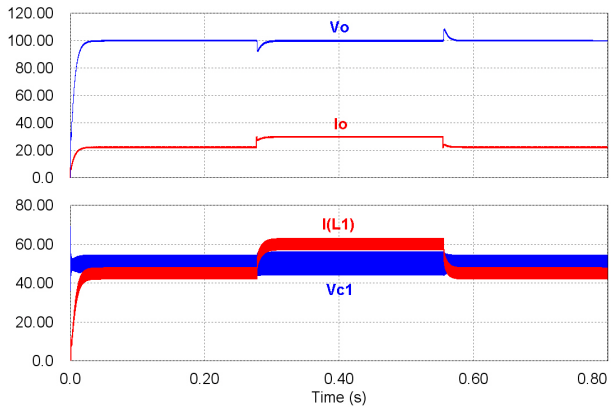

Fig. 9. The output voltage V_O and current I_O the inductor current $i_{L1}(t)$ and capacitor voltage $V_{C1}(t)$ when the load changes from 75% of the rated power to full power, and back to 75% of the rated power.

of the PWM generator which supplies the PWM gate signal to each MOSFET switch. Generally a P controller is enough to ensure the stability of the current loop of the inner loop and to improve the loop bandwidth, but an I controller is not necessary as the steady state error does not affect the system performance. The current reference is obtained from the voltage control loop of the outer loop.

On the other hand the output voltage loop as an outer control loop is to regulate the output voltage V_O and to generate the current command for the inner current loop. The voltage control loop is composed of a PI voltage controller, a current control loop, an output capacitor C_2, and a load. Generally a PI controller is utilized to ensure the stability of the outer voltage loop and to improve the loop bandwidth. In the case of the outer voltage control loop the I controller is necessary as the steady state error does affect the system performance.

In order to verify the operation of the proposed PWM Sepic dc-dc converter, a prototype converter was properly simulated with a rated power of 1.0[kW], an output voltage of 100[V] and an input voltage of 40 60[V]. Detailed converter ratings and circuit parameters are shown in TABLE I. The simulated converter is controlled through the PWM operation with a carrier frequency of 40[kHz].

An overall control block diagram of the proposed converter is shown in Fig. 8.

The upper graph of Fig. 9 shows the output voltage V_O and the current I_O when the load changes from 75% of the rated power to the rated power, and then back to 75% of the rated power. The lower graph of Fig. 9 shows the inductor current $i_{L1}(t)$ and the capacitor voltage $V_{C1}(t)$ under the same operation conditions. As shown in Fig. 9 the proposed converter operates very well with a low output voltage deviation.

Fig. 10 shows the output voltage V_O, the inductor current $i_{L1}(t)$ and the capacitor voltage $V_{C1}(t)$ when the input voltage

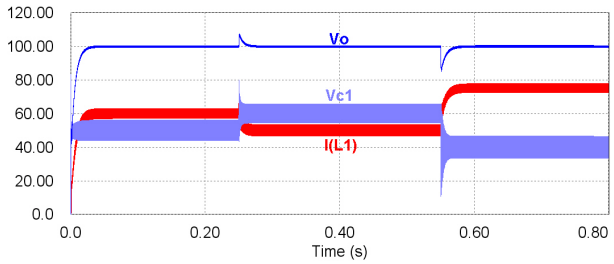

Fig. 10. The output voltage V_O, the inductor current $i_{L1}(t)$ and capacitor voltage $V_{C1}(t)$ when the input voltage changes from 50[V] to 60[V], and back to 40[V].

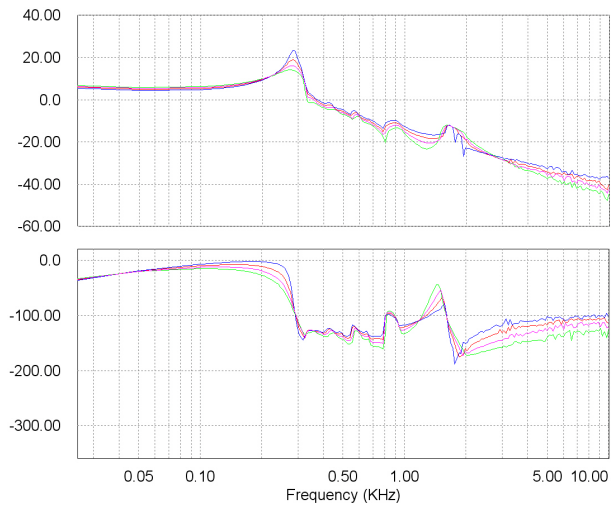

Fig. 11. The Bode plots of the inner current loop gain when the output load power vary from light load(25%) to full load(100%).

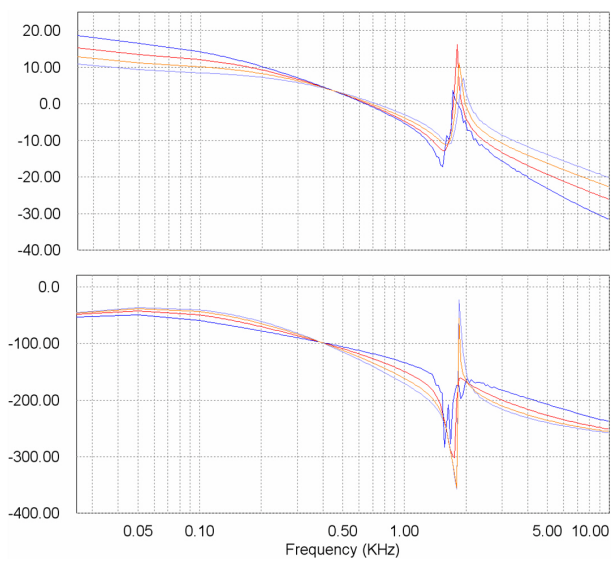

Fig. 12. The Bode plots of the outer voltage loop gain when the output load power vary from light load(25%) to full load(100%).

changes from 50[V] to 60[V], and then to 40[V]. It proves that the proposed converter operates very well under variations of the input voltage V_i.

Fig. 11 and Fig. 12 show the Bode plots of the inner current loop gain and the outer voltage loop gain, respectively when the output load power varies from light load to full load. The

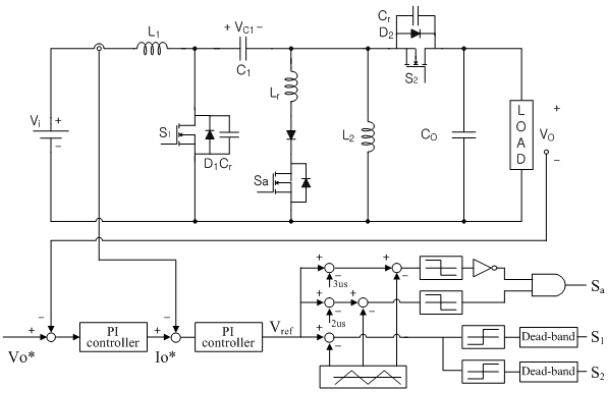

Fig. 13. Control block diagram of the proposed converter.

P controller and the PI controller were designed with the use of Bode plots according to the traditional method of control loop design.

V. EXPERIMENTAL RESULTS

In order to verify the operation of the proposed ZVS PWM Sepic dc-dc converter, a prototype converter was properly implemented with a rated power of 1.0[kW], an output voltage of 100[V] and an input voltage of 40 60[V]. The detailed converter ratings and circuit parameters are shown in TABLE I. The prototype converter is controlled through PWM operation with a carrier frequency of 40[kHz].

Fig. 13 shows an overall control block diagram of the proposed converter implemented with a DSP controller TMS320F2808. The control block diagram consists of two feedback loops, that is, an inner current loop and an outer voltage loop. The outer voltage loop is to regulate the output voltage V_O and to generate the current command for the inner current loop. The inner current loop is to control the inductor current and to generate the reference voltage of the PWM generator which supplies the PWM gate signal to each MOSFET switch.

Fig. 14 (a) shows the measured voltage V_{S1} and the current i_{S1} waveform of the switch S_1. Fig. 14 (b) and (c) show zoomed up waveforms during the turn-on interval and the turn-off interval, respectively. Fig. 15 (a) shows the measured voltage V_{S2} and the current i_{S2} waveform of the switch S_2. Fig. 15 (b) and (c) show zoomed up waveforms during the turn-on interval and the turn-off interval, respectively. They prove that the proposed converter achieves good ZVS by using the ARCPC circuit.

Fig. 16 shows the measured current waveforms i_{L1}, i_{L2} of the inductors L_1 and L_2. It shows that the proposed converter is very well controlled through the PWM method.

Fig. 17 shows the measured current i_{Lr} of the auxiliary resonant inductor L_r and the gate voltage $V_{GS}(S_a)$ of the auxiliary switch S_a. As shown in Fig. 17, the resonant inductor current increases above zero after turning on the auxiliary switch S_a, and then it returns to zero before turning it off. It proves that the auxiliary switch also achieves good ZCS operation.

Fig. 18 shows the measured efficiency of the proposed converter. It shows that the proposed converter has good

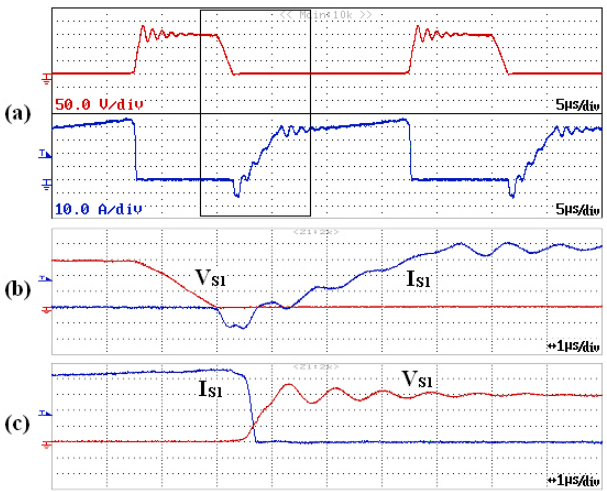

Fig. 14. (a) Voltage V_{S1} and current I_{S1} waveforms of switch S_1, (b) during turn-on interval, (c) during turn-off interval.

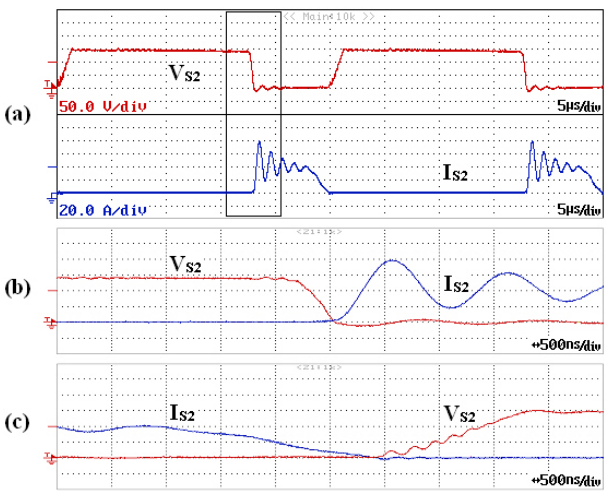

Fig. 15. (a) Voltage V_{S2} and current I_{S2} waveform of switch S_2, (b) during turn-on interval, (c) during turn-off interval.

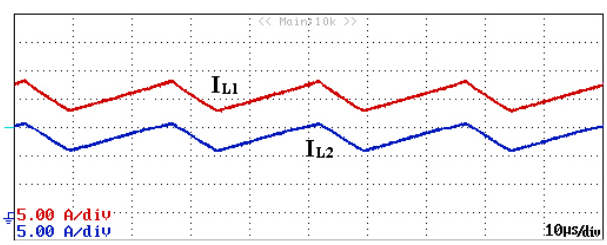

Fig. 16. Current waveforms i_{L1}, i_{L2} of inductors L_1 and L_2.

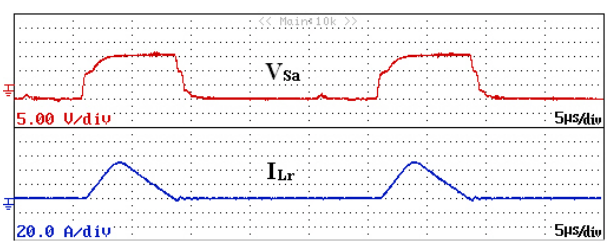

Fig. 17. Current i_{Lr} of auxiliary resonant inductor L_r and gate voltages $V_{GS}(S_a)$ of auxiliary switches S_a.

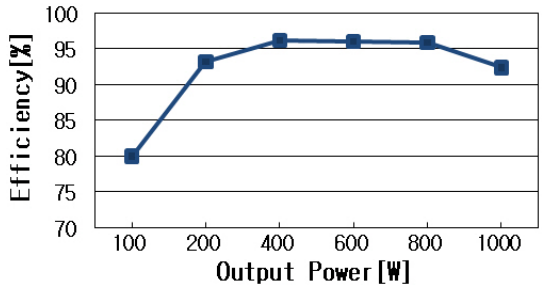

Fig. 18. The measured efficiency of the proposed converter.

efficiency.

VI. Conclusions

This paper proposes a new ZVS PWM Sepic dc-dc converter. The proposed converter not only has the capability of bilateral power flow, but it also has low switching losses and conduction losses due to its zero voltage switching and synchronous rectifier operation. Furthermore, thanks to the positive and buck/boost-like DC voltage transfer function (M=D/(1-D)), the proposed converter is desirable for use in distributed power systems, battery charger/dischargers, dc uninterruptible power supplies, etc. The paper also suggests some design guidelines for the power circuit and the control loop of the proposed converter.

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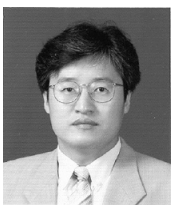

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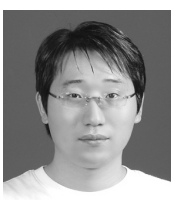

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