

# Quasi Resonant DC Link Inverter with a Simple Auxiliary Circuit

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## Abstract

In this paper, a new soft switching three phase inverter with a quasi-resonant dc-link is presented. The proposed inverter has a dc-link switch and an auxiliary switch. The inverter switches are turned on and off under zero voltage switching condition and all auxiliary circuit switches and diodes are also soft switched. The control utilizes PWM and the auxiliary switch does not require an isolated gate drive circuit. In this paper, the operation analysis and design considerations of the proposed soft switching inverter are discussed. The presented experimental results of a realized prototype confirm the theoretical analysis.

**Key Words:** Pulse Width Modulation (PWM), Quasi-resonant dc-link (QRDCL), Soft switching inverter, Zero Voltage Switching (ZVS)

## I. INTRODUCTION

Inverters have many applications in power electronic devices such as motor drives, active power filters and uninterruptible power supplies. In order to decrease the size of the output filter and to eliminate audio noise, the switching frequency must be increased. In hard switching inverters, a higher switching frequency leads to increased switching losses which consequently increases the size of the snubber circuits and heatsinks. In addition, electro magnetic interference (EMI) increases and efficiency decreases. To overcome these problems, the application of soft switching techniques is essential [1]–[10].

Quasi-resonant dc-link (QRDCL) inverters are one type of soft switching inverter that can be controlled by pulse width modulation (PWM) [11]–[19]. In these inverters, the input power supply is separated from the inverter dc-link by a switch, which is called a dc-link switch. Also, a resonant capacitor is placed in parallel with the inverter dc-link as shown in Fig. 1.

When a change in the state of the inverter switches is necessary, the dc-link switch is turned off and the resonant capacitor discharges by an auxiliary circuit and thus the state of the inverter switches can be changed under zero voltage switching (ZVS) condition. Then the auxiliary circuit charges the resonant capacitor and the dc-link switch is turned on again. The auxiliary circuit usually requires two or more switches in order to charge and discharge the dc-link capacitor.

One of the main QRDCL inverter research goals is to achieve soft switching conditions with a minimum number of

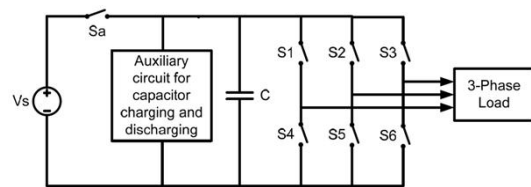


Fig. 1. A typical quasi-resonant dc-link inverter.

auxiliary circuit elements. The auxiliary circuit in [11] has three auxiliary switches and the auxiliary circuits in [12]–[16] have two auxiliary switches. Reducing the number of auxiliary switches simplifies the control circuit and decreases the inverter cost. Therefore it is essential to offer QRDCL inverters with one auxiliary switch [17], [18]. In [17] the number of auxiliary switches is reduced at the cost of employing extra elements including three diodes, coupled inductors and a resonant capacitor. The auxiliary circuit presented in [18] has reduced the number of extra elements at the expense of adding a capacitive voltage divider at the inverter input and losing control over the zero voltage interval of the inverter dc-link. The control of the dc-link zero voltage interval, is used in some switching methods such as space vector modulation. The QRDCL inverter presented in [19] has no auxiliary switch and the soft switching condition is achieved by a dc-link switch. This advantage is achieved at the cost of a higher voltage stress on dc-link switch.

In this paper a QRDCL inverter with one switch in its auxiliary circuit is presented. This switch is turned on under zero current switching (ZCS) condition and turned off under an almost ZVS condition. Also, the auxiliary diode in this circuit turns on under ZVS condition and turns off under ZCS condition. Since the source of the auxiliary switch is

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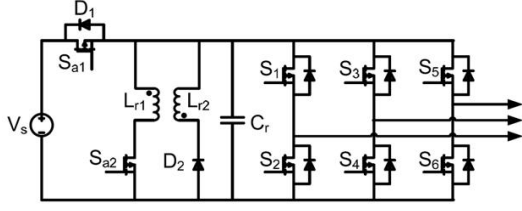


Fig. 2. Proposed QRDCL inverter.

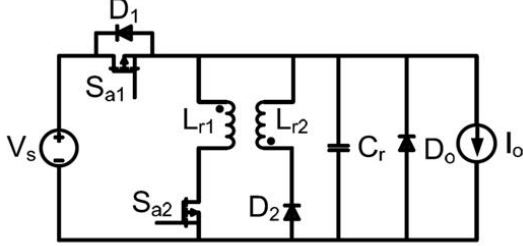


Fig. 3. Equivalent circuit of the proposed inverter.

connected to the source of three inverter main switches, this switch does not require an isolated gate drive circuit. The proposed inverter has a lower number of extra elements than previously developed QRDCL inverters.

The proposed inverter is introduced and its operating intervals are discussed in the second section. The design considerations of the proposed inverter are provided in the third section and the experimental results of a 250W, 20kHz prototype inverter are presented in the fourth section. The presented experimental results confirm the theoretical analysis.

## II. PROPOSED INVERTER OPERATION

The circuit configuration of the proposed QRDCL inverter is illustrated in Fig. 2. The main inverter is composed of  $S_1$  to  $S_6$ . The dc-link switch is  $S_{a1}$  and the dc-link resonant capacitor is  $C_r$ . The auxiliary circuit consists of switch  $S_{a2}$ , diode  $D_2$  and the coupled inductors  $L_{r1}$  and  $L_{r2}$ . Diode  $D_1$  is the anti-parallel diode of switch  $S_{a1}$ . Because the inductors  $L_{r1}$  and  $L_{r2}$  are much smaller than the load inductance, an inverter with a three phase load can be replaced by the current source  $I_o$ , as shown in Fig. 3.  $I_o$  is abruptly altered when the state of the inverter switches changes. Diode  $D_o$  stands for the anti-parallel diodes of the inverter switches. In order to simplify the description of the inverter operating intervals, all circuit elements are assumed to be ideal. The proposed inverter has seven distinct operating intervals in a switching cycle as shown in Fig. 4 and the main theoretical waveforms are presented in Fig. 5. Before the first operating interval, it is assumed that  $S_{a1}$  is on and  $S_{a2}$  is off. Therefore, the output current  $I_{o1}$  flows through  $S_{a1}$ .

**Interval 1** ( $t_0 \leq t \leq t_1$ ): Whenever a change in the state of the inverter main switches is desired,  $S_{a2}$  is turned on. Due to existence of  $L_{r1}$ , the turn on of  $S_{a2}$  is under ZCS condition and  $L_{r1}$  increases linearly until it reaches  $I_{min}$  which is defined as the minimum required current of  $L_{r1}$  that guarantees the charging of  $C_r$  in interval 4. The design procedure of  $I_{min}$  is illustrated in section III.  $L_{r1}$  and the duration of this interval

are as follows:

$$i_{Lr1}(t) = \frac{V_s}{L_{r1}}(t - t_0) \quad (1)$$

$$\Delta t_1 = t_1 - t_0 = \frac{L_{r1} I_{min}}{V_s}. \quad (2)$$

**Interval 2** ( $t_1 \leq t \leq t_2$ ): When  $L_{r1}$  reaches  $I_{min}$ , switch  $S_{a1}$  must be turned off.  $S_{a1}$  is turned off under ZVS condition due to the existence of  $C_r$ . In this interval, a resonance starts between  $C_r$  and  $L_{r1}$  which decreases the dc-link voltage. The  $L_{r1}$  and  $C_r$  equations are:

$$i_{Lr1}(t) = \frac{V_s}{Z_r} \sin(\omega_r(t - t_1)) + (I_{min} + I_{o1}) \cos(\omega_r(t - t_1)) - I_{o1} \quad (3)$$

$$v_{Cr}(t) = V_s \cos(\omega_r(t - t_1)) - Z_r(I_{min} + I_{o1}) \sin(\omega_r(t - t_1)) \quad (4)$$

where

$$\omega_r = \frac{1}{\sqrt{L_{r1} C_r}}, \quad Z_r = \sqrt{\frac{L_{r1}}{C_r}}. \quad (5)$$

When the dc-link voltage reaches zero, this interval ends. The duration of this interval is:

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_r} \tan^{-1}\left(\frac{V_s}{Z_r(I_{min} + I_{o1})}\right). \quad (6)$$

**Interval 3** ( $t_2 \leq t \leq t_3$ ): At  $t_2$ ,  $C_r$  reaches zero and diode  $D_2$  turns on. Thus, a fraction of the flux linkage of  $L_{r1}$ , moves to  $L_{r2}$ . At beginning of this interval  $L_{r1}$  is:

$$i_{Lr1}(t_2) = I_1 = \sqrt{\left(\frac{V_o}{Z_r}\right)^2 + (I_{min} + I_{o1})^2} - I_{o1}. \quad (7)$$

The ampere-turns of the coupled inductors must be constant, therefore:

$$N_1 I_1 = N_1 I_{Lr1} + N_2 I_{Lr2} \quad (8)$$

where  $I_{Lr1}$  and  $I_{Lr2}$  are the currents of  $L_{r1}$  and  $L_{r2}$ , and  $N_1$  and  $N_2$  are inductor winding turns of  $L_{r1}$  and  $L_{r2}$  respectively.

The dc-link voltage in this interval is  $(nV_{on,sw} - V_{on,d})/(n+1)$  where  $V_{on,sw}$  and  $V_{on,d}$  are the voltage drops of switch  $S_{a2}$  and diode  $D_2$ , and  $n = N_2/N_1$ . Since  $n$  is greater than unity, the dc-link voltage is small and positive which reverse biases the inverter anti-parallel diodes ( $D_o$ ). Thus:

$$I_{Lr2} = I_{Lr1} + I_{o1}. \quad (9)$$

By substituting equation (7) into equation (8) the following equations are obtained:

$$I_{Lr1} = \frac{I_1 - nI_{o1}}{n+1} \quad (10)$$

$$I_{Lr2} = \frac{I_1 + I_{o1}}{n+1}. \quad (11)$$

In order to operate at ZVS condition, the state of the inverter switches must be changed in this interval. In space vector modulation controllers this interval can be used as the zero vector.

**Interval 4** ( $t_3 \leq t \leq t_4$ ): At  $t_3$ , switch  $S_{a2}$  is turned off and the ampere-turns of  $L_{r1}$  move to  $L_{r2}$ . Thus,  $L_{r2}$  current increases and begins to charge  $C_r$ . Since the voltage of  $C_r$  is almost zero at the beginning of this interval, switch  $S_{a2}$  is turned off

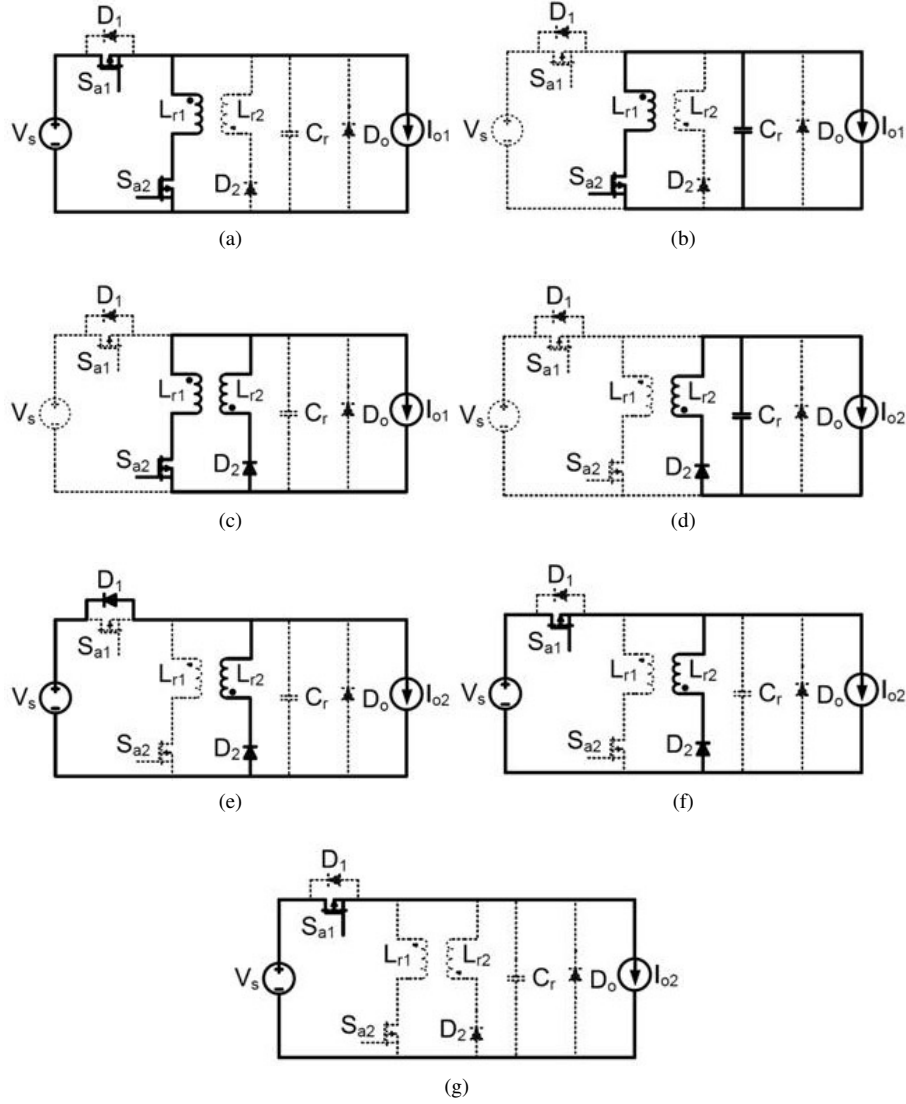


Fig. 4. Equivalent circuit of each operating interval.

under ZVS condition. Since the state of the inverter switches was changed in the previous interval,  $I_{o1}$  is changed to  $I_{o2}$ .  $L_{r2}$  and  $C_r$  in this interval are:

$$v_{Cr}(t) = Z_r(I_1 - nI_{o2}) \sin\left(\frac{\omega_r}{n}(t - t_3)\right) \quad (12)$$

$$i_{Lr2}(t) = \left(\frac{I_1}{n} - I_{o2}\right) \cos\left(\frac{\omega_r}{n}(t - t_3)\right) + I_{o2}. \quad (13)$$

When  $C_r$  reaches  $V_s$ , this interval ends. Thus, the duration of this interval is:

$$\Delta t_4 = t_4 - t_3 = \frac{n}{\omega_r} \sin^{-1}\left(\frac{V_s}{Z_r(I_1 - nI_{o2})}\right). \quad (14)$$

**Interval 5** ( $t_4 \leq t \leq t_5$ ): In this interval, diode  $D_1$  turns on under ZVS condition. Thus, switch  $S_{a1}$  can be turned on under zero voltage zero current switching (ZVZCS) condition.  $L_{r2}$  current decreases linearly from  $I_2$  to  $I_{o2}$ . Thus:

$$i_{Lr2}(t) = I_2 - \frac{V_s}{L_{r2}}(t - t_4) \quad (15)$$

where

$$I_2 = \frac{\sqrt{Z_r^2(I_1 - nI_{o2})^2 - V_s^2}}{nZ_r} + I_{o2}. \quad (16)$$

Duration of this interval is:

$$\Delta t_5 = t_5 - t_4 = \frac{L_{r2}(I_2 - I_{o2})}{V_s}. \quad (17)$$

**Interval 6** ( $t_5 \leq t \leq t_6$ ): This interval starts when  $D_1$  reaches zero and turns off under ZVZCS condition. Therefore  $S_{a1}$  begins to increase until it reaches  $I_{o2}$ . The current of  $L_{r2}$  is:

$$i_{Lr2}(t) = I_{o2} - \frac{V_s}{L_{r2}}(t - t_5). \quad (18)$$

This interval continues until  $L_{r2}$  current reaches zero. Therefore, the duration of this interval is:

$$\Delta t_6 = t_6 - t_5 = \frac{L_{r2}I_{o2}}{V_s}. \quad (19)$$

**Interval 7** ( $t_6 \leq t \leq t_7$ ): In this interval,  $I_{o2}$  flows through  $S_{a1}$ . This interval continues until the state of the inverter switches needs to be changed again.

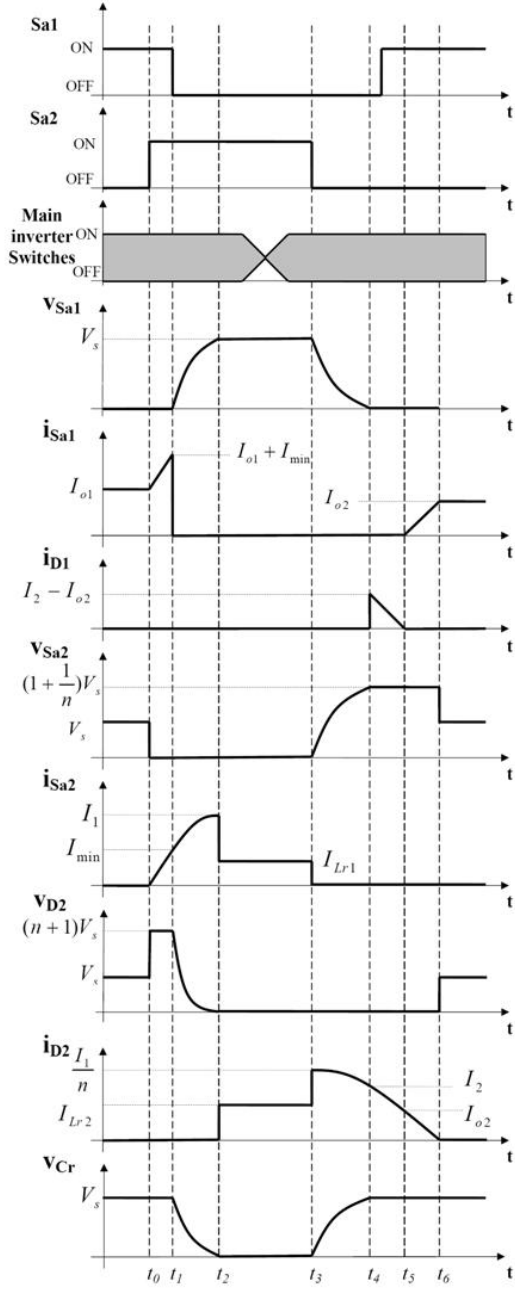


Fig. 5. Main theoretical waveforms of the proposed inverter.

### III. DESIGN CONSIDERATIONS

The design of the proposed inverter includes  $C_r$ ,  $L_{r1}$ ,  $n$  and the switch gate pulses.  $C_r$  is the turn off snubber capacitor for switch  $S_{a1}$  and  $L_{r1}$  is the turn on snubber inductor for switch  $S_{a2}$ . Therefore they can be designed like any conventional switch snubber [20].

The control circuit must drive the auxiliary switch and the dc-link switch at the proper time. It can be observed from Fig. 5 that when the control circuit decides to change the state of inverter switches, this action should be performed with a delay in order to have enough time to reduce the dc-link voltage to zero. Thus, switch  $S_{a2}$  is turned on first and  $L_{r1}$  current increases until it reaches  $I_{min}$ . This current must be large enough to guarantee charging  $C_r$  in interval 4. According

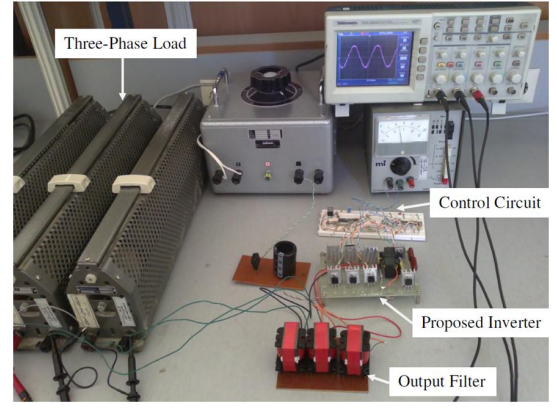


Fig. 6. Photograph of the prototype proposed inverter.



Fig. 7. Top: Sa1 voltage (50V/div), Bottom: Sa1 Current (4A/div), (time: 1μs/div).

to equation (12), to guarantee charging  $C_r$  to  $V_s$ , the following relation must be held:

$$Z_r(I_1 - nI_{o2}) \geq V_s. \quad (20)$$

By substituting  $I_1$  from equation (7) into relation (20), the following is obtained:

$$I_{min} \geq \sqrt{\left(\frac{V_s}{Z_r} + I_{o1} + nI_{o2}\right)^2 - \left(\frac{V_s}{Z_r}\right)^2} - I_{o1} \quad (21)$$

The right side of relation (21) is at its maximum when  $I_{o1} = I_{o2} = I_{om}$  where  $I_{om}$  is the maximum value of  $I_o$ . Thus the value of  $I_{min}$  which provides ZVS condition is obtained as follows:

$$I_{min} = \sqrt{\left(\frac{V_s}{Z_r} + (n+1)I_{om}\right)^2 - \left(\frac{V_s}{Z_r}\right)^2} - I_{om}. \quad (22)$$

To select a proper value for  $n$ , there is a tradeoff between  $I_{min}$  and the voltage stress of  $S_{a2}$ . According to (22), a larger  $n$  causes a larger  $I_{min}$  and thus greater current stresses on  $S_{a1}$  and  $S_{a2}$ . However a small value of  $n$  causes a higher voltage stress on  $S_{a2}$ . Therefore, a proper value for  $n$  is between 1.5 and 2.5. After determining  $n$ ,  $\Delta t_1$  can be obtained from equation (2).

The state of the inverter switches can be changed  $\Delta t_2$  seconds after turning  $S_{a1}$  off. According to equation (6), the maximum value of  $\Delta t_2$  is:

$$\Delta t_{2,max} = \frac{\pi}{2\omega_r}. \quad (23)$$



Fig. 8. Top: Sa2 voltage (50V/div), Bottom: Sa2 Current (2A/div), (time: 1 $\mu$ s/div).

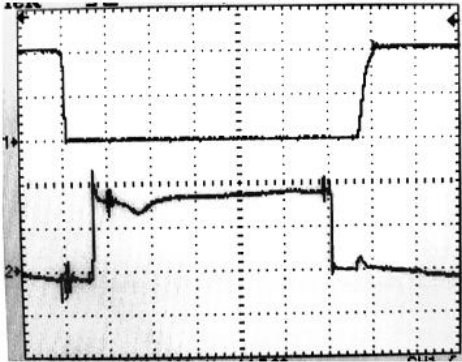


Fig. 9. Top: S1 voltage (50V/div), Bottom: S1 Current (2A/div), (time: 5 $\mu$ s/div).

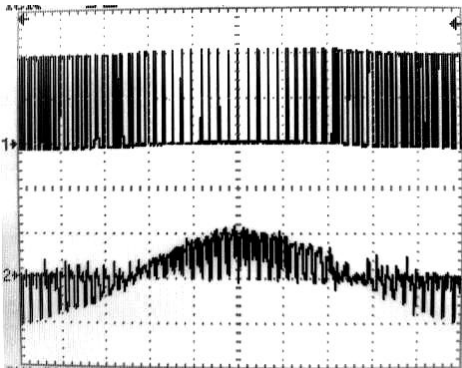


Fig. 10. Top: S1 voltage (50V/div), Bottom: S1 Current (5A/div), (time: 250 $\mu$ s/div).

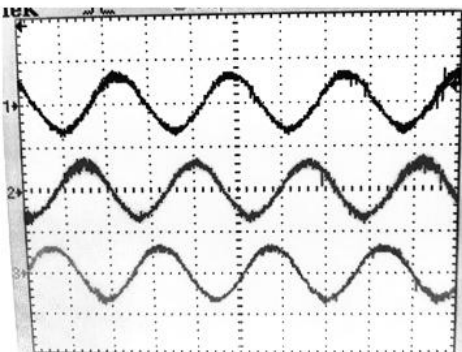


Fig. 11. Three phase output currents (10A/div), time: (1ms/div).

TABLE I  
INVERTER SPECIFICATIONS

Input StateDC voltage	$V_s$	100V
Switching frequency	$f_s$	20kHz
Output frequency	$f_o$	400Hz
Output Power	$P_o$	250W
Load power factor	PF	0.9
Modulation Index	$M_a$	0.8

TABLE II  
EMPLOYED COMPONENTS

Resonant capacitor	$C_r$	10nF
Resonant Inductor	$L_{r1}$	17 $\mu$ H
Coupled Inductors turns ratio	$n$	2
Switches	$S_{a1}, S_{a2}, S_1-S_6$	IRF640
Diode	$D_2$	MUR460

#### IV. EXPERIMENTAL RESULTS

A prototype of the proposed QRDCL inverter is implemented at a 20kHz switching frequency as shown in Fig. 6. The inverter specifications and the employed components are shown in Table I and Table II respectively.  $L_{r1}$  and  $L_{r2}$  are very small and are realized by winding 5 and 10 turns respectively on an EI2820 ferrite core using a small air gap.

The experimental results are illustrated in Fig. 7. The soft switching conditions of  $S_{a1}$  and  $S_{a2}$  are shown in Fig. 7 and Fig. 8 respectively. The voltage and current of one of the inverter main switches are shown in Fig. 9. It can be observed from this figure that the inverter main switches are turned on and off under ZVS conditions. The voltage and current of this switch in one cycle of output current is shown in Fig. 10. Also, Fig. 11 shows the inverter three phase output currents.

#### V. CONCLUSIONS

In this paper a new soft switching three phase inverter with a quasi-resonant dc-link is presented. This inverter has one auxiliary switch in addition to the conventional dc-link switch. In other words, it has a lower number of extra elements than previously presented QRDCL inverters. In addition, all auxiliary switches and diodes are soft switched. A theoretical analysis and the design considerations of the proposed inverter are presented. The presented experimental results of a prototype inverter confirm the theoretical analysis.

#### REFERENCES

- [1] M. D. Bellar, T. S. Wu, A. Tchamdjou, J. Mahdavi, and M. Ehsani, "A review of soft-switched DC-AC converters," IEEE Trans. on Ind. Applicat., Vol. 34, No. 4, pp. 847-860, Jul./Aug. 1998.
- [2] Y. Kawaguchi, E. Hiraki, T. Tanaka, and M. Nakaoka, "Basic study of a phase-shifted soft switching high-frequency inverter with boost PFC converter for induction heating," Journal of Power Electronics, Vol. 8, No. 2, pp.192-199, Apr. 2008.
- [3] T. Ahmed, S. Nagai, M. Nakaoka, and T. Tanaka, "Utility-interactive four-switch three-phase soft-switching inverter with single resonant DC-link snubber and boost chopper," Journal of Power Electronics, vol. 7, no. 2, pp.109-117, Apr. 2007.
- [4] M. R. Amini, and H. Farzanehfar, "Novel family of PWM soft-single-switched DC-DC converters with coupled inductors," IEEE Trans. on Industrial Electronics, Vol. 56, No. 6, pp. 2108-2114, Jun. 2009.
- [5] S. Nagai, S. Sato, and T. Matsumot, "Three-phase PWM inverter and rectifier with two-switch auxiliary resonant DC link snubber-assisted," Journal of Power Electronics, Vol. 5, No. 3, pp.233-239, Jul. 2005.

- [6] E. Adib, and H. Farzanehfard, "Family of isolated zero current transition PWM converters," *Journal of Power Electronics*, Vol. 9, No. 2, pp.156-163, Mar. 2009.
- [7] N. A. Ahmed, T. Iwai, H. Omori, H. W. Lee, and M. Nakaoka, "A novel auxiliary edge-resonant snubber- assisted soft switching PWM high frequency inverter with series capacitor compensated resonant load for consumer induction heating," *Journal of Power Electronics*, Vol. 6, No. 2, pp.95-103, Apr. 2006.
- [8] M. Mahdavi, and H. Farzanehfard, "A new zero voltage transition bridgeless PFC with reduced conduction losses," *Journal of Power Electronics*, vol. 9, no. 5, pp.708-717, Sep. 2009.
- [9] H. Iyomori, S. Nagai, M. Yoshida, E. Hiraki, and M. Nakaoka, "Power module bridge type auxiliary resonant AC link snubber-assisted three-phase soft switching inverter," *Journal of Power Electronics*, Vol. 4, No. 2, pp.77-86, Apr. 2004.
- [10] M. Kurokawa, C. Y. Inaba, M. Rukonuzzaman, E. Hiraki, Y. Konishi, and M. Nakaoka, "Feasible power loss analysis and estimation of auxiliary resonant DC link assisted soft-switching inverter with new zero voltage vector generation method," *Journal of Power Electronics*, vol. 2, no. 2, pp.77-87, Apr. 2002.
- [11] J. He, and N. Mohan, "Parallel resonant dc-link circuit-a novel zero switching loss topology with minimum voltage stresses," *IEEE Trans. on Power Electron.*, Vol. 6, No. 4, pp. 687-694, Oct. 1991.
- [12] Z. Y. Pan, and F. L. Luo, "Novel soft-switching inverter for brushless DC motor variable speed drive system," *IEEE Trans. on Power Electron.*, Vol. 19, No. 2, pp. 280-288, Mar. 2004.
- [13] M. Kurokawa, Y. Konishi, and M. Nakaoka, "Auxiliary resonant dc-link snubber assisted voltage-source soft switching inverter with space zero voltage vector generation method," in *IEE Proc. Elect. Power Appl.*, Vol. 149, No. 5, pp. 337-342, Sep. 2002.
- [14] Q. Li, J. Wu, and H. Jiang, "Design of parallel resonant dc-link soft-switching inverter based on DSP," in *proc. World Congress on Intelligent Control and Automation*, pp. 5595-5599, Jun. 2004.
- [15] Z. Y. Pan, and F. L. Luo, "Transformer based resonant dc-link inverter for brushless DC motor drive system," *IEEE Trans. on Power Electron.*, Vol. 20, No. 4, pp. 939-947, Jul. 2005.
- [16] H. Hucheng, D. Jingyi, C. Xiaosheng, and L. Weiguo, "Three-phase soft-switching PWM inverter for brushless DC motor," in *proc. IEEE Industrial Electronics and Applications*, pp. 3362-3365, May 2009.
- [17] Y. T. Chen, "A new quasi-parallel resonant dc-link for soft-switching PWM inverters," *IEEE Trans. on Power Electron.*, Vol. 13, No. 3, pp. 427-435, May 1998.
- [18] S. Mandrek, and P. J. Chrzan, "Quasi-resonant dc-link inverter with a reduced number of active elements," *IEEE Trans. on Ind. Electron.*, Vol. 54, No. 4, pp. 2088-2094, Aug 2007.
- [19] M. R. Amini and H. Farzanehfard, "Novel quasi-parallel resonant dc-link inverter with one auxiliary switch," in *proc. IEEE International Conference on Power and Energy*, pp. 614-618, Dec. 2008.
- [20] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics*, Third edition, John Wiley & Sons, 2003.



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