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A Digitally Controlled Three-Phase Cycloconverter Type High Frequency AC Link Inverter Using Space Vector Modulation

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Abstract

In this paper, a three phase cycloconverter type high frequency AC link inverter is discussed. The configuration consists of a high frequency full-bridge inverter and a high frequency transformer followed by a three phase cycloconverter whose switch is composed of anti-series connected MOSFETs with a common source. A simple digital control strategy based on space vector modulation (SVM) and repetitive control for the cycloconverter is proposed although its input voltage is a high frequency AC pulse. The operation principle of the proposed control strategy is analyzed and the equivalent working modes during one interval are also presented. The effectiveness of the proposed control strategy is verified through Matlab/Simulink simulations and experiments on a 1.45kW prototype.

Key Words: Cycloconverter, Digital control, High frequency link, Inverter, Space vector modulation

I. INTRODUCTION

A high frequency link (HF) inverter has many practical advantages when compared to a line frequency transformer isolated inverter in terms of power density, the size of the transformers, cost and other characteristics. Among these, a high-frequency transformer can satisfy the requirements of galvanic isolation and high power density. HF inverters can be divided into two categories. One is a high frequency inverter with a fixed DC link, and the other is a high frequency AC link inverter [1], [2]. The widely used high frequency fixed DC link inverter suffers from low reliability due to its bulky electrolytic capacitors. Another disadvantage of a HF DC link inverter is the lack of bidirectional flow capability, and therefore, an additional reactive power absorbing unit is necessary in the DC link.

A HF AC link inverter has attributes such as the elimination of bulky capacitors, bi-directional power flow capability without adding additional components, which results in improved conversion efficiency and reliability. HF AC link inverters can be classified into two categories. One is the rectifier-type HF AC Link (RHFACL) inverter, whose structure is similar to that of a conventional fixed DC link inverter except for the elimination of the DC link filter. The other is called a cycloconverter type HF AC link (CHFACL) inverter, which is characterized by placing a cycloconverter directly on the secondary side of a high frequency transformer [3]. Although a RHFACL inverter requires less switches, it has three stage power conversion, therefore, the conversion efficiency is lower than that of a CHFACL inverter. In addition, the generation of gate signals for the switches of a RHFACL inverter is more complex than that of a CHFACL inverter. Each switch of the cycloconverter should be bilateral, and thus it is required to conduct the ac current and block the ac voltage. Although anti-parallel SCRs can be used to form the bi-directional switches, the switching frequency is low and they are difficult to turn off [4], [5]. Fully controlled high-frequency power switching devices such as IGBTs and MOSFETs are widely used for this configuration. It is well known that MOSFETs are used more frequently in small power applications due to their higher switching frequency. Besides, it is also worth noting that MOSFETs have a special feature in their ability to work in quadrant III in which the current flows from the source to the drain.

A cycloconverter must be able to block voltages and currents in two directions. Hence, each bilateral switch can be composed of two anti-series or anti-parallel connected switches. Compared with the anti-series connection, the anti-parallel configuration requires a fast recovery diode to be series connected with each switch [6]. For IGBTs, the anti-series connection can be a common collector or a common emitter, while for MOSFETs, the connection can be a common source or a common drain. With a common collector or common drain connection, two separate driver circuits are needed for the bilateral switch [7], [8], while the common emitter or common source connection can share the same driver circuit [3], [9].

Most of the control strategies for a CHFACL inverter utilize

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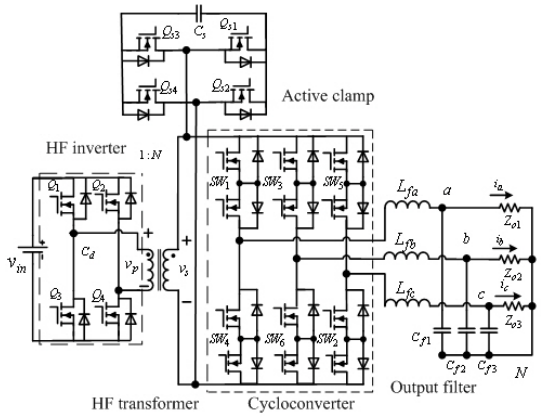


Fig. 1. High frequency AC link three-phase inverter.

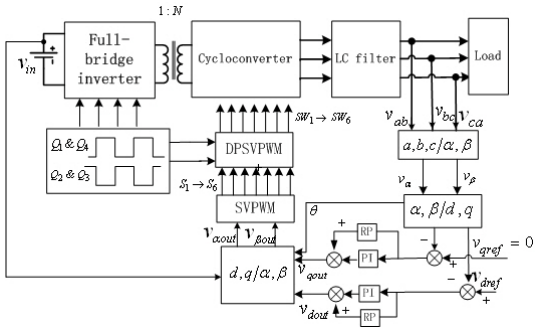


Fig. 2. Proposed digital control strategy.

carrier-based PWM [1]–[3], [8], [10], [11]. However, for a three-phase RHFACL inverter, space vector modulation (SVM) is widely used due to an almost fixed DC voltage input for three-phase conventional inverters [11], [12]. SVM has the advantages of low harmonics and a higher modulation index in addition to the feature of complete implementation with a digital signal processor [13], [14]. For a three phase controllable rectifier incorporating cycloconveters, although SVM can yield high quality input currents with an almost unity power factor [8], no papers have been published on a three phase CHFACL inverter using this control strategy.

This paper proposes a very simple digital control using SVM for a three phase CHFACL inverter although the input voltage for the cycloconverter is a HF AC pulse with a 50% duty cycle. The operation principle of the strategy is analyzed. A simulation analysis is also made to verify its effectiveness. In addition, a 1.45kW prototype is fabricated and experimentally evaluated.

This paper is organized as follows. The proposed digital control strategy is presented and analyzed in Section II. Simulation analysis is carried out in Section III. Experimental results of the prototype are illustrated in Section IV. Some conclusions are given in Section V.

II. DISCRETE PULSE SVM CONTROL STRATEGY

A. Operation principles of the proposed control strategy

Fig.1 shows the proposed three-phase HF AC link inverter, which consists of a high frequency inverter, a HF transformer, a three-phase cycloconverter and a three-phase LC filter. The high-frequency inverter consists of four N-type MOSFETs in a full bridge connection. The three-phase cycloconverter consists of six bi-directional switches SW_1-SW_6 in a three phase full bridge connection. The bidirectional switch configuration is composed of two N-type anti-series connected power MOSFETS with a common source. An active clamp circuit is added and in parallel with the input of the cycloconverter. The cycloconverter is similar to a three phase inverter, except for the input voltage. In a conventional three phase inverter, the input voltage is DC and stable while for the cycloconverter, the input voltage is a pulsating rectangle AC. For the cycloconverter, when the polarity of the secondary voltage v_s is positive, the gate signals for the cycloconverter switches are the same as those for a conventional three phase full bridge inverter. On the other hand, when the polarity is negative, the gate signals for the cycloconverter switches can be obtained by reversing the PWM signals for the three phase inverter. To achieve this, it is essential to know the polarity of the secondary voltages. Actually, it is difficult to sense a high frequency AC voltage with a high amplitudes due to the high switching noise. As seen from Fig.1, the variation of the polarity of the HF AC voltage v_s is synchronized with the gate signals for the HF inverter switches. Hence, according to the gate sequence for the HF inverter, it is easy to determine the variation of the polarity of the HF voltage v_s. The amplitude of the HF AC voltage can be obtained by the multiplication of the DC input voltage v_{in} and the transformer turns ratio N.

Fig.2 shows a diagram of the digital control strategy. With the control strategy, the three phase output line-to-line voltages are sampled, the Clark and Park transformations are applied to them and two phase decoupled and the time invariant outputs $v_d$and $v_q$are obtained. Because the desired outcome is to get three phase balanced AC output voltages with line frequency, the reference voltage for the q-axis should be zero, while the reference voltage for the d-axis is determined by the desirable output voltage amplitude. Since repetitive control (RC) is used for the PWM inverter, it can significantly reduce the output THD in the presence of uncertainties and disturbances. To decrease the THD of the output voltage under nonlinear loads [15], the voltage error of each axis is amplified by a hybrid compensator comprised of proportional integral (PI) control and RC, then we have two independent outputs $v_{dout}$and v_{qout}, which are applied to the inverse Park transformation. The outputs of this projection are $v_{\alpha out}$ and $v_{\beta out}$, which are the two components in the α,β stationary orthogonal reference frame, respectively. They also work as the inputs of the space vector PWM (SVPWM). Using the conventional SVPWM method, we obtain the six gate signals for a conventional three phase inverter with a stable DC voltage input. Based on these gate signals, as well as the gate sequence for the primary HF inverter, we obtain the gate sequence for the cycloconverter switches.

For a conventional three-phase inverter, there are eight voltage vectors $\vec{V}_0, \cdots \vec{V}_7$ corresponding to the eight switching states respectively, and this can be seen in Fig.3, wherein the voltage vector space is divided up into six sectors. Depending on the sector that the voltage reference is in, the two adjacent vectors are chosen. The binary representations of the two

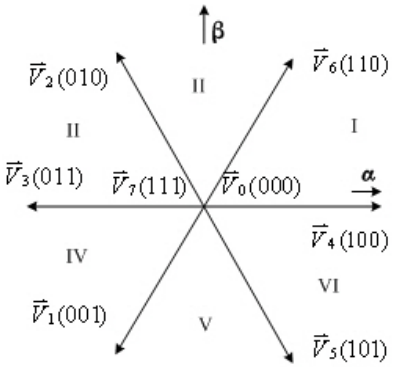


Fig. 3. Voltage vector space.

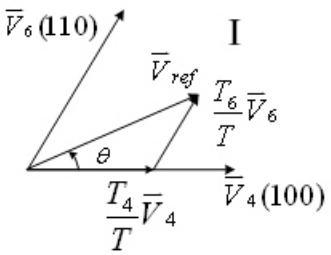


Fig. 4. Reference vector as combination of adjacent vectors in sector I.

adjacent basic vectors differ only by one bit, so that only one of the upper MOSFETs switches when the switching pattern moves from one vector to the adjacent one.

Supposing the reference voltage $\vec{V}_{ref}$ lies in sector I, as seen in Fig.4, where θ is the angle of the reference voltage. The two adjacent vectors are $\vec{V}_4$ and $\vec{V}_6$. T_4 and T_6 are the times during which the two vectors are applied, respectively.

$$\begin{cases} \vec{V}_{ref} = \frac{T_4}{T}\vec{V}_4 + \frac{T_6}{T}\vec{V}_6 \\ T = T_4 + T_6 + T_0 \end{cases} . \tag{1}$$

When the reference voltage and the sample periods are known, it is possible to determine the time durations T_4,$T_6$and T_0 according to (1), where T_0 is the zero vector application interval. The zero vectors can be $\vec{V}_0$ or $\vec{V}_7$. The seven-segment gate sequences S_1, S_3 and S_5, working as gate signals for the upper switches of a conventional three-phase inverter with a stable DC voltage input, can be seen in Fig.5.

In addition to the gate signals for a conventional three-phase inverter, the gate signals for a HF inverter are also illustrated. They are synchronized with the up counting or down counting periods of General Timer 1. The gate sequence for the upper switches of the cyloconverter can be obtained based on the following equation:

$$\begin{cases} SW_1 = S_1 \bullet Q_1 + Q_3 \bullet \bar{S}_1 \\ SW_3 = S_3 \bullet Q_1 + Q_3 \bullet \bar{S}_3 \\ SW_5 = S_5 \bullet Q_1 + Q_3 \bullet \bar{S}_5 \end{cases} . \tag{2}$$

Neglecting the dead time between the switches Q_1 and Q_4, we have:

$$Q_1 = \bar{Q}_3. \tag{3}$$

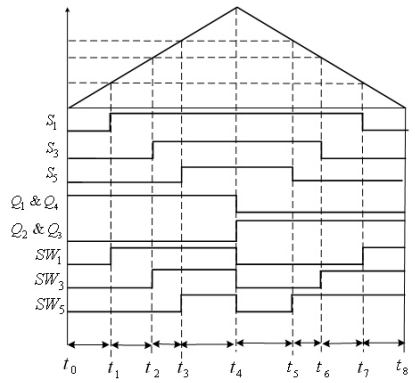


Fig. 5. Pattern of the DPSVPWM in sector I.

Based on (2) and (3), we can obtain:

$$\begin{cases} SW_1 = S_1 \oplus Q_1 \\ SW_3 = S_3 \oplus Q_1 \\ SW_5 = S_5 \oplus Q_1 \end{cases} . \tag{4}$$

From (4), we have the gate sequence for all of the upper switches of the cycloconverter, while the gate signal for the lower switch of each leg is complementary to that of the upper one in the same leg. In this way, we can obtain all of the gate signals for the cycloconverter switches.

To suppress voltage spikes across the cycloconverter switches, a full-bridge active clamp circuit is added and in parallel with the secondary winding of the HF transformer. The logic of the gating signals is as follows:

$$\begin{cases} Q_{S1} = Q_{S4} = Q_1 = Q_4 \\ Q_{S2} = Q_{S3} = Q_2 = Q_3 \end{cases} . \tag{5}$$

With the gating logic of the switches for the clamp circuit shown above, when the output voltage of the secondary voltage is positive, the clamp capacitor C_s is connected in the positive direction while it is connected reversely when the secondary voltage is negative.

As seen from Fig.5, four non-zero vectors are needed to form a reference vector with the proposed SVM strategy for a cycloconverter whose input is a HF AC voltage, and the switching frequency for the cycloconverter is two times that for the HF inverter.

Assuming the three-phase output line-to-neutral voltages balance, they can be expressed as follows:

$$\begin{cases} v_{aN} = \sqrt{2}V\cos(\omega t) \\ v_{bN} = \sqrt{2}V\cos\left(\omega t - \frac{2}{3}\pi\right) \\ v_{cN} = \sqrt{2}V\cos\left(\omega t - \frac{4}{3}\pi\right) \end{cases} . \tag{6}$$

Where V is the RMS value of each line to neutral output voltage. In order to establish a time invariant system model, the transformation of a three phase time variant system into a two phase time variant system is constructed first. The transformation can be described as:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{2/3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix}. \tag{7}$$

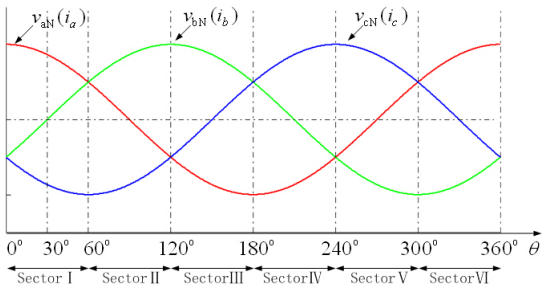


Fig. 6. Classification of six sectors according to θ.

Substituting (6) into (7) yields:

$$v_\alpha = \sqrt{3}V\cos(\omega t). \tag{8}$$

From (8), we conclude that v_α is in phase with $v_{\alpha N}$ after the general Clarke transformation.

B. Equivalent circuit mode analysis

To understand the operation principles of the inverter, an equivalent circuit mode analysis is carried out. Before the analysis, we assume that all of the components are ideal except for the body diodes of the MOSFETs. The voltage drops over the body diodes when they conduct can not be neglected.

The magnetizing inductance for the transformer is very large, thus the magnetizing current is so small that it can be ignored. Furthermore, for each output phase, the current through the filtering capacitor can be omitted when compared to its load current. Besides, we also assume that the loads are three-phase balanced resistors and thus the output voltage and the current of each phase are in phase. Assume that $\vec{V}_{ref}$ lies in sector I and that its angle in comparison with the α axis satisfies: $0^o < \theta < 30^o$. During this interval,$v_{aN} > 0$, $v_{bN} < 0$ and $v_{cN} < 0$, the instantaneous three output voltages and the currents can be observed from Fig.6 when $0^o < \theta < 30^o$. The detailed working modes of this interval are shown in Fig.7.

According to the sequence of the gating signals for the inverter, the mode analysis can be classified into eight modes. The time interval classification can be seen in Fig.5.

(1) Mode 1 [t_0-t_1]: At t_0, Q_1 and Q_4 are turned on, SW_1, SW_3 and SW_5 are off, the output three phase currents flow through SW_4, SW_6 and SW_2. The output power is supplied by the filtering inductors and capacitors.

(2) Mode 2 [t_1-t_2]: At t_1, SW_1 is turned on while SW_4 is turned off, the output three phase currents flow through SW_1, SW_6 and SW_2, and the input DC power is transferred to the secondary side through Q_1 and Q_4.

(3) Mode 3 [t_2-t_3]: At t_2, SW_3 is turned on and SW_5 is off, the output three phase currents flow through SW_1, SW_3 and SW_2, and the input DC power is still transferred to the secondary side through Q_1 and Q_4.

(4) Mode 4 [t_3-t_4]: At t_3, SW_5 is turned on and SW_2 is turned off, although Q_1 and Q_4 are gated on, the power transfer from the primary side to the secondary side is interrupted for the cycloconverter working in the zero state. The output three phase currents flow through SW_1, SW_3 and SW_5.

TABLE I
SYSTEM SPECIFICATIONS

Parameters	Values
Input StateDC voltage v_{in}	30V
Output line to line voltage (RMS)	380V
Rated resistor per phase R_o	100Ω
Transformer turns ratio 1:N	1:22
Switching frequency for the HF inverter	10kHz
Filtering inductor L_f	1mH
Filtering capacitor C_f	10μF

(5) Mode 5 [t_4-t_5]: At t_4, SW_1, SW_3, SW_5, Q_1 and Q_4 are turned off simultaneously while their individual complementary switches are turned on. The cylconconverter works in the zero state and no power is transferred from the primary side to the secondary side although Q_2 and Q_3 are gated on.

(6) Mode 6 [t_5-t_6]: At t_5, SW_5 is turned on while SW_2 is turned off. The DC power is transferred to the secondary side through Q_2 and Q_3 by magnetic coupling.

(7) Mode 7 [t_6-t_7]: At t_6, SW_3 is turned on while SW_6 is turned off. The DC power is still transferred to the secondary side through Q_2 and Q_3 by magnetic coupling.

(8) Mode 8 [t_7-t_8]: At t_7, SW_4 is turned off while SW_1 is turned on. The power transfer is interrupted and the cycloconverter works in the zero state.

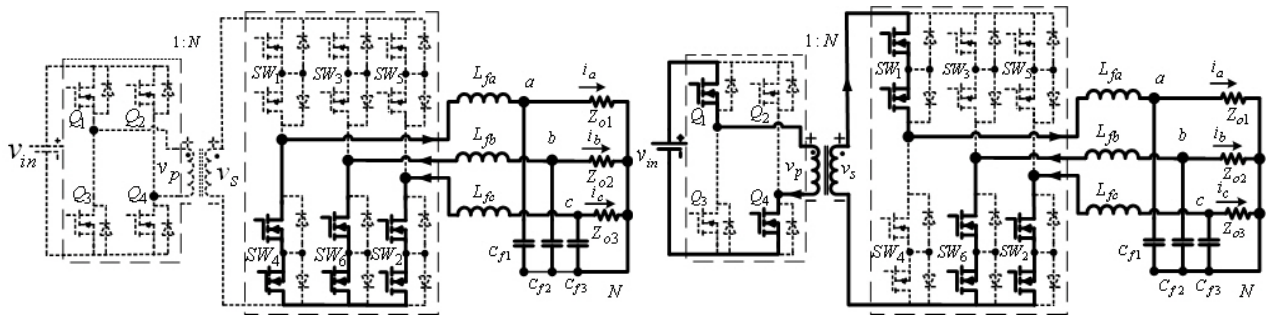
From the above mode analysis, at any time, no current flows through the body diodes of any of the cycloconverter switches. When the current conducts through one bilateral switch made up of two anti-series connected MOSFETs with a common source, one MOSFET works in quadrant I in which the current conducts from the drain to the source while the same current flows through the other MOSFET from the source to the drain. However, it should be noted here that the on-resistance of the other MOSFET has to be considered. In fact, the current flowing path is determined by a comparison between the voltage drop of its body diode and the voltage drop is obtained through a multiplication of the Rds(on) and the current.

III. Simulation Results

In this section, a MATLAB/Simulink model is developed to verify the proposed control strategy for a three-phase CHFACL inverter. The simulation parameters are shown in Table I.

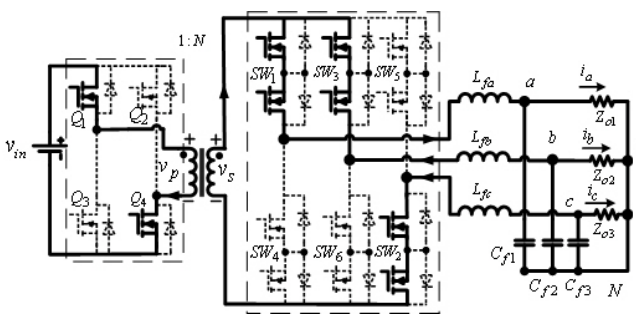
With the system specifications shown in Table I, the simulation results are shown in Fig.8 to Fig.10. Fig.8 shows the high frequency primary and secondary voltages. Both of them are HF AC rectangle waveforms with 50% duty cycles and are in phase simultaneously. Although their amplitudes are different, their ratio is the same as the transformer turns ratio. As for the primary current, it experiences a sudden change during each pulse. According to the mode analysis, the spike occurs at the time when mode 2 is transferring to mode 3 or mode 5 is transferring to mode 6. For instance, before the transient from mode 2 to mode 3, the transformer secondary current is actually iL_{fa}, but just after the transient, the current iL_{fb}flows through SW_3 instead of SW_6. Therefore, the transformer secondary current decreases suddenly just after the transition because it equals $iL_{fa} - iL_{fb}$.

Fig.9 shows the gate signals for some of the switches during Section I. As can be seen, the switching frequency of the cycloconverter is twice that of a high frequency inverter.

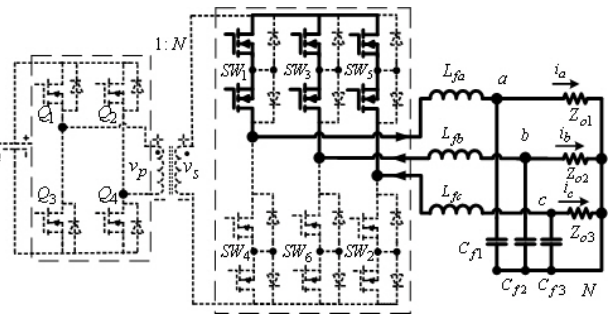


(a) Mode 1 ($t_0 < t < t_1$).

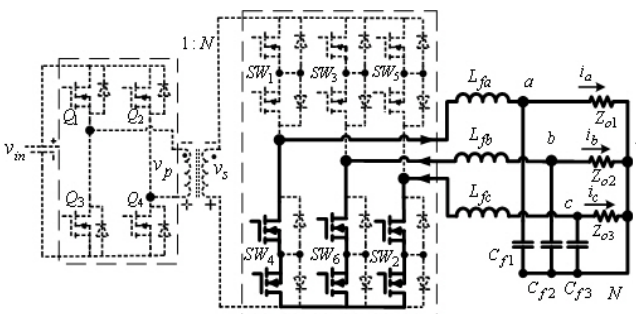
(b) Mode 2 ($t_1 < t < t_2$).



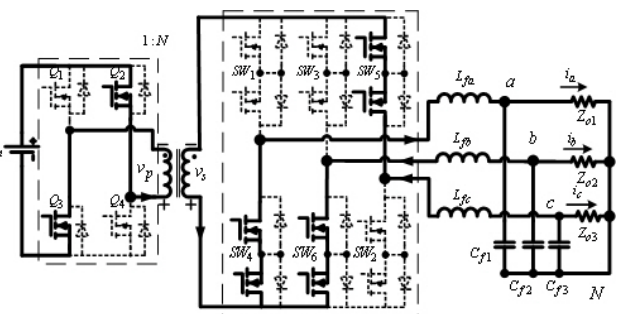
(c) Mode 3 ($t_2 < t < t_3$).



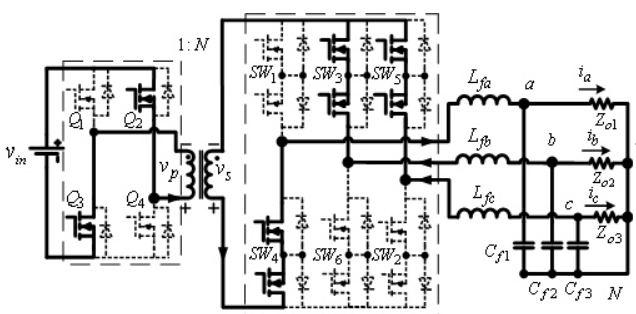
(d) Mode 4 ($t_3 < t < t_4$).



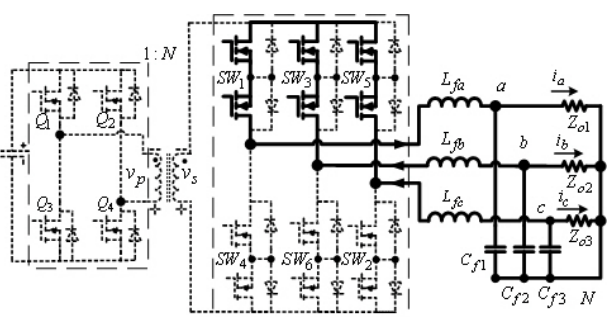
(e) Mode 5 ($t_4 < t < t_5$).



(f) Mode 6 ($t_5 < t < t_6$).



(g) Mode 7 ($t_6 < t < t_7$).



(h) Mode 8 ($t_7 < t < t_8$).

Fig. 7. Operation modes in sector I when $0^\circ < \theta < 30^\circ$.

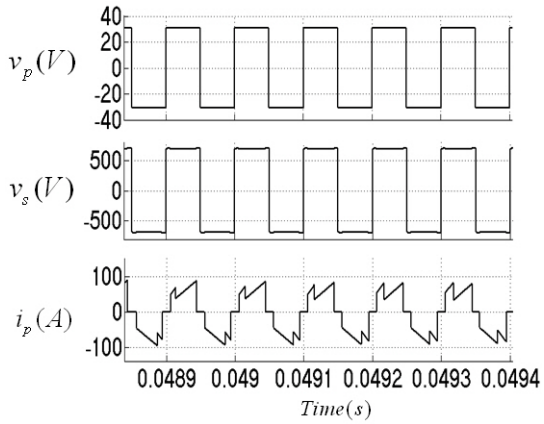


Fig. 8. Primary voltage ,current and secondary voltage.

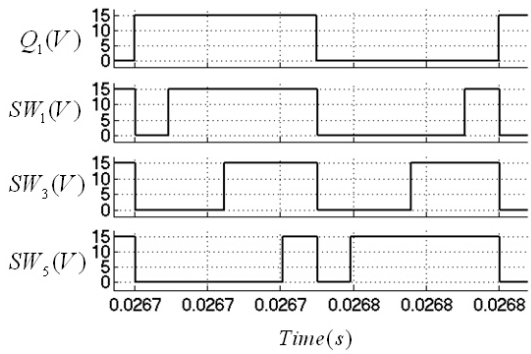


Fig. 9. Gate signals in sector I.

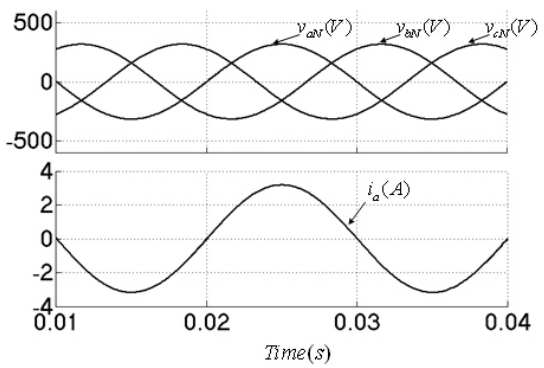


Fig. 10. Three phase output voltages and one phase current.

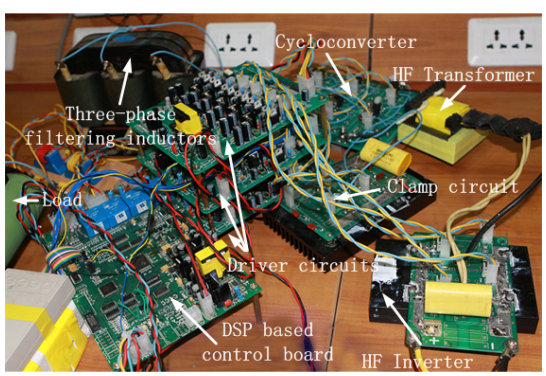


Fig. 11. Prototype of the three phase HF AC link inverter.

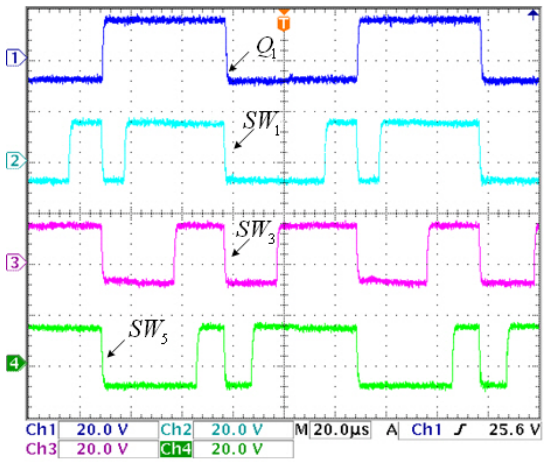


Fig. 12. Gate signals for some switches.

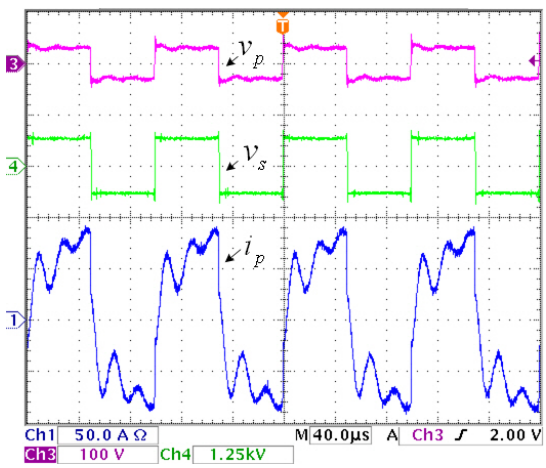


Fig. 13. Transformer voltage and primary current.

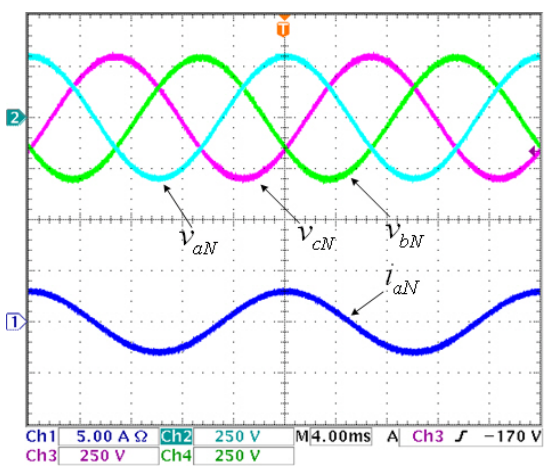


Fig. 14. Output Voltages and currents under rated resistive load.

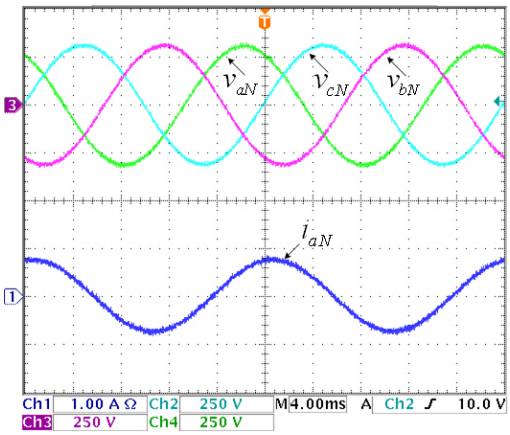


Fig. 15. Output Voltages and currents under a capacitive load.

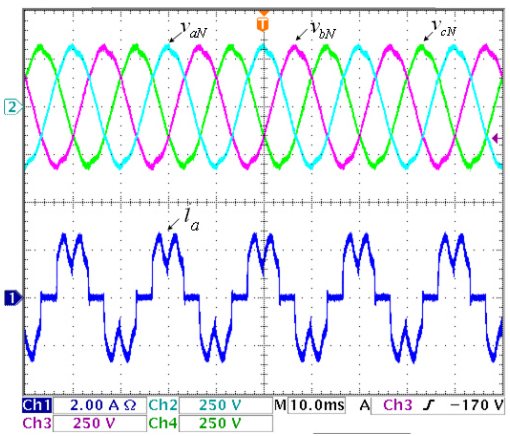


Fig. 16. Output Voltages under a rectifier-type load.

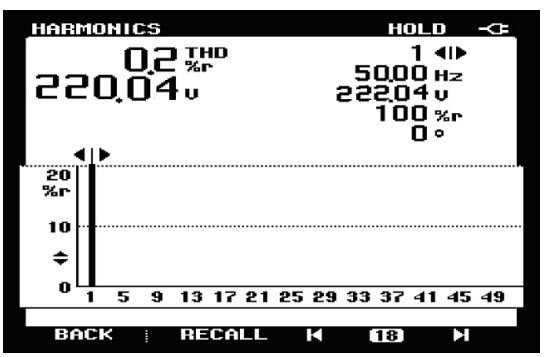


Fig. 17. Harmonic analysis of output line-to-neutral voltage v_{aN}.

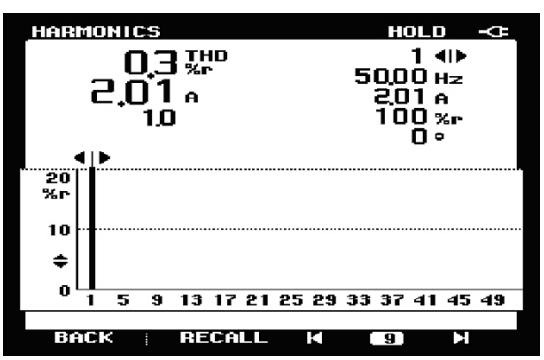


Fig. 18. Harmonic analysis of output line-to-neutral current i_{aN}

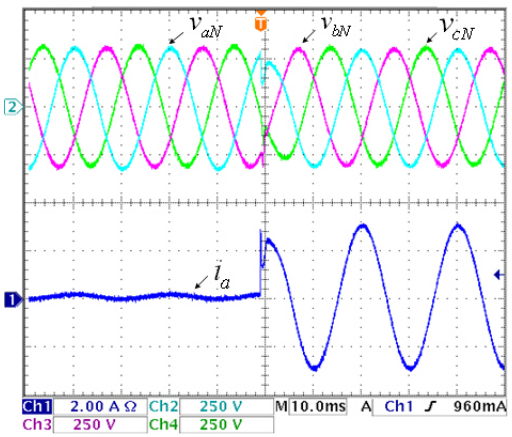


Fig. 19. Response to a step change of the load.

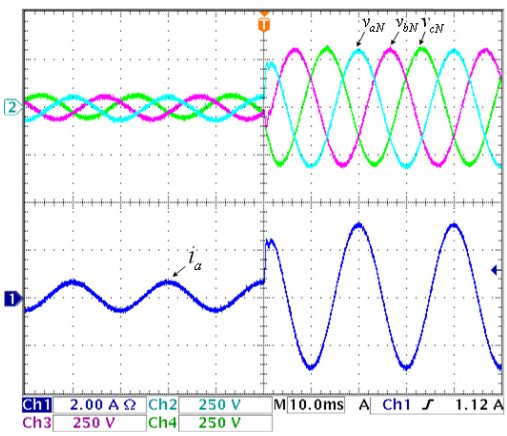


Fig. 20. Response to a step change of the output voltage reference.

Fig.10 shows the three output voltages and one phase current under a balanced and rated purely resistive load. With the proposed control strategy, we have three phase balanced sinusoidal output voltages with a low THD.

IV. Experimental Results

Experiments on a 1.45kW prototype with the same parameters as illustrated in Table I are carried out. Fig.11 shows a photograph of the laboratory prototype.

The digital control strategy for the proposed CHFACL inverter has been implemented with a DSP (TMS320F2407). All of the gate signals and the implementation of the closed loop control are carried out by the DSP. To guarantee the sensing accuracy, an external 14-bit A/D max125 is taken to sense the DC input voltage and the output three voltages. A CPLD EPM3064 is used to implement the logic process. The drive circuit for the HF switches is transformer isolated while that for the cycloconverter switches is implemented by opt couplers with independent power supplies.

In addition, the prototype contains the following power devices:

1) switching devices Q_1-Q4: FQA160N08
2) transformer: EE85 ferrite core with 1:N=5:110
3) switching devices SW_1-SW_6: IXFH24N80P.

Fig.12 shows the gate signals for some of the switches during sector I in the experiment. As seen, the driving logic for

the HF inverter and the cycloconverter switches agrees well with the analysis in Section 2 and the simulation results in Section 3. Fig.13 shows the transformer primary voltage, the secondary voltage and the primary current. It is worth noting that although the primary current has a sudden change during mode transfer as explained previously in the simulation results analysis, the voltage spikes can be suppressed effectively by using the proposed active clamp circuit.

Fig.14 shows the three output line-to-neutral voltages and the one phase current under the rated resistive load. As seen, during the steady state, the output line-to-neutral voltages are almost purely sinusoidal and well balanced. Fig.15 gives the three phase output line-to-neutral voltages under a capacitive load which is the series connection of a 20Ω resistor and a 40 μF capacitor. As can be seen, the converter has bi-directional power flow capability. Even under nonlinear loads, the THD of the output AC voltage is very low for the implementation of the repetitive control, which can be seen in Fig.16. The load is a three-wave-bridge-rectifier connected directly to a 100μF capacitor in parallel with a 200Ω resistor.

The total harmonic distortion (THD) of the line-to-neutral voltage and the current of phase A are shown in Fig.17 and Fig.18, respectively. The load is a rated purely resistive load. As seen, both the output voltage and the current are almost purely sinusoidal with a very small THD. This is because the proposed control strategy employing RC can effectively mitigate the output harmonics.

Fig.19 and Fig.20 show the output line-to-neutral voltages due to a step change in the load and the voltage reference, respectively. As seen in Fig.19, a full load is suddenly added to the system at the peak value of the line-to-neutral voltage of phase A. Although there is a small sag in the line-to-neutral voltage of phase A for a short time interval, the three-phase output voltages are regulated to be balanced quickly. In Fig.20, the output voltage reference sustains a step rise in the peak value of the line-to-neutral voltage of phase A, and the three-phase output voltages are regulated to be well balanced quickly after the change. As can be seen, despite the transient, the system with the proposed control strategy has a good dynamic response.

V. Conclusions

This paper proposes a digital control strategy for a three phase HFACL inverter composed of a full-bridge inverter and a high frequency transformer followed by a three phase cycloconverter. The proposed control strategy is very simple to implement with a DSP based on SVM modulation. The working principles are analyzed. The conversion efficiency can be improved due to the fact that no current is flowing through the body diodes of the cycloconverter MOSFETs. With only one DSP, the gate signals for all of the switches can be generated. In addition, all of the control purposes are carried out by the same DSP. The effectiveness of the proposed control strategy is verified by simulation results. A 1.45kW prototype is fabricated and evaluated. The experimental results agree well with the analysis and the simulation results. With the proposed control strategy employing RC, the proposed converter has an excellent static response even under a rectifier-type load. Additionally, the dynamic response of the system is good.

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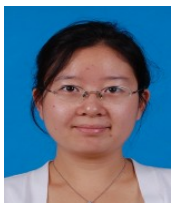

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