

Duty Ratio Predictive Control Scheme for Digital Control of DC-DC Switching Converters

Pengju Sun[†] and Luwei Zhou^{*}

^{†*} State Key Laboratory of Power Transmission Equipment & System Security and New Technology, College of Electrical Engineering, Chongqing University, Chongqing, China

Abstract

The control loop time delay caused by sampling, the zero-order-holder effect and calculations is inevitable in the digital control of dc-dc switching converters. The time delay will limit the bandwidth of the control loop and therefore degrade the transient performance of digital systems. In this paper, the quantization time delay effects with different time delay values based on a generic second-order system are analyzed. The conclusion that the bandwidth of digital control is reduced by about 20% with a one cycle delay and by 50% with two cycles of delay in comparison with no time delay is obtained. To compensate the time delay and to increase the control loop bandwidth, a duty ratio predictive control scheme based on linear extrapolation is proposed. The compensation effect and a comparison of the load variation transient response characteristics with analog control, conventional digital control and duty ratio predictive control with different time delay values are performed on a point-of-load Buck converter by simulations and experiments. It is shown that, using the proposed technique, the control loop bandwidth can be increased by 50% for a one cycle delay and 48.2% for two cycles of delay when compared to conventional digital control. Simulations and experimental results prove the validity of the conclusion of the quantization effects of the time delay and the proposed control scheme.

Key Words: DC-DC switching converters, Digital control, Duty ratio predictive control, Quantization effects, Time delay compensation

I. INTRODUCTION

Over the past decade, as the performance/price ratio of digital processors continues to increase, digital control is potentially becoming a cost-effective and alternative solution to analog control in dc-dc switching converters. It is well known that digital control offers potential advantages over analog control such as reprogrammability, ease of implementing more advanced and sophisticated control algorithms, lower susceptibility to aging and environmental variations (temperature, humidity, etc.), and better noise immunity [1]–[9].

However, the digital control of dc-dc switching converters also has some limitations, such as a limited signal resolution, quantization errors and a control loop time delay. One of the major disadvantages is the inherent time delay of the control loop, which comes from the analog to digital conversion, the zero-order-holder (ZOH), the computation, the PWM generation, etc [8]–[11]. For switchmode power supplies, the control loop time delay is usually an integral multiple of the switching period since the duty ratio can only be updated at the beginning of each switching cycle. Because of this delay,

the system enters into the next or the next several cycles after the duty ratio of this switching cycle has been calculated. As a result, it is difficult to obtain high-performance dc-dc switching converters using the traditional digital control technology.

The investigation of time delay has been an important subject in the digital control of dc-dc switching converters. In the existing literature, a basic understanding of the effects of the control loop time delay includes significantly degrading the control loop performance, reducing the controller bandwidth and degrading the transient response characteristics [2]–[13]. However, the quantization effects of the time delay on system performance and dynamic response have not been fully taken into account. In [12],[13], an exact small-signal discrete-time model of Buck and Boost converters with a time delay is proposed. It shows that the phase response of the control to output voltage transfer function is reduced with the increasing of the time delay based on an application example, which is also a qualitative description, not quantitative. However, it is unknown how much the control loop bandwidth is reduced. It is also unknown how great an influence there is on performance. There is no general quantitative description of the time delay effects among the existing research results.

To overcome the effects of the control loop time delay, some methods have been proposed for the digital control of dc-dc switching converters [11], [14]–[19]. Adding pole/zero

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[†] Corresponding Author: spengju@163.com

Tel: +86-13594144949, Fax: +86-23-65111934, Chongqing University

^{*} State Key Laboratory of Power Transmission Equipment and System Security & New Technology, College of Electrical Engineering, Chongqing University, China

pair to an existing digital controller to compensate for the phase lag introduced by ZOH has been proposed in [15]. This method has the advantage that it is not necessary to redesign the control parameters. However, this compensator may lead to instability at low sampling rates and it is also limited to the compensation of the delay of ZOH, not the total of the control loop [18]. Smith predictor and dead-beat control methods have been widely used to reduce the effects of time delay [14]-[16]. Nonetheless, since they are based on a model of the controlled plant, more computational resources are required, particularly for more complex systems and for high switching frequency and/or short available calculation times. An analogue wrap-around method employing a mixed realization using an ‘analogue wrap-around’ by adding a proportional signal to bypass the computer for the computer’s digitally-evaluated components is presented in [17]. The control loop bandwidth is increased with this method, but it also requires redesigning the control loop circuits and adding analog components. Bibian and Jin [11] presented two compensation predictors, which include a modified predictor and a simplified predictor. They show that both methods result in an increase in the controller bandwidth. However, both of them can only compensate a one cycle time delay, the modified predictor reduces robustness as it is based on a model of the controlled converter, and the simplified predictor induces a new time delay to the control loop because of the assumption that the control variable is updated only once every two sampling periods [11], [19]-[20].

In order to fully utilize the advantages of digital control, improve stability, reliability and dynamic response of digital controlled dc-dc switching converters, and overcome the time delay effects, the quantization effects of different time delay values based on a generic system and a new simple, robust duty ratio predictive technique are presented in this paper. A comparison of the control loop performance is presented respectively for the no time delay, the conventional digital control (CDC) with time delay and the duty ratio predictive control (DP) proposed in this paper. Simulations and experimental results provide further verification of the conclusion of the quantization effects on the time delay and the improved performance with the proposed duty ratio predictive control method.

In this paper, the quantization effects of the time delay based on a generic second-order system are analyzed in detail in Section II. The concept, implementation and compensation effect of the duty ratio predictive control scheme are discussed in Section III. Then section IV describes an application of the proposed scheme on a voltage mode controlled point-of-load Buck converter, and simulations and experimental results verify the validity of the analytical results and the proposed duty ratio predictive control method. The conclusion of this paper is drawn in Section V.

II. QUANTIZATION EFFECTS OF TIME DELAY

Conventionally, the control loop time delay of switching mode dc-dc converters is an integral multiple of the switching period since the duty ratio can only be updated at the beginning of each switching cycle [2], [11]-[13], [18]. To understand

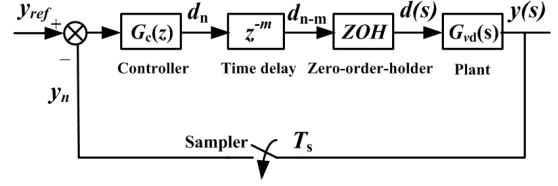


Fig. 1. Discrete time domain feedback control system.

the time delay problem, we consider the digital control loop represented in Fig. 1, where $G_c(z)$ is the discrete time domain controller, $G_{vd}(s)$ is the control-to-output transfer function of the plant to be controlled, ZOH is the zero-order-holder, z^{-m} is the digital control loop time delay which has m cycles of delay, d_n is the duty ratio at the n th switching cycle, and T_s is the sampling period which also equals the switching period of the converter.

Without loss of generality, we assume the plant to be a generic second-order system to analyze the quantization effects of the time delay. We have:

$$G_{vd}(s) = \frac{k_1 \cdot s + k_2 \cdot \omega_0^2}{s^2 + 2\xi \omega_0 \cdot s + \omega_0^2}. \quad (1)$$

The natural frequency ω_0 , the damping factor ξ and the coefficients k_1 and k_2 can be obtained through open loop identification. The process transfer function $G_{vd}(s)$ can be transposed into the discrete time domain using a classical z -transform table and a certain approximation ($\xi \omega_0 T_s \ll 1$) (see [11])

$$G_{vd}(z) = (1 - z^{-1})Z\left(\frac{G_{vd}(s)}{s}\right) \approx \frac{k_1 \cdot T_s}{z - 1} = \frac{k}{z - 1} \quad (2)$$

where $k = k \cdot T_s$.

A conventional PI compensation controller is used here to study the performance of a typical second-order system. In the discrete time domain, it is expressed as:

$$G_c(z) = k_p + k_i/(z - 1) \quad k_p > 0, \quad k_i > 0. \quad (3)$$

The discrete open-loop transfer functions $G_{o_no}(z)$ (without a time delay) and $G_{o_delay}(z)$ (with a time delay) are presented as:

$$\begin{cases} G_{o_no}(z) = G_c(z) \cdot G_{vd}(z) = \frac{k}{z - 1} \cdot (k_p + \frac{k_i}{z - 1}) \\ G_{o_delay}(z) = G_c(z) \cdot z^{-m} \cdot G_{vd}(z) = z^{-m} \cdot \frac{k}{z - 1} \cdot (k_p + \frac{k_i}{z - 1}). \end{cases} \quad (4)$$

The frequency response of a discrete transfer function can be measured by substituting z with $e^{j\omega T_s}$. Given the phase margin φ_m , the cross-over frequency f_c and k , the coefficients k_p and k_i can be derived from the following equations:

$$\begin{cases} |G_o(e^{j2\pi f_c T_s})| = 1 \\ \angle G_o(e^{j2\pi f_c T_s}) = -180^\circ + \varphi_m. \end{cases} \quad (5)$$

From (4) and (5), we can see that the coefficient k is just a proportional coefficient and that it does not affect the positive or negative of k_p and k_i . Taking a system with $k = 1$ and a given phase margin $\varphi_m = 45^\circ$ as an example, the relation curves between k_p, k_i and f_c for different time delay values are shown in Fig. 2 where $\lambda = f_c \cdot T_s = f_c / f_s$. In Fig. 2, when both

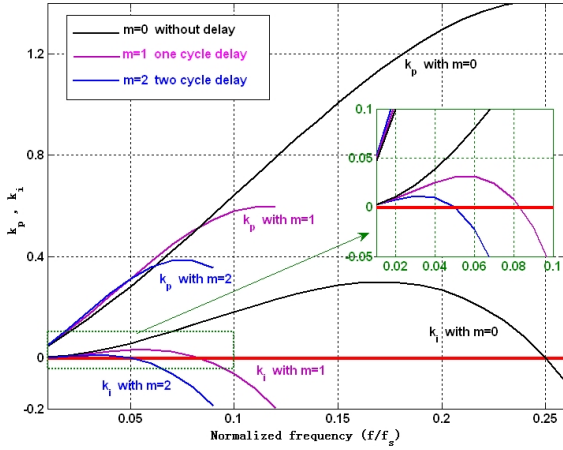


Fig. 2. Compensator coefficients k_p , k_i as a function of cross-over frequency f_c at different values of time delay.

k_p and k_i are positive, the maximum λ is 0.25, 0.083 and 0.05 without a time delay, with a one cycle delay and with two of cycles delay, respectively. In practical applications, the cross-over frequency is generally set to one-tenth of the switching frequency, which means that λ is 0.1. The maximum that λ can be compensated to is 0.083 using a conventional digital control method when the system has a one cycle time delay, that is to say, the system bandwidth with a one cycle time delay is reduced by about 20% when compared with an ideal design without a time delay. In a similar manner, the control loop bandwidth with two cycles of time delay is reduced by 50%. Based on equations (4) and (5), the more cycles of time delay, the larger decrease in control loop bandwidth with the same phase margin. One and two cycles of time delay are the common cases in practical applications, therefore, the quantitative effects of a time delay is that the control loop bandwidth is reduced by about 20% and 50% with one cycle of delay and two cycles of delay, respectively. This conclusion is suitable for almost all of the dc-dc switching converters.

III. PROPOSED DUTY RATIO PREDICTIVE CONTROL SCHEME

Based on the research work in section II, the bandwidth is reduced because of a control loop time delay. In order to improve the transient performance of digital controlled dc-dc switching converters which require a fast dynamic response speed, in this section, we propose a predictive control scheme based on the linear extrapolation technique which is well known in the control field.

A. Prediction Concept

In Fig. 1, the control variable d_n , calculated to compensate for the error between y_n and the reference value y_{ref} , is used only after m sampling periods because of a time delay. The main idea behind the duty ratio predictive control method is to update the controller using \hat{d}_{n+m} , which is the estimated value of d_{n+m} . The predictive control variable \hat{d}_{n+m} can be achieved at the time $t = T_n$. As a result, the plant output is adjusted without delay under ideal conditions. The control loop time

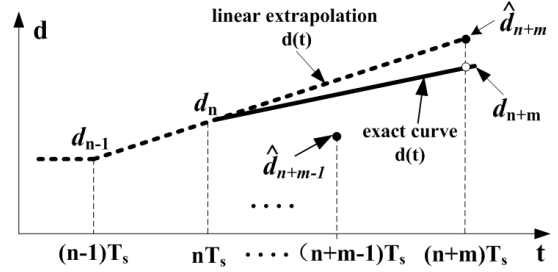


Fig. 3. Representation of the prediction function mechanism.

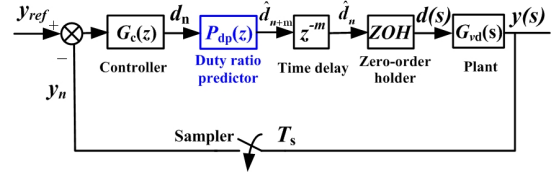


Fig. 4. Control loop system with duty ratio predictor.

delay is fully compensated when the estimated value equals the future control variable, that is, $\hat{d}_{n+m} = d_{n+m}$.

The estimated \hat{d}_{n+m} can be calculated based on the linear extrapolation technique, and Fig. 3 gives a graphical representation of the predictive scheme, where T_s is the sampling period as well as the switching period. The PWM duty ratio d_n , which is calculated based on the occurrence of the n th switching cycle, is only applied at the $(n+m)$ th switching cycle because the control loop time delay is m cycles. As a result of the linear extrapolation, the estimated \hat{d}_{n+m} , d_n , and d_{n-1} are on the same line. The estimate of \hat{d}_{n+m} can be expressed as:

$$\hat{d}_{n+m} = (m+1)d_n - md_{n-1}. \quad (6)$$

The expression (6) can be transposed in the discrete time domain as:

$$\hat{d}(z) = \frac{(m+1)z - m}{z} \cdot d(z) = P_{dp}(z) \cdot d(z). \quad (7)$$

A discrete control loop system integrating the duty ratio predictor is represented in Fig. 4, where $P_{dp}(z)$ is the duty ratio predictor. As shown in Fig. 4, the discrete open-loop transfer functions with the duty ratio predictor and with the conventional digital control method (without the duty ratio predictor) are expressed respectively as:

$$G_{o_dp}(z) = G_c(z) \cdot P_{dp}(z) \cdot z^{-m} \cdot G_{vd}(z) \quad (8)$$

$$G_{o_cdc}(z) = G_c(z) \cdot z^{-m} \cdot G_{vd}(z). \quad (9)$$

B. Compensation Effect

To study the effect of the proposed predictor on control loop design, only the time delay models of the duty ratio predictive control and a conventional digital control are compared since the parameters of the PI controller, the controlled plant and the zero-order-holder are the same.

Using $z = e^{j\omega T_s}$, the m cycles of time delay and the duty ratio predictor can be transposed into the continuous time domain,

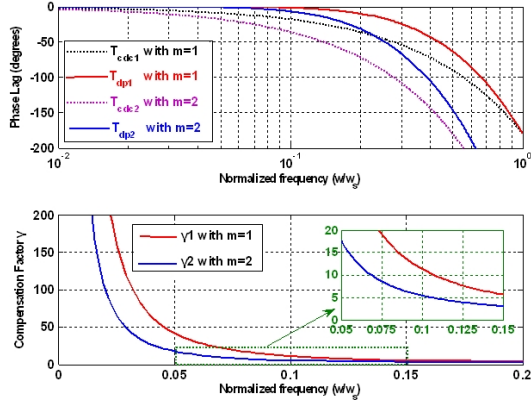


Fig. 5. Characterization of the compensation effect.

and the time delay models of conventional digital control and the duty ratio predictive control are expressed as:

$$\begin{cases} T_{cdc}(j\omega) = e^{-m \cdot j\omega T_s} \\ T_{dp}(j\omega) = e^{-m \cdot j\omega T_s} \cdot P_{dp}(j\omega) \\ = e^{-m \cdot j\omega T_s} \cdot [(m+1) - me^{-j\omega T_s}] \end{cases} \quad (10)$$

To assess more accurately the compensation capability of the proposed predictor, we define the phase lag compensation factor γ as the ratio of the phase lag before and after prediction. For the duty ratio predictor, we have:

$$\gamma = \frac{\phi T_{cdc}(\omega)}{\phi T_{dp}(\omega)} \quad (11)$$

The phase lag reduction of expression (10) and the phase lag compensation factor for $m=1$ and $m=2$ are shown in Fig. 5 where ω_s is the sampling angular frequency. From this diagram, the delay effects on the phase response are clearly visible and they are more serious with an increase in m . Fortunately, the phase lag is reduced significantly by using the duty ratio predictor, and the effectiveness of the predictor increases with a decrease in frequency. For instance, if the sampling frequency is much higher than the cross-over frequency of the controller, the control loop time delay is almost fully compensated. If the cross-over frequency of the control loop is about one tenth of the sampling frequency, the phase lag is reduced by a factor of 11 for a one cycle delay and 5 for two cycles of delay. If γ is below 1, no improvement should be expected with the proposed duty ratio predictor. From Fig. 5, it can also be seen that the compensation effectiveness for two cycles of delay is not as good as that for a one cycle delay because the previous duty ratios used to calculate the predictive control variable \hat{d}_{n+m} are a little far away from the $(n+m)^{\text{th}}$ cycle, and the information included in them is not enough to estimate an exact d_{n+m} . It is a limitation of the duty ratio predictive scheme based on the linear extrapolation technique to compensate for multiple cycles of delay.

IV. SIMULATION AND EXPERIMENTAL ANALYSIS

To validate the duty ratio predictive control concept, we applied the proposed control design procedure to the point-of-load converter represented in Fig. 6. The power stage of the point-of-load is a Buck converter, and the parameters of the

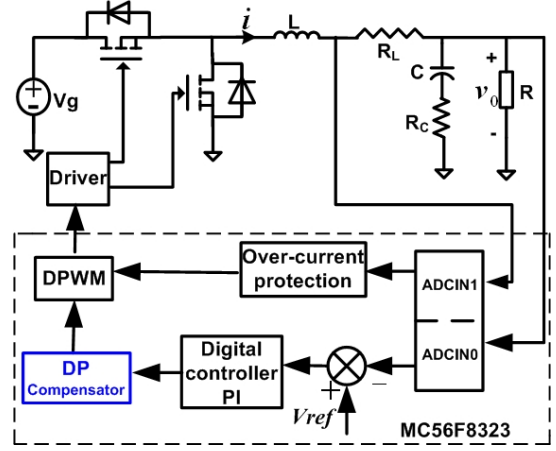


Fig. 6. Point-of-load Buck converter and its DSP controller.

converter are given as: $V_g = 12\text{V}$, $V_{ref} = 2.5\text{V}$, $D = 0.21$, $L = 20\mu\text{H}$, $R_L = 160\text{m}\Omega$, $C = 1000\mu\text{F}$, $R_C = 80\text{m}\Omega$, $R = 1\Omega$, and $f_s = 1/T_s = 100\text{kHz}$. The control-to-output transfer function $G_{vd_buck}(s)$ of the Buck converter can be obtained based on the classical state space averaging technique [21].

A conventional PI compensator is used and designed based on the previous method in section II. When the control loop has no time delay, the parameters of the PI controller are designed as $k_{pa} = 1.316$ and $k_{ia} = 0.3820$ to get a 10kHz cross-over frequency and a 45° phase margin. When the control loop has one and two cycles of delay, with the same 45° phase margin, the parameters of the PI controller are designed respectively as $k_{p1} = 1.062$ & $k_{i1} = 0.0074$ and $k_{p2} = 0.6626$ & $k_{i2} = 0.0065$ to get the maximum cross-over frequency. It is necessary to note that the parameters of the PI controller are identical in both the conventional digital control method and the duty ratio predictive control method with the same time delay values.

To further verify the stability of the duty ratio predictive control method, based on the expressions (3), (8) and (9), the control-to-output transfer function $G_{vd_buck}(s)$ of the Buck converter [21] and the previous parameters of the converter and the controller, the magnitude and the phase frequency responses of the open-loop transfer function with no time delay, the conventional digital control and the duty ratio predictive control for different time delay values are shown in Fig. 7 respectively. Fig. 8 shows the root-locus of the different control conditions with different open-loop gains.

As shown in Fig. 7, with the same time delay, the magnitude and the phase responses of the conventional digital control method and the duty ratio predictive control method are almost the same in the low frequency range, but in the medium and high frequency range, the responses of the duty ratio predictive control are larger than those of the conventional digital control. The cross-over frequency and the phase margin of the no time delay condition, the conventional digital control and the duty ratio predictive control at different time delay values are summarized in Table I where the analogy control method (AC) represents the no time delay condition. As expected, with the conventional digital control the control loop bandwidth at different time delay values is reduced by about 20% and 50% respectively in comparison with the no time delay condition.

TABLE I
CONTROLLERS' CHARACTERISTICS

Control methods	Cross-over frequency f_c (kHz)	Phase margin Φ_m (°)	k_p	k_i
AC m=0	10.0	44.8	1.3160	0.3820
CDC m=1	8.33	44.5	1.0620	0.0074
DP m=1	12.1	52.4		
CDC m=2	5.02	44.6	0.6626	0.0065
DP m=2	7.44	58.7		

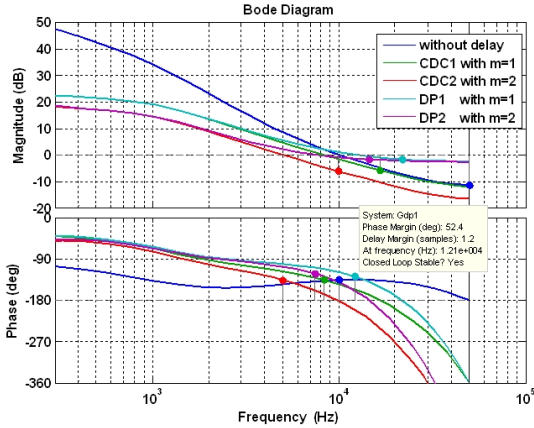


Fig. 7. Magnitude and phase responses at different conditions.

Compared with the conventional digital control method, with the same parameters for the PI controller, the cross-over frequency and the phase margin are increased by 50% and 8° respectively with the duty ratio predictive scheme at m=1, and increased by 48.2% and 14° at m=2. Note that the cross-over frequency of the duty ratio predictive control method is even superior to that of the analogy control when there is a one cycle delay. After compensation, the cross-over frequency of two cycles of delay is still less than that of the analogy control, which means that the time delay is not fully compensated. However, the cross-over frequency is also increased by 48.2% using the proposed predictive control method. That is to say, for multiple cycles delay applications, the compensation effect is not as good as the one cycle delay condition, which is a limitation of the proposed compensation method.

From Fig. 8, increasing the open loop gain causes one or both of the closed loop poles to leave the unit circle. The stability boundaries are shown in Table II. It can be seen that the stability boundary is increased by using the duty ratio predictive control scheme with the same time delay.

The bandwidth of the digital control system is limited due to the control loop time delay, and the impact of the bandwidth is reflected to the output transient response in the time domain. An experimental analysis of the output transient response with the different control methods is discussed below to verify the results of the analysis and the simulation.

TABLE II
STABILITY BOUNDARY AT DIFFERENT TIME DELAY CONDITIONS

Time delay and control method	Gain at the stability boundary
CDC m=0	3.70
CDC m=1	1.95
DP m=1	2.42
CDC m=2	2.0
DP m=2	3.69

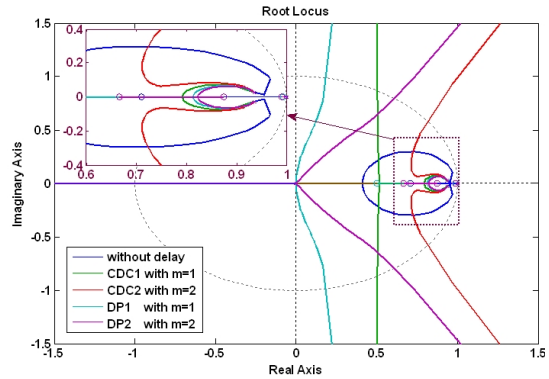


Fig. 8. Root-locus for the buck converter example at different conditions.

An experimental system of a point-of-load Buck converter based on a digital control IC MC56F8323 is set up, and the analogy control method using a PWM controller IC TL494 is implemented to represent the no time delay condition. The three control methods, analogy control, conventional digital control and duty ratio predictive control are implemented on this platform, respectively. If the sampling period equals the switching period and the calculation time is smaller than the switching period, it always has a one cycle time delay, and a flow chart for the CDC and the DP methods is shown in Fig. 9(a). For two cycles of time delay, it can be obtained through estimations and reasonable programming and the flow chart is shown in Fig. 9(b).

With the same controller parameters as the simulation, the experimental waveforms of the load transient response using the three control methods for different time delay values with the load stepped from 1A to 5A and then back from 5A to 1A are illustrated in Fig. 10.

An increase and decrease of load will cause a transient process. It is clearly shown in Fig. 10 (a), (b) and (d) that the conventional digital control method increases the transient response time from 100µs to 120µs or 200µs compared with the analogy control when the load current changes from 1A to 5A. From Fig. 10(c), when the load step changes at m=1, it takes about 80µs to reach the new steady-state which is reduced by 33% when compared with the conventional digital control shown in Fig. 10 (b). Similarly, the settling time is reduced by 30% when the system has two cycles of delay when Fig. 10 (d) is compared to Fig. 10 (e).

In Table III, the experimental results for a load disturbance are presented. The transient response of the conventional digital control is slower than that of the analogy control due to the control loop time delay, and the compensation of load disturbances is faster using the duty ratio predictive scheme. Moreover, the overshoot and undershoot are both reduced.

It can be clearly seen from the experimental results that the transient response time is inversely proportional to the bandwidth of the control loop, which gives further verification that the conclusions of the quantization time delay effects are correct and that the proposed duty ratio predictive control scheme can greatly decrease the effects of the time delay and improve the transient performance of a digital controller significantly.

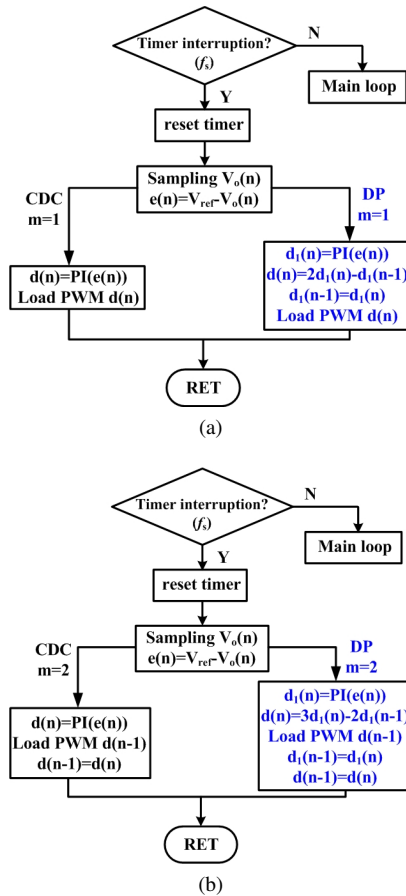


Fig. 9. Flow charts of the algorithms with different time delay. (a) one cycle delay $m=1$. (b) two cycles delay $m=2$.

TABLE III
EXPERIMENTAL RESULTS OF LOAD CHANGING

Control method	Settling time(μ s)		Overshoot voltage (mV)		f_c (kHz)
	1A \rightarrow 5A	5A \rightarrow 1A	1A \rightarrow 5A	5A \rightarrow 1A	
AC $m=0$	100	120	200	200	10.0
CDC $m=1$	120	140	300	300	8.33
DP $m=1$	80	80	200	200	12.1
CDC $m=2$	200	200	300	300	5.02
DP $m=2$	140	140	250	250	7.44

V. CONCLUSIONS

A control loop time delay always exists in digital controllers for dc-dc switching converters. In this paper, the quantization effects of different time delay values based on a generic second-order system are analyzed and a duty ratio predictive control scheme has been developed based on the linear extrapolation technique to compensate the digital control loop time delay and to improve the dynamic response. The bandwidth of the digital control loop is reduced by about 20% with a one cycle delay and 50% with two cycles of delay in comparison with no time delay (analogy control) which seriously degrades the transient response of the digital control system. A comparison of the simulation and experimental results for the analogy control, the conventional digital control and the proposed duty ratio predictive control with different time delay values shows that the proposed method has a much better transient performance than that of the conventional digital control and that it is even superior to that of the analogy control at a one cycle delay with the same phase

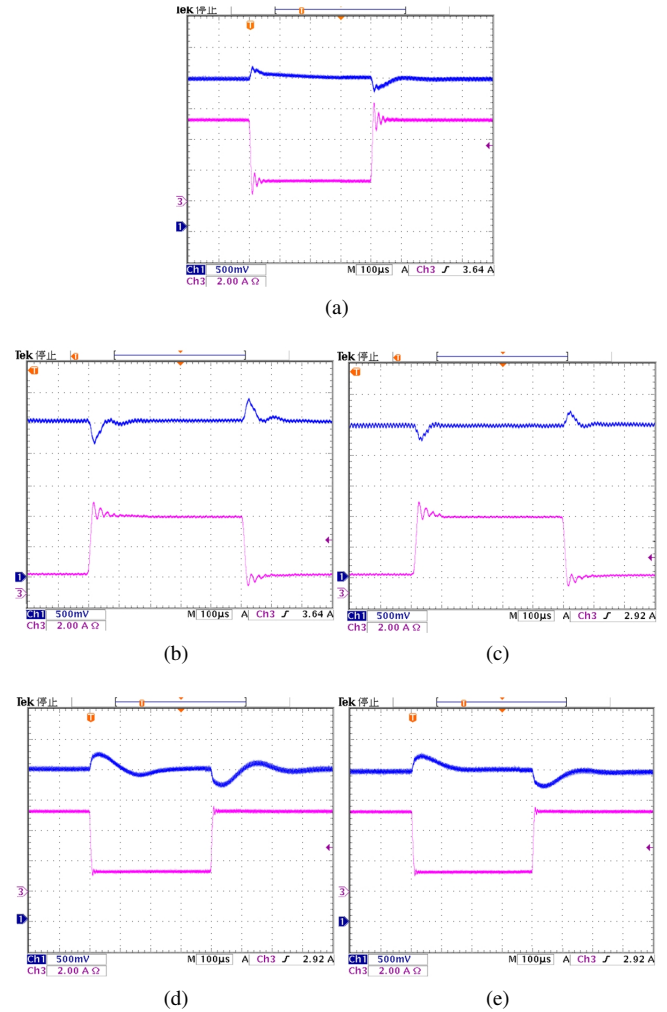


Fig. 10. Waveforms with different control methods (load current step change 1A \rightarrow 5A \rightarrow 1A). (a) Analogy control. (b) CDC with $m=1$. (c) DP with $m=1$. (d) CDC with $m=2$. (e) DP with $m=2$.

margin. Furthermore, the proposed method is more suitable for practical application since it is simple, independent of the system model and does not require a redesign of the controller. Although the bandwidth of the control loop with two cycles of delay can not be compensated as well as the analogy control, the bandwidth is still increased and the transient response is also improved using the proposed compensation method.

Although this paper focuses on a Buck-type point-of-load application, a similar concept can be extended to other digital control switching converter systems.

REFERENCES

- [1] D. Maksimovic, R. Zane, and R. Erickson, "Impact of digital control in power electronics," in *Proc. ISPSD*, pp. 13-22, 2004.
- [2] J. Q. Chen, A. Prodic, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 411-419, Jan. 2003.
- [3] L. Corradini, E. Orietti, P. Mattavelli, and S. Saggini, "Digital hysteretic voltage-mode control for DC-DC converters based on asynchronous sampling," *IEEE Trans. Power Electron.*, Vol. 24, No. 1, pp. 201-211, Jan. 2009.
- [4] H. S. Bae, J. H. Yang, J. H. Lee, and B. H. Cho, "Digital state feedback current control using the pole placement technique," *Journal of Power Electronics*, Vol. 7, No. 3, pp. 213-221, Jul. 2007.

- [5] Y. F. Liu, E. Meyer, and X. D. Liu, "Recent developments in digital control strategies for DC/DC switching converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 11, pp. 2567-2577, Nov. 2009.
- [6] J. W. Shin, B. C. Hyeon, and B. H. Cho, "Digital control of a power factor correction Boost rectifier using diode current sensing technique," *Journal of Power Electronics*, Vol. 9, No. 6, pp. 903-910, Nov. 2009.
- [7] Y. F. Liu and P. C. Sen, "Digital control of switching power converters," in *Proc. CCA*, pp. 635-640, 2005.
- [8] T.-H. Hsia, H.-Y. Tsai, Y.-Z. Lin, and D. Chen, W.-H. Chang, "Digital compensation of a high-frequency voltage-mode DC-DC converter," in *proc. EPE*, pp. 1-8, 2007.
- [9] K. G. Shin and X. Z. Cui, "Computing time delay and its effects on real-time control systems," *IEEE Trans. Control Syst. Technol.*, Vol. 3, No. 2, pp. 218-224, Jun. 1995.
- [10] J. P. Xu, G. H. Zhou and M. Z. He, "Improved digital peak voltage predictive control for switching DC-DC converters," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 8, pp. 3222-3229, Aug. 2009.
- [11] S. Bibian and H. Jin, "Time delay compensation of digital control for DC switchmode power supplies using prediction techniques," *IEEE Trans. Power Electron.*, Vol. 15, No. 5, pp. 835-842, Sep. 2000.
- [12] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled DC-DC converters," in *Proc. COMPEL*, pp.231-235, 2006.
- [13] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled PWM converters," *IEEE Trans. Power Electron.*, Vol. 22, No. 6, pp. 2552-2556, Nov. 2007.
- [14] N. Abe and K. Yamanaka. "Smith predictor control and internal model control-a tutorial," in *Proc. SICE*, pp. 1383-1387, 2003.
- [15] D. Raviv and E. W. Djaja. "Technique for enhancing the performance of discretized controllers," *IEEE Control Systems Magazine*, Vol. 19, No. 3, pp. 52-57, Jun. 1999.
- [16] S. Saggini, W. Stefanutti, E. Tedeschi, and P. Mattavelli, "Digital deadbeat control tuning for DC-DC converters using error correlation," *IEEE Trans. Power Electron.*, Vol. 22, No. 4, pp. 1566-1570, Jul. 2007.
- [17] D. W. Clarke and S. P. Maslen, "Discretising controllers with slow sampling," *IET Control Theory and Applications*, Vol. 1, No. 3, pp. 624-635, May 2007.
- [18] M. Z. He, J. P. Xu, G. H. Zhou, and N. Chen, "Algorithm to overcome time delay in digital controller of switching DC-DC converters," in *Proc. ICIEA*, pp. 2305-2310, 2007.
- [19] T. Nussbaumer, M. L. Heldwein, G. Gong, S. D. Round, and J. W. Kolar, "Comparison of prediction techniques to compensate time delays caused by digital control of a three-phase Buck-type PWM rectifier system," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 2, pp. 791-799, Feb. 2009.
- [20] S. Bibian and H. Jin, "High performance predictive dead-beat digital controller for dc power supplies," *IEEE Trans. Power Electron.*, Vol. 17, No. 3, pp. 420-427, May 2007.
- [21] R.W. Erickson and D. Maksimovic. *Fundamentals of power electronics*, Second Edition, Kluwer Academic Publishers Group, 2001.



Pengju Sun was born in Henan Province, Chian, in 1982. She received her B.S. in Electrical Engineering from Chongqing University, Chongqing, China in 2005. Since September 2005, she has been a candidate for the Master-Doctor combined program at Chongqing University. She was a Visiting Student at the University of California, Irvine, from September 2009 to August 2010. Her research interests include wide output range DC/DC converters, digital control techniques, high power high performance power converters and power factor correction.



Luowei Zhou was born in Sichuan Province, China, in 1954. He received his B.S., M.S., and Ph.D. in Electrical Engineering from Chongqing University, Chongqing, China, in 1982, 1988, and 2000, respectively. Since 1982, he has been with the College of Electrical Engineering, Chongqing University, where he is currently a Full Professor. He was a Visiting Professor at the University of California, Irvine, from September 1998 to August 1999. He is the Administrative Director of the China Society of Power Supply. He has published more than 60 papers, is the holder of one U.S. and three Chinese patents, and has three patents pending. His major research interests include the analysis and control of power electronics circuits, the realization of active power filters, power factor correction techniques, and high frequency power conversion.