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Novel Interleaved Single-Stage AC/DC Converter with a High Power Factor and High Efficiency

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Abstract

A novel single-stage AC/DC converter with the soft-switching characteristic based on interleaving technology and an LLC topology is proposed here. The converter is integrated by an interleaved cell and an LLC cell. Because the components of the system are reduced as a result of integrating, the cost decreases. Since interleaving technology is adopted, the converter can work in a high voltage input state. The LLC topology chosen here ensures that the switches on the primary side work in the ZVS condition and that the diodes on the secondary side work in the ZCS condition, which decreases the switching loss of the system. A theoretical analysis and the design procedures of the proposed converter are proposed and discussed in detail. Simulations and experimental studies with a 100W prototype are done to prove the analysis.

Key Words: AC/DC, Interleaving, LLC, ZCS, ZVS

I. INTRODUCTION

There is usually a full-bridge rectifier and a large input capacitor in a common AC/DC converter which causes rich harmonics and a low power factor. Recently, standards such as IEEE 519 and IEC 61000-3-2 have imposed limits on the harmonic current drawn by pieces of equipment connected to an ac line in order to prevent the distortion of ac line voltage. Usually the solution is to add a PFC (power factor correction) pre-regulator in the DC-DC stage by shaping the input current so that it is sinusoidal and in phase with the input voltage. A two-stage AC-DC converter has a very high PF and a low THD, but at an increased cost [1], [2]. Therefore, a single-stage AC/DC converter is proposed to reduce the cost and to simplify the circuit. A single-stage AC/DC converter is achieved by combining the PFC stage and the DC/AC stage into one stage by sharing one or more switches.

Recently, many new single–stage AC/DC converters have been proposed, but most of them did not pay much attention to soft switching. As a result, the switches usually have a lot of voltage or current stresses, which decrease the efficiency of the converter [3]–[7]. Some researchers have adopted a full-bridge converter to form a single-stage converter in order to achieve soft switching, but the full-bridge has four switches which increases the cost and the control method is complicated [8]–[10].

A boost topology is usually adopted to be the PFC stage, because it has many advantages such as the main inductor is on the input side which decreases the input harmonics and the switch links to the power ground which makes it easy to design the drive circuit. Since half bridge converters are very simple, and they supply two switches to be combined with, they are very widely used in single-stage AC/DC converters [11]–[15]. There has been a great deal of research on single-stage AC/DC converters by integrating a boost circuit with a half bridge converter, but the output voltage must be higher than the input voltage, so they are only suitable for low line input [11], [12]. If they are used for a 220 AC input, the bus voltage will be twice as high as the input peak value, which increases the voltage stress for both the switch and the bulk capacitor. As a result, a switch and capacitor with a high rated voltage must be used which increases the cost a lot.

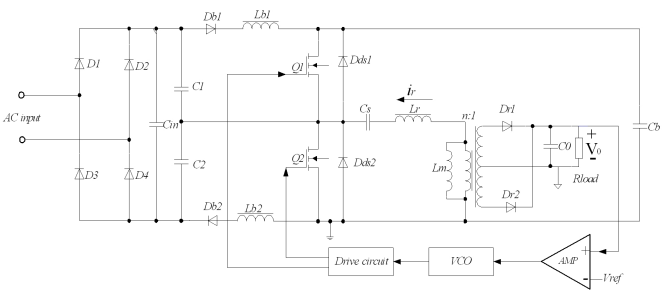

Fig. 1. Single-stage AC/DC converter proposed in the paper.

A simple single-stage topology is proposed in [14], which integrates a boost circuit and a half-bridge converter. Since an LLC circuit is adopted, the primary switches can work in the ZVS state, and the secondary diodes can work in the ZCS state, which decreases the switching losses of the system a great deal. However, its drawback is very clear. The bus voltage is

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always twice as high as the peak input value, so if it is used in a high line input, the voltage stress of the system is much higher, and since its input current is in the discontinuous state, its THD is also high. A novel single stage AC/DC converter is proposed in this paper to achieve soft switching and to avoid adding extra voltage stress to the components of the converter. The proposed converter is shown in Fig.1. It is made up of two cells: an interleaving cell and an LLC cell. In the interleaving cell, the half-bridge is divided into two boost cells, and the boost circuit works in the DCM which has a natural PFC function. Because the half-bridge is divided into two boost cells, the output voltage can be controlled a little higher than the input voltage, so it can be used in a high line input. The two boost cells work in the interleaving mode, so the input current is continuous, which decreases the THD of the system. The other cell is an LLC circuit. If it works at a proper frequency, the primary switches can work in the ZVS condition and the secondary diodes can work in the ZCS state, which decreases the switching losses of the converter. In the laboratory, a 100W prototype was constructed. The PF of the converter is as high as 0.99, the THD is lower than 10%, and the efficiency is as high as 90.25%.

II. Operating principles

Fig.1 shows the proposed converter. It is made up of two cells: a PFC cell and an LLC cell. L_{b1}, Q_1, D_{ds2} and C_b form a boost circuit, and L_{b2}, Q_2, D_{ds1} and C_b form the other boost circuit. The PFC cell is made up of two boost circuits which work in the discontinue mode. Since the half bridge must work with a dead time, the switching duty cycle is nearly 0.5, and the two boost circuit work in the interleaving mode. C_{in} is used as an input filter to filter the high-frequency harmonics after rectification, and C_1 and C_2 are voltage dividers to form two boost circuits in the interleaving mode.

A half bridge circuit and a resonant circuit form an LLC cell. L_r is the leakage inductor of the transformer, and L_m is the magnetizing inductor. If a proper switching frequency is selected, the switches Q_1 and Q_2 can work in the ZVS mode and the diodes D_{r1} and D_{r2} can work in the ZCS mode, which increases the efficiency a great deal. The converter has six operation modes in a single duty cycle. In the following descriptions, the working flow of the converter is shown in detail.

Mode 1 ($t_0 \sim t_1$): This mode begins when Q_2 is turned off at t_0. In this mode, because Q_2 is turned off and Q_1 is not yet opened, L_{b2} discharges through C_2, D_{ds1}, the resonant load and C_b. The energy stored in L_{b1} was released in the last mode, so now there is no energy saved inL_{b1}. At the same time, the resonant current i_r discharges the output capacitor of Q_1, and the voltage of Q_1 between the drain pole and the source pole begins to fall. When the voltage deceases to zero, the body diode of Q_1 is turned on. On the secondary side of the transformer, D_{r1} is turned on, and the voltage of L_m is clamped by the output voltage. In fact L_r and C_s resonate in this moment, and the current of L_m increases linearly.

Mode 2 ($t_1 \sim t_2$): At t_1, the drive signal of Q_1 begins, and Q_1 is turned on in the ZVS state. L_{b1} begins being charged. Because the dead time of the half bridge is very short, L_{b2} continues to be charged until the current of L_{b2} reaches zero. L_m continues to increase linearly, and the resonant current i_r runs through Q_1 and increases with a sinusoidal shape. The current running through the rectifier D_{r1} is the difference between the resonant current and the magnetizing current. Since the working frequency is smaller than the resonant frequency of L_r and C_s, Q_1 is still in the open state after half a resonant cycle. When the resonant current equals the magnetizing current, this mode ends.

Mode 3 ($t_2 \sim t_3$): In this mode, because Q_1 is still open, L_{b1} continues to be charged until its voltage reaches the peak value when Q_1 is turned off. The energy stored in L_{b2} was released in the last mode, so now there is no energy saved in L_{b2}. At t_2, D_{r1} is turned off in the ZCS state, so that the secondary side is separated from the resonant circuit, the voltage of the magnetizing inductor is not clamped by the output voltage, and L_m and L_s resonate with C_s. Since $L_m >> L_r$, the resonant period becomes much longer. This can then be seen as: $i_r(t) = i_m(t) = I_m$.

Mode 4 ($t_3 \sim t_4$): This mode begins when Q_1 is turned off at t_3. In this mode, because Q_1 is turned off and Q_2 has not yet been opened, L_{b1} discharges through C_1, D_{ds2}, the resonant load and C_b. The energy stored in L_{b2} was released in the last mode, so now there is no energy saved in L_{b2}. At the same time, the resonant current i_r discharges the output capacitor of Q_2, and the voltage of Q_2 between the drain pole and the source pole begins to fall. When the voltage decreases to zero, the body diode of Q_2 is turned on. On the secondary side of the transformer, D_{r2} is turned on, and the voltage of L_m is clamped by the output voltage. In fact L_r and C_s resonant at this moment, and the current of L_m increases linearly.

Mode 5 ($t_4 \sim t_5$): At t_4, the drive signal of Q_2 begins, and Q_2 is turned on in the ZVS state, and L_{b2} is charged. Because the dead time of the half bridge is very short, L_{b1} continues to be charged until the current of L_{b1} reaches zero. i_m continues to decrease linearly, and the resonant current i_r runs through Q_2 and increases with a sinusoidal shape. The current running through the rectifier, D_{r2} is the difference between the resonant current and the magnetizing current. Since the working frequency is smaller than the resonant frequency of L_r and C_s, Q_2 is still in the open state after half a resonant cycle. When the resonant current equals the magnetizing current, this mode ends.

Mode 6 ($t_5 \sim t_6$): In this mode, because Q_2 is still open, L_{b2} continues to be charged until its voltage reaches the peak value when Q_2 is turned off. The energy stored in L_{b1} was released in the last mode, so now there is no energy saved in L_{b1}. At t_2, rectifier D_{r2} is turned off in the ZCS state, so that the secondary side is separated from the resonant circuit, the voltage of the magnetizing inductor is not clamped by the output voltage, and the magnetizing inductor and the resonant inductor resonate with the resonant capacitor. Since $L_m >> L_r$, the resonant period becomes much longer. This can then be seen as: $i_r(t) = i_m(t) = I_m$.

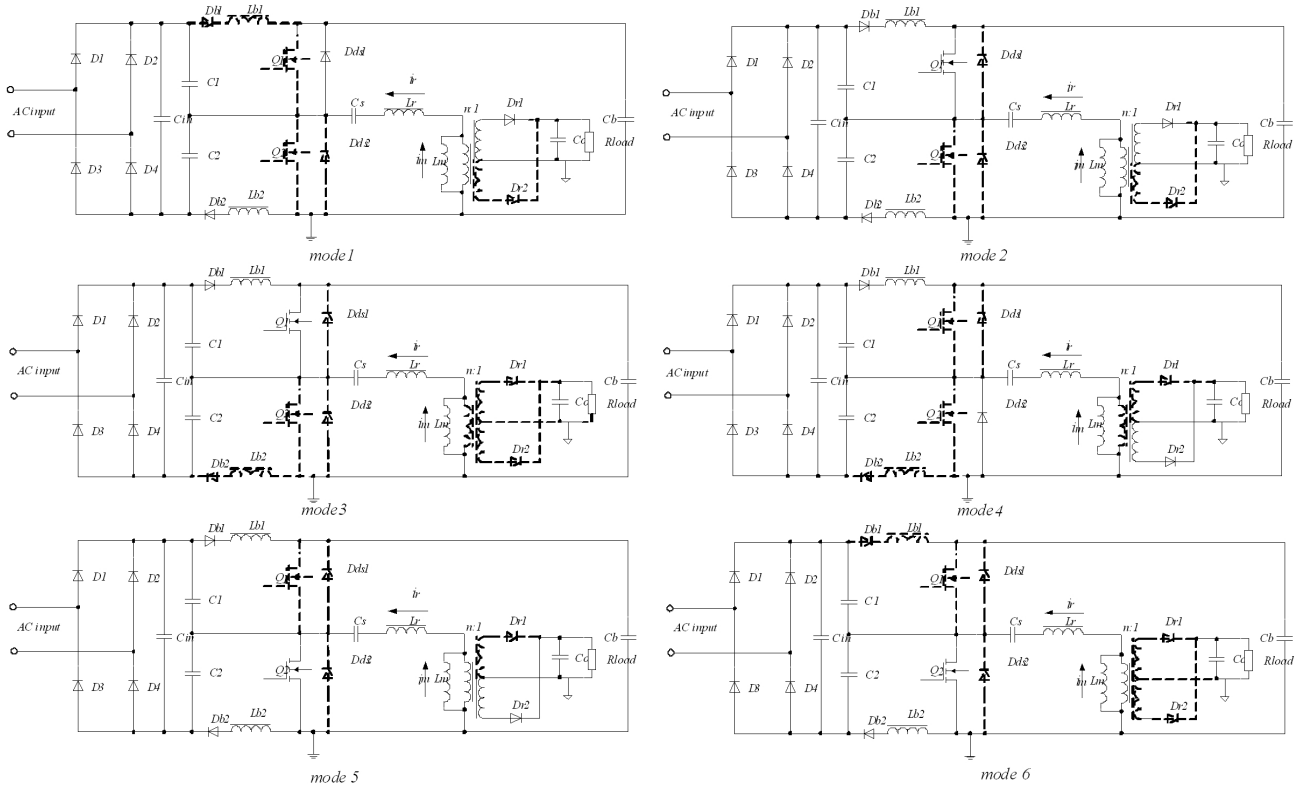


Fig. 2. Operating mode.

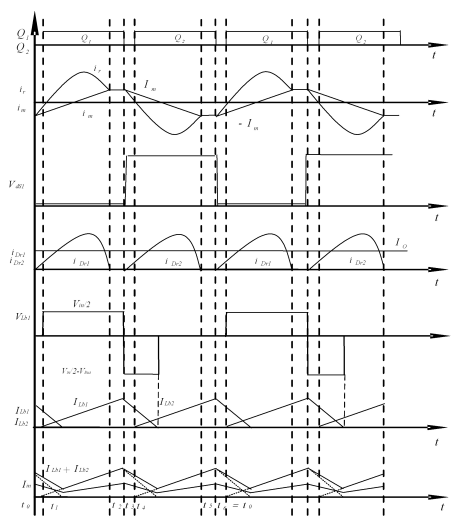


Fig. 3. Key operating waveforms.

A. Interleaved circuit analyses

As Fig. 1 shows, the interleaved circuit used here is made up of two boost circuits which work in the DCM, and its main operating waveforms are shown in Fig. 3. Because the boost circuits work in the DCM, the input current can follow the input current accurately.

From Fig. 3, it is easy to calculate the peak current of L_{b1} and L_{b2} as in the following:

$$I_{peak} = I_{Lb1\_peak} = I_{Lb2\_peak} = \frac{\frac{1}{2}V_{in}}{L_{b1}} \times \frac{1}{2} \times T_s = \frac{V_{in}T_s}{4L_{b1}} \quad (1)$$

where T_s is the switching cycle of the converter.

The discharge time of the inductors L_{b1} and L_{b2} can be calculated in the following equation:

$$T_{dis} = \frac{V_{in}T_s}{2(2V_B - V_{in})}. \quad (2)$$

Therefore, the current of L_{b1} and L_{b2} can be described as:

$$i_{Lb1}(t) = \begin{cases} \dfrac{v_{in}}{2L_{b1}}t, & 0 \le t < \frac{1}{2}T_s \\ \left(\dfrac{T_s}{2} + T_{dis} - t\right)\dfrac{V_B - v_{in}/2}{L_{b1}}, & \frac{1}{2}T_s \le t < \frac{1}{2}T_s + T_{dis} \\ 0, & \frac{1}{2}T_s + T_{dis} \le t < T_s \end{cases} \quad (3a)$$

$$i_{Lb2}(t) = \begin{cases} \dfrac{v_{in}}{2L_{b2}}(t - \dfrac{1}{2}T_s), & \frac{1}{2}T_s \le t < T_s \\ (T_s + T_{dis} - t)\dfrac{V_B - v_{in}/2}{L_{b2}}, & T_s \le t < T_s + T_{dis} \\ 0, & T_s + T_{dis} \le t < \frac{3T_s}{2} \end{cases} \quad (3b)$$

It is obvious that the input current equals $\frac{i_{Lb1}(t)+i_{Lb2}(t)}{2}$, so that the average input current can be descried as:

$$I_{avg} = \frac{1}{T_s}\int_0^{T_s}\left(\frac{i_{Lb1}(t) + i_{Lb2}(t)}{2}\right)dt = \frac{T_s V_B v_{in}}{8L_{b1}(2V_B - v_{in})}. \quad (4)$$

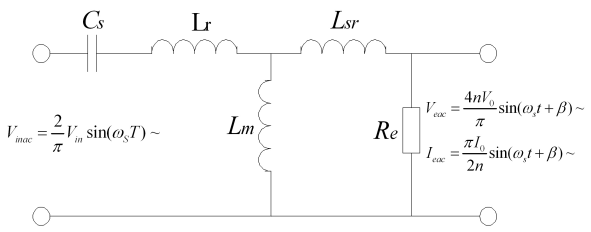


Fig. 4. Equivalent circuit of LLC resonant circuit.

The input power can be obtained as following:

$$P_{in}=\frac{1}{\pi}\int_0^{\pi}I_{avg}v_{in}d\theta=\frac{1}{\pi}\int_0^{\pi}\frac{T_sV_BV_{in}\sin\theta}{8L(2V_B-V_{in}\sin\theta)}V_{in}\sin\theta d\theta$$
$$=\frac{T_sV_{in}^2}{16\pi L_B\alpha^2\sqrt{1-\alpha^2}}(\pi+2arctg(\frac{\alpha}{\sqrt{1-\alpha^2}})-(2\alpha+\pi)\sqrt{1-\alpha^2}) \quad (5)$$

where $\alpha=\frac{V_{in}}{2V_B}$.

B. LLC resonant circuit of the converter

If the working frequency is selected properly, the primary switches of the LLC resonant circuit can work in the ZVS mode while the secondary diodes can work in the ZCS mode, and the efficiency of the system can be improved a great deal. Here we define f_m and f_s as:

$$f_m=\frac{1}{2\pi\sqrt{C_s(L_r+L_m)}} \quad (6)$$

$$f_r=\frac{1}{2\pi\sqrt{C_sL_r}}. \quad (7)$$

If the working frequency satisfies the equation $f_m<f_s<f_r$, then the primary switches of the LCC resonant circuit can work in the ZVS mode, and the secondary diodes can work in the ZCS mode. If $f_s>f_r$, then only the ZVS condition can be satisfied. If $f_s<f_m$, then only the ZCS condition can be satisfied [16]-[20].

Based on the fundamental wave analysis method, the equivalent circuit of the LLC resonant circuit can be obtained as in Fig.4.

V_{inac}: the equivalent AC input voltage of the LLC resonant circuit.

V_{eac}: the equivalent AC output voltage of the LLC resonant circuit.

I_{eac}: the equivalent AC output current of the LLC resonant circuit.

β: the phase shift between the input and the output.

The equivalent resistance $R_e=V_{eac}/I_{eac}=\frac{8n^2}{\pi^2}R_0$, and $R_0=V_0/I_o$. Also the transfer function of the system can be obtained as in equation (8).

$$M=\left|\frac{\frac{4nV_0}{\pi}\sin(\omega_st+\beta)}{\frac{2}{\pi}V_{in}\sin(\omega_st)}\right|=\left|\frac{L_mR_e\omega_s^2C_s}{j\omega_s(1-\frac{\omega_s^2}{\omega_0^2})(L_m+n^2L_{sr})+R_e(1-\frac{\omega_s^2}{\omega_p^2})}\right| \quad (8)$$

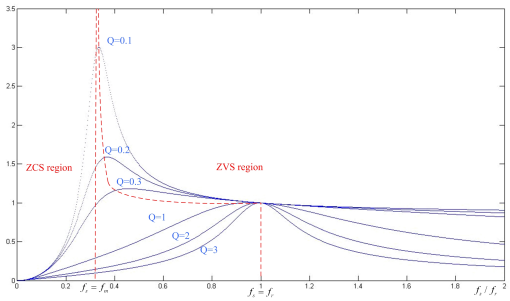


Fig. 5. Voltage gain characteristic of LLC circuit.

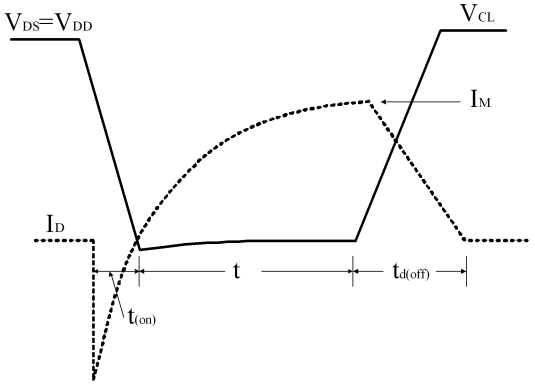


Fig. 6. Switching waveforms of Inductive load inverter.

where:

$$\omega_0=\frac{1}{\sqrt{C_s(L_r+L_m//n^2L_{rs})}} \quad (9)$$

$$\omega_p=\frac{1}{\sqrt{C_s(L_m+L_r)}} \quad (10)$$

Since the leakage inductor of the secondary side is very small, it can be neglected in this analysis.

As a result, the voltage gain of the circuit can be obtained as follows:

$$M=\left|\frac{\frac{4nV_0}{\pi}}{\frac{2}{\pi}V}\right|=\left|\frac{L_mR_e\omega_s^2C_s}{j\omega_sL_m(1-\frac{\omega_s^2}{\omega_r^2})+R_e(1-\frac{\omega_s^2}{\omega_m^2})}\right|=\frac{1}{\sqrt{\left(\frac{L_r\omega_r^2}{L_m\omega_s^2}(\frac{\omega_s^2}{\omega_m^2}-1)\right)^2+\left(\frac{Q\pi^2}{8}(\frac{\omega_s}{\omega_r}-\frac{\omega_r}{\omega_s})\right)^2}} \quad (11)$$

where $Q=\frac{\sqrt{L_r/C_s}}{n^2R_L}$, and the characteristic factor Q is the ratio between the characteristic impedance and the load.

The voltage gain characteristic can be seen in Fig.5 [16]. It is obvious that the ZVS and the ZCS conditions can only be satisfied if $f_m<f<f_s$. The converter works in the boundary of the ZVS and the ZCS region, the LLC resonant circuit has the highest voltage gain, and the system has the highest efficiency.

As in the analysis in the third part of this paper, in mode 2 and mode 4, the magnetizing current keeps increasing until it equals the resonant current. Therefore, the peak current can be obtained as in equation (12), where $T_s$is the working period of the converter.

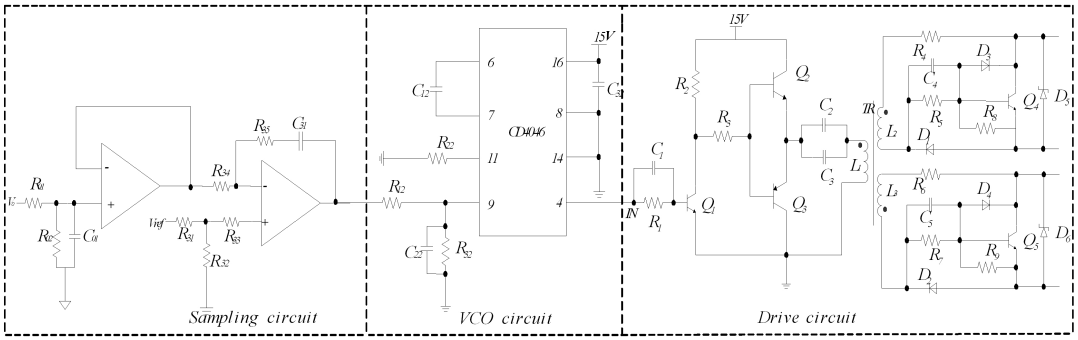


Fig. 7. Control circuit of the converter.

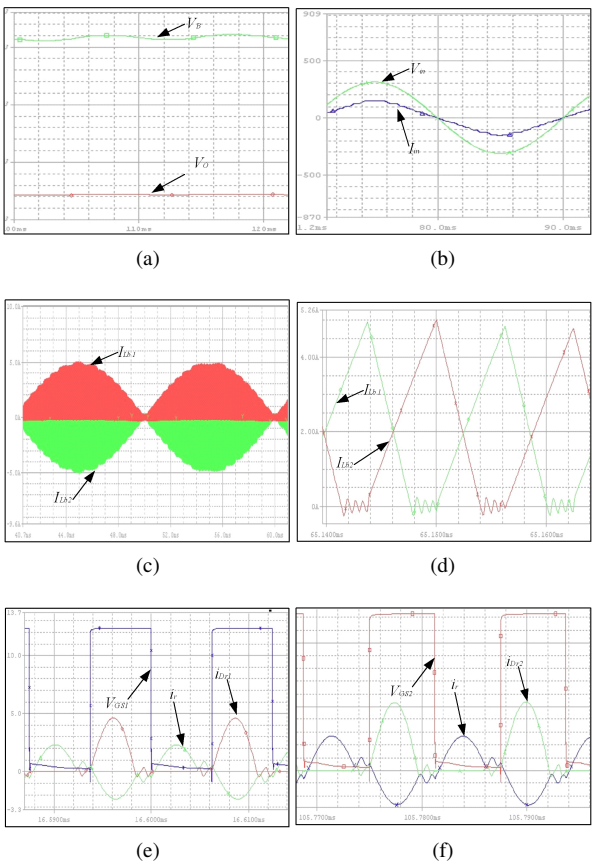


Fig. 8. Simulation results of the converter.

$$I_{peak} = \frac{nV_0}{L_m} \times \frac{T_s}{4} = \frac{nV_0}{4L_m f_s}. \tag{12}$$

Suppose that the converter works with a frequency of f_s, such that the resonant current can be seen as a sinusoidal wave. Here the resonant current can be clarified as:

$$i_r(t) = \sqrt{2} I_{rms} \sin(2\pi f_s + \varphi) \tag{13}$$

where I_{rms} is the root-mean-square value of the resonant circuit, and φ is the phase shift between the resonant tank circuit and the magnetizing inductor current. From Fig. 3, it is obvious that:

$$i_r(0) = \sqrt{2} I_{rms} \sin(2\pi f_s + \varphi) = I_{peak}. \tag{14}$$

The difference between the currents i_r and i_m refers to the energy which transfers from the primary side to the secondary side. As a result, equation (15) can be obtained.

$$\int_0^{\frac{T_s}{2}} (i_r(t) - i_m(t))dt = \frac{V_0}{nR_L} \times \frac{T_s}{2} \tag{15}$$

From the equations (13), (14) and (15), the current can be calculated from equation (16).

$$I_{rms} = \frac{V_0}{8nR_L} \sqrt{\frac{2n^4 R_L^2 T_s^2}{L_m^2} + 8\pi^2}. \tag{16}$$

If the input voltage is higher, the switching frequency will be higher, and I_{rms} will be higher, too. When the input voltage increases, the losses of the converter decrease. As a result, the converter has a high efficiency and a high input voltage, which is different from a traditional PWM converter. In an experiment, where the converter is under a light load, and the bus voltage increases, the LLC circuit chosen here can make the system highly efficiency with a light load.

In mode 3 and mode 6, if we assume that the magnetizing inductor current $i_m(t)$ is constant, and is equals to the I_{peak}, the following equation can be obtained.

$$V_o = \frac{1}{2n} V_{in} + \frac{I_m}{4nC_s} (T_s - T_r). \tag{17}$$

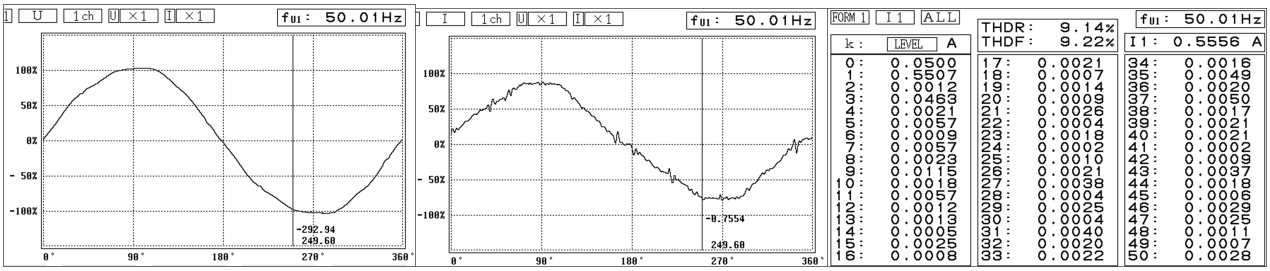
With (12) and (17), the following equation can be obtained:

$$\frac{V_{in}}{2nV_o} = 1 + \frac{\pi^2}{4} \frac{L_s}{L_m} \left(1 - \frac{f_r}{f_s}\right). \tag{18}$$

This equation shows that the ratio of $\frac{L_s}{L_m}$ is very important for the working frequency range and the DC bus voltage range.

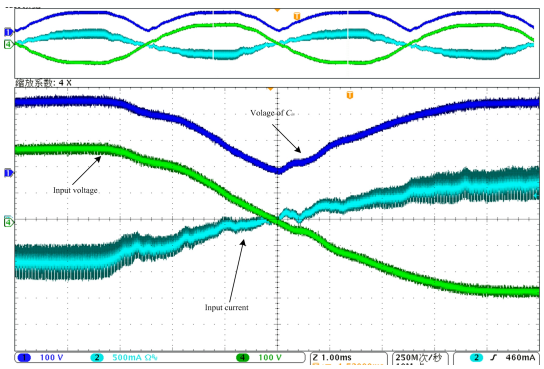
When the switching frequency is equal to the resonant frequency, the resonant current is a pure sine waveform, the output current $(i_{Dr1} + i_{Dr2})$ is critical continuous, and its RMS value is at its minimum. The conduction losses are also at their minimum. As a result, the converter is in the best working condition, and it has the highest efficiency.

If the working frequency is chosen to be the resonant frequency, the converter has the highest efficiency. However, as can be seen in Fig.5, if the working frequency is higher than f_r, the diodes on the secondary sides will lose their soft switching characteristics. Also, the working point must leave some margin in case there is a deviation of the passive

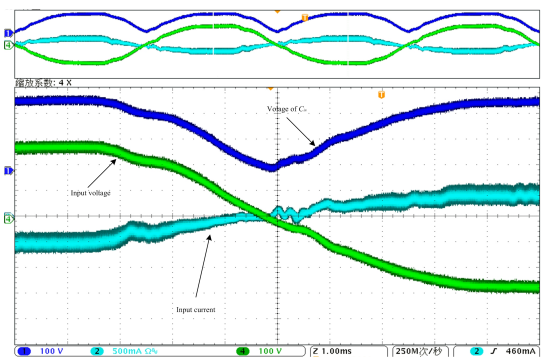


(a) (b) (c)

Fig. 9. Test results of input. (a) Waveform of input voltage. (b) Waveform of input current. (c) Content of harmonics.

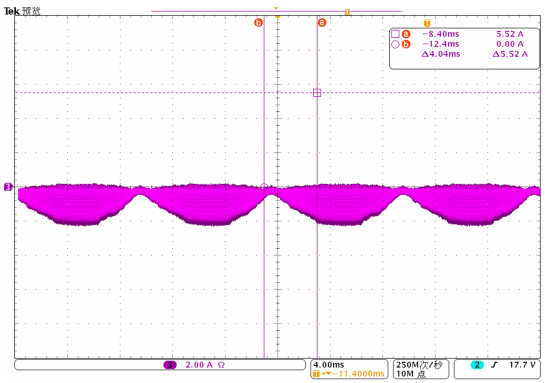


(a) 112W.

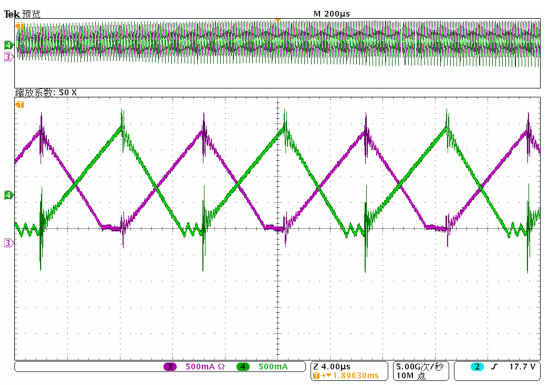


(b) 70W.

Fig. 10. Zero cross current distortion in different loads.



(a)



(b)

Fig. 11. Test results of the inductor current. (a) Envelop waveform of $i_{L_{b1}}$. (b)Waveforms of $i_{L_{b1}}$ and $i_{L_{b2}}$.

components in the system and a fluctuation of the bus voltage. This means the resonant frequency is always chosen to be a little lower than the working frequency.

C. Loss analysis of the power devices

From [21], [22], since the switch is in the ZVS working condition, the power losses in the MOSFET and the inverse diode can be expressed as the sum of the conduction and the switching losses [22].

$$P_M = P_{cM} + P_{swM} = R_{DSon} \cdot I_{Drms}^2 + \frac{V_{in} I_m t_{off} f_s}{6} \tag{19}$$

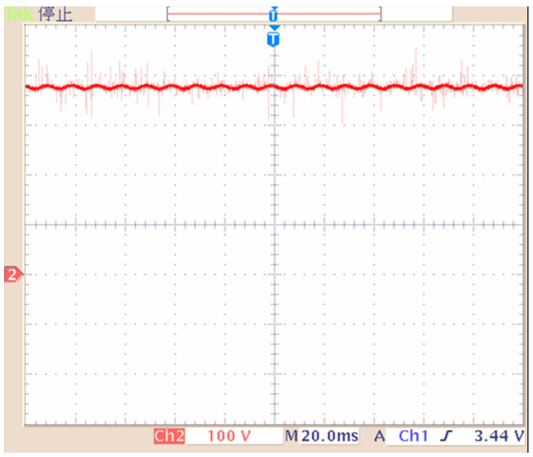
$$P_D = P_{cD} + P_{swD} = u_{D0} \cdot I_{Fav} + R_D \cdot I_{Frms}^2. \tag{20}$$

The ideal switching waveforms for inductive loaded inverters are shown in Fig.6. The integration losses for the FETs can be approximated by calculating the areas of triangles [21]. From (19) and (20), the critical losses of the proposed converter are the conduction losses and the turn-off losses. The conduction losses can be expressed as $P_{cM} = R_{DSon} \cdot I_{Drms}^2$. Here, I_{Drms} is fixed by the rated output power. To reduce the conduction losses of the proposed inverter, it is necessary to reduce the on-resistance (R_{DSon}) of the MOSFETs being used.

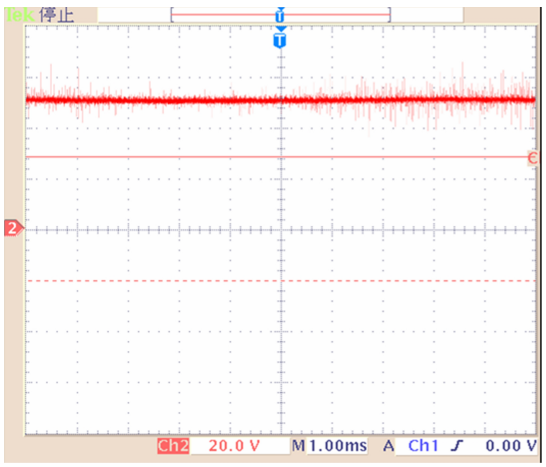
The diodes and Dr_2 work in the ZCS state, the losses of the diodes are only the conduction losses and they can be described as $P_D = I_o V_F$. Here I_o is the output current of the converter, and V_F is the voltage drop of the diode on the secondary side.

III. Design of the Converter

First, some parameters must be given. In the laboratory, a prototype with a 100W rated power and a 52V output is



(a)



(b)

Fig. 12. Test results of output (a) Waveform of the input voltage (b) Waveform of the output voltage.

constructed. From equation (5), the input inductor of the boost circuit can be easily obtained:

$$L_{b1} = L_{b2} = \frac{T_s V_P^2}{16\pi P_{in}\alpha^2\sqrt{1-\alpha^2}}(\pi + 2arctg(\frac{\alpha}{\sqrt{1-\alpha^2}}) - (2\alpha+\pi)\sqrt{1-\alpha^2}). \quad (21)$$

$P_0 = \eta P_{in}$, where P_0 is the output power, and η is the efficiency between the input and the output. The bus voltage is supposed to be 375V under a full load, the input voltage $V_{in} = 220\sqrt{2}\sin\theta$V, and the efficiency is supposed to be 90%. As a result, with calculation, $L_{b1} = L_{b2} = 409uH$.

When the working frequency is equal to the frequency $f_r = {}^1\!/_{2\pi\sqrt{L_r C_s}}$, the converter is at its highest efficiency. When the converter works in this frequency, the gain of the converter is 1, and from equation (11), the turn ration can be easily calculated.

$$M = \left|\frac{\frac{4nV_0}{\pi}}{\frac{2}{\pi}V_B}\right| = 1 \Rightarrow n = \frac{V_B}{2V_0} = \frac{400}{2\times 52} \approx 4. \quad (22)$$

C_s can be seen as a blocking capacitor, and it can supply resonant energy in half a duty cycle of the converter, as shown in the above analysis. Because the average voltage of C_s is half of the bus voltage, the following equation can be obtained:

$$V_{c\max} = nV_o + \frac{I_o T_{\max}}{4nC_s} \quad (23)$$

where $T_{\max}$ is the maximum working frequency of the converter. $V_{c\max}$ is the maximum voltage of C_s, and it can not be higher than the bus voltage. Therefore, the minimum value of C_s can be obtained in the following equation:

$$C_s = \frac{I_o T_{\max}}{4n(V_{c\max} - nV_o)} \Rightarrow C_s > \frac{I_o T_{\max}}{4n(V_B - nV_o)} = 12nF. \quad (24)$$

Because $f_s = \frac{1}{2\pi\sqrt{L_r C_s}}$, and f_s is set to 100kHz, L_r can be obtained, and it is determined that $L_r = 115uH$.

From equation (18), the magnetizing inductor L_m can be easily obtained.

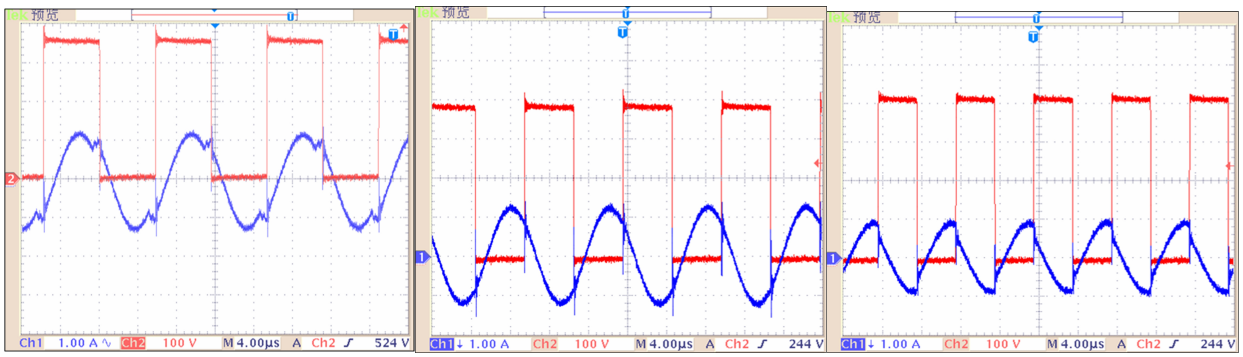
The design parameters for this experiment are shown in Table I.

TABLE I
PARAMETERS OF THE CONVERTER

Components	Symbol	Value	Part name
Boost inductor	L_{b1}, L_{b2}	400uH	
Switches of half bridge converter	Q_1, Q_2		7N60B
Diodes for two boost circuits	D_{r1}, D_{r2}		F8L60
Resonant capacitor	C_s	22nF	
Leakage inductor of the transformer	L_r	115uH	
Magnetizing inductor of the transformer	L_m	600uH	
Input filter	C_{in}	330nF	
Voltage dividers	C_1 ,C_2	220nF	
Output diodes	D_{b1}, D_{b2}		B20100
Rectifier	D_1—D_4		D6KBA80R
Bus capacitor	C_b	330uF	
Output capacitor	C_o	100uF	

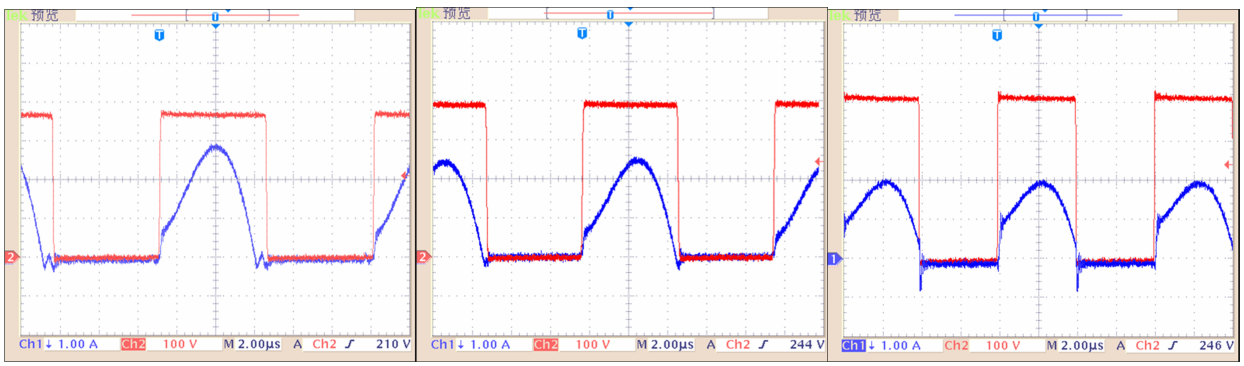
IV. Control Circuit Design

The control circuit is made up of three parts, and they are a sampling circuit, a VCO (voltage control oscillator) circuit and a drive circuit. The sampling circuit is made up of a voltage follower and a PI controller, and the difference between the reference value and the sampling value is the given value of the VCO circuit. The VCO circuit changes the voltage signal into a frequency signal. Here a CD4046 is chosen for the VCO, and the output of the CD4046 is a square wave with nearly a 0.5 duty cycle. Since a half bridge is adopted here, and the drive signal must be isolated, pulse transformers are used. How the drive circuit works is shown above. When the high level part of a PWM signal comes, the top tube of a push-pull circuit will be on, and the primary side of the pulse transformer will have a forward voltage. Therefore, L2 works and supplies the driving signal to the top tube of the half bridge, and L3 does not work because of the blockading function of the diode. The working condition of the negative half-cycle signal has the



(a) (b) (c)

Fig. 13. Waveforms of V_{DS2} and i_{Cs}. (a) 112W input. (b) 100W input. (c) 90W input.



(a) (b) (c)

Fig. 14. Waveforms of V_{DS2} and i_{Dr1}. (a) 112W input. (b) 100W input. (c) 90W input.

same theory, stabilivolts are designed to supply a stable 15V signal. R4 and R6 are used to control the length of the dead time for the half bridge. If the ohm value is larger, then the dead time increases as the charging time increases. As a result, the dead time can be adjusted freely. Q4 and Q5 are used to draw current from the power switches of the half bridge.

V. Simulation Results

Here PSpice was used to simulate the proposed converter. Fig. 8 shows the simulation results of the converter. As can be seen in Fig. 8(a), the bus voltage V_B, which has about a 5V ripple is 375V, and the output voltage is 52V. Fig. 8(b) shows that the input current shapes with the input voltage accurately, which means that the converter has a very high power factor. Fig. 8(c) shows the current of L_{b1} and L_{b2}, and it is obvious that the boost circuits work in the DCM. Fig. 8(d) is the envelop waveform of Fig. 8(c) which tests in the peak input voltage. As can be seen, the two inductors work with a 180 degree phase shift. Fig. 8(e) and Fig. 8(f) show the simulation results of the LLC resonant converter. As can be seen, the rectifier diodes of the output are turned off after their currents reach zero. Therefore, it is obvious that both of the output rectifier diodes work in the ZCS state.

VI. Experimental Results

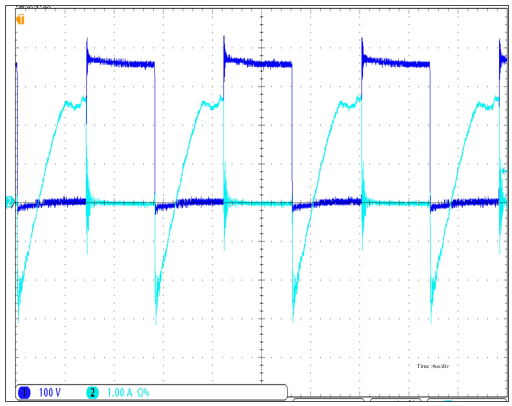
Fig. 9(a) and Fig. 9(b) show the waveforms of the input voltage and current tested by a HIOKI 3193 POWER HITESTER. As can be seen, the input current shapes with the input voltage, which shows that a high power factor has been attained. Fig. 9(c) shows the content of the input current, and the test results agree with the IEEE 519 and IEC 61000-3-2 standards.

The zero cross current distortion phenomenon influences the power factor of the system. The zero cross current distortion phenomenon is caused by C_{in} . When the voltage of C_{in} is higher than the input voltage, the input current is zero. Even if the voltage of C_{in} is zero, the positive direction conduction pressure drop of the bridge rectifier will still make the input current zero. Therefore, the zero current distortion phenomenon always exists. When the load is lower, the voltage of C_{in} is higher, and the zero current distortion phenomenon is more obvious.

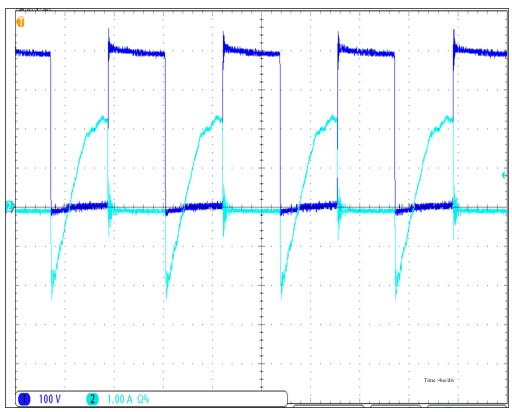
Fig. 10 shows the test results of the zero cross current distortion with 112W and 70W loads. It is evident that when the load is lower, the time of the input current keeping zero is longer.

Fig. 11(a) and Fig. 11(b) show the waveforms of $i_{L_{b1}}$ and $i_{L_{b2}}$, and it is obvious that both L_{b1} and L_{b2} work in the DCM, which ensures that the circuit has a natural PFC function. It can also be seen that the two inductors work with a 180 degree phase shift and that the two boost circuits work in the interleaving mode.

Fig. 12(a) shows the waveform of V_B. Its RMS value is 375V with a 5V ripple, and the vibration frequency of V_B is 100Hz. Since the RMS value of the input voltage is 220V,



(a)



(b)

Fig. 15. Waveforms of V_{DS1} and I_{Ds1}(a) 112W input (b) 90W input.

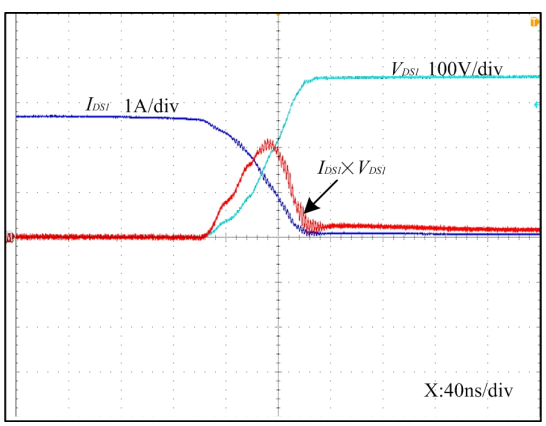


Fig. 16. Waveforms of V_{DS1} and I_{Ds1}at turn off time.

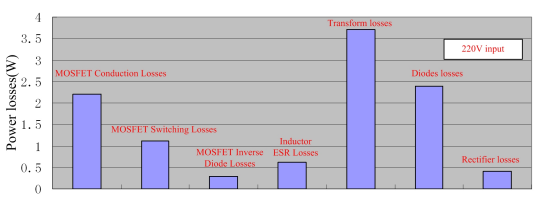


Fig. 17. Power-loss distribution of the studied converter.

the peak value of the input voltage is 311V. It is obvious that the bus voltage V_B is only a little larger than the peak value of the input voltage, which decreases the voltage stress of the switches a great deal. Fig. 12(b) shows the output voltage of the converter. The RMS value of V_0 is 52V with a 1V ripple.

Fig. 13 shows the waveforms of V_{DS2} and i_{Cs} with different input powers, Fig. 13(a) shows the waveforms of V_{DS2} and i_{Cs} with a full load and a 90 kHz working frequency. At this time, the bus voltage is 375V. Since the secondary diodes work in the ZCS mode, the primary current is not sinusoidal and has a step which proves the description in section II Fig. 13 (c) shows the waveforms of V_{DS2} and i_{Cs} with a 90W input power and a 125 kHz working frequency. At this time, the secondary diodes are no longer in the ZCS mode, and i_{Cs} is not sinusoidal. It is obvious from Fig. 13(a)-(c) that the bus voltage increases with the working frequency.

To test the ZCS characteristics of the diodes on the secondary side of the LLC circuit, the waveforms of V_{DS2} and i_{Dr1} are shown in Fig. 14. In Fig. 14(a), there is a short time i_{Dr1} keeping zero in one half a switching cycle, so the diodes on the secondary side work in the ZCS mode. In Fig. 14(b), the diode is turned off when the current of D_{r1} reaches zero and the diodes on the secondary side still work in the ZCS mode, which is a critical point. As is shown in Fig. 14(c), as the working frequency increases, the diodes on the secondary side have lost the ZCS characteristic. Therefore, it is evident that the diodes on the secondary side of the LLC circuit lose their ZCS characteristics under a light load. As we know from Fig.5, the switches on the primary side still have the ZVS characteristics with a decreasing load.

Fig. 15 shows the waveforms of V_{DS1} and I_{Ds1}. From Fig. 5, it is known that the switches of the converter are always satisfied with the ZVS condition. As a result, the switches are turned on in the ZVS state. In this experiment, V_{DS1} and I_{Ds1} are tested, and it is evident that, S_1 is in the ZVS state with a load ranging from 112W to 90W.

The switching losses of the switches are only the turn-off losses, because the switches are in the ZVS working condition. Fig.16 shows the waveforms of V_{DS1} and I_{Ds1} at the turn-off time, which shows the existence of the turn-off losses.

The power loss distribution of the proposed converter under full-load operation is measured and shown in Fig.17 to highlight the key features of the topology under study.

Fig.18 shows the load characteristics of the converter. It is obvious that the power factor is always larger than 0.96 within a 45%∼100% load. The THD is always lower than 10% within a 45%∼100% load. The PF and the THD satisfy the IEEE 519 and IEC 61000-3-2 standards. The efficiency is from 0.872 to 0.9025, and the converter achieves maximum efficiency with a full load. As the load decreases, the bus voltage ranges from 375V to 491V.

Fig. 19 shows the converter characteristics with an input voltage ranging from 180V to 260V with a full load. The power factor is always larger than 0.97, the THD is always within 10% , the bus voltage ranges from 262V to 435V, and the efficiency ranges from 62.89kHz to 130.4kHz, with an input voltage ranging from 180V to 260V under full load.

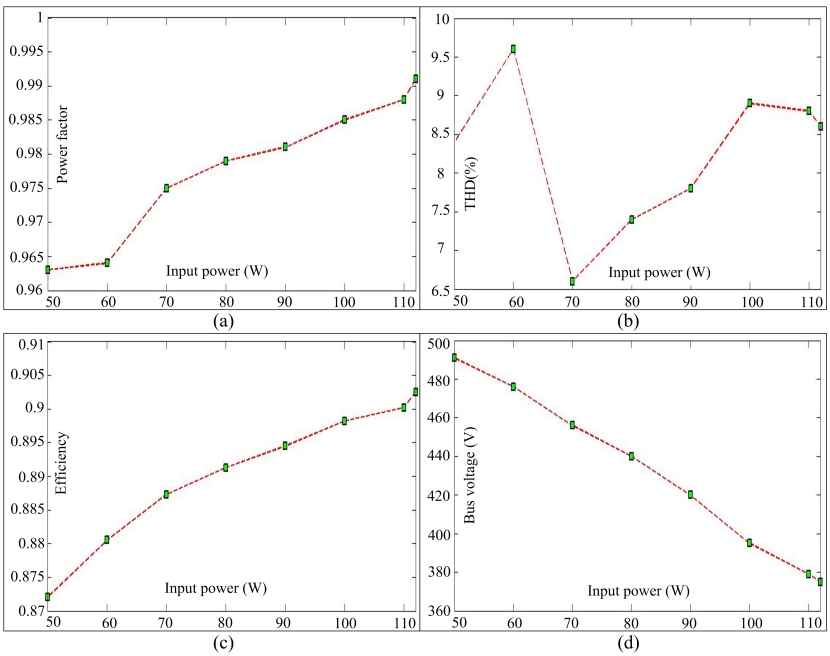


Fig. 18. Load characteristics.

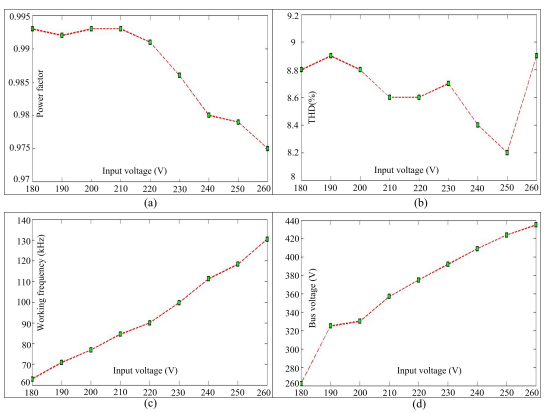


Fig. 19. Converter characteristics with input voltage range (100% load).

VII. Conclusion

A single stage AC/DC converter based on interleaving technology and an LLC resonant network is proposed here. Since an interleaving cell is adopted, the bus voltage can be a little more than the peak value of the input voltage, and the converter is suitable for both low line input and high line input. Since an LLC resonant network is adopted here, the primary switches can work in the ZVS mode while the secondary diodes can work in the ZCS mode, which increases the efficiency of the system. Simulations are done to analyze the circuit. A 100W prototype is studied in the laboratory. In the experiments, the efficiency is as high as 90.25 %, the PF is as high as 0.99, the THD is within 10%, and the working mode is in agreement with the simulation.

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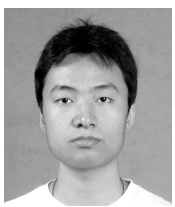

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