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Novel Passive Snubber Suitable for Three-Phase Single-Stage PFC Based on an Isolated Full-Bridge Boost Topology

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Abstract

In this paper a novel passive snubber is proposed, which can suppress the voltage spike across the bridge leg of the isolated full-bridge boost topology. The snubber is composed of capacitors, inductors and diodes. Two capacitors connected in series are used to absorb the voltage spike and the energy of each capacitor can be transferred to the load during one switching cycle by the resonance of the inductors and capacitors. The operational principle of the passive snubber is analyzed in detail based on a three-phase power factor correction (PFC) converter, and the design considerations of both the converter and the snubber are given. Finally, a 3kW laboratory-made prototype is built. The experimental results verify the theoretical analysis and evaluations. They also prove the validity and feasibility of the proposed methods.

Key Words: Isolated full-bridge boost topology, Passive, Snubber, Three-phase power factor correction (PFC), Voltage spike

I. INTRODUCTION

Power factor correction (PFC) is one of the most effective methods for reducing harmonic current and increasing power factor [1]–[4]. Based on their circuit structures, PFC techniques are usually divided into two categories: two-stage and single-stage approaches. The first stage of the two-stage approach is a PFC circuit and the second stage is a DC/DC converter. As a result of these two processing stages, conversion efficiency is reduced and an extra PFC stage adds both components and complexity. The single-stage approach can overcome these drawbacks. This approach uses only one stage circuit to achieve both PFC and DC/DC conversion, and it has the advantages such as high efficiency, simplicity and low cost [5]–[8]. Therefore, single-stage PFC is an important developing orientation of PFC techniques [9], [10].

The isolated full-bridge boost topology is attractive in applications such as isolated DC/DC converters, as well as single-phase and three-phase single-stage PFC. This is due to the fact that it can: 1) realize electrical isolation between the input and output sides and the output voltage regulation, 2) achieve soft-switching for all of the switches, and 3) avoid the short-through problem of bridge leg switches [11]–[14]. However, the topology itself has a serious problem. Due to the existence of the transformer leakage inductance, there is a voltage spike across the bridge leg, which will increase the voltage stress on each of the switches and decrease the reliability of the topology [15], [16].

To suppress the voltage spike, a number of techniques have been proposed. A method based on the active clamping technique is introduced in [17]–[20], a passive clamping technique is proposed in [21] and a passive snubber is investigated in [22], [23]. The voltage spike is efficiently suppressed after the adoption of each of the above methods. However, all of them have their own drawbacks. 1) For the first method, an additional switch is introduced, which increases the complexity of control circuit and reduces the reliability of the whole system, moreover, the switching frequency of the additional switch is two times as high as that of the main switches, so it is difficult to choose the additional switch. 2) For the second method, the problem of magnetic bias of the power transformer appears after the adoption of the passive clamping circuit. 3) For the third method, a diode is connected in series with the bridge leg switches, which increases some of the losses and reduces the efficiency of the converter.

In this paper, a novel passive snubber is proposed, and its investigation is based on a three-phase single-stage PFC converter. Theoretical analysis and experimental results show that the voltage spike can be suppressed efficiently after the adoption of the snubber which can also overcome the drawbacks of the methods in [17]–[23].

II. OPERATIONAL PRINCIPLE

A three-phase single-stage PFC converter based on an isolated full-bridge boost topology is shown in Fig. 1, where

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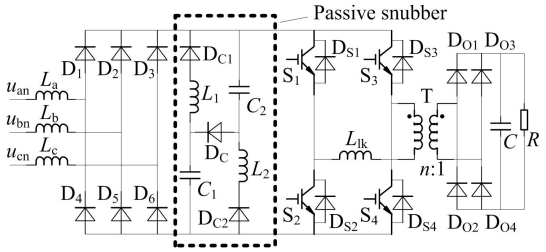


Fig. 1. Three-phase single-stage PFC converter based on isolated full-bridge boost topology.

the passive snubber proposed in this paper is composed of C_1, C_2 ($C_1 = C_2$), L_1, L_2 ($L_1 = L_2$), D_{C1}, D_{C2} and D_C. The PFC converter is mainly made up of six parts: a three-phase input AC source u_{an}, u_{bn} and u_{cn}, an input rectifier, a passive snubber, a phase shift full bridge (PSFB), a high frequency transformer, an output rectifier and a filter. L_a, L_b, L_c ($L_a = L_b = L_c = L$) are the boost inductors. The PSFB is the main part of the converter, where the duty cycle of each switch is fixed at 50%, the switching states of S_1 & S_2 are contrary to those of S_3 & S_4 and the switching phase between S_1 and S_2, S_3 and S_4 can be controlled to regulate the output voltage. D_{S1}-D_{S4} are the body diodes of the switches S_1-S_4, L_{lk} and n are the equivalent leakage inductance and the voltage ratio of transformer T, respectively.

The converter in Fig. 1 operates in discontinuous current mode (DCM). When the bridge leg switches are shorted (S_1 & S_2 or S_3 & S_4 are turning on), the boost inductors are charged by u_{an}, u_{bn} and u_{cn}, and the input current increases almost linearly. When the bridge diagonal-leg switches turn on (S_1 & S_4 or S_2 & S_3 are turning on), the output current is provided by u_{an}, u_{bn} and u_{cn} and L_a, L_b and L_c, and the input current decreases. It can be seen that the process above is repeated periodically. The discontinuous input current follows the envelopes which are proportional to the input voltage. Therefore, both PFC and AC/DC conversion can be achieved.

To simplify the analysis, we assumed that: 1) all devices are ideal, 2) the capacitor C is large enough, so the output voltage U_o can be considered as a constant value, and 3) during one switching period, the changes in u_{an}, u_{bn} and u_{cn} are negligible because the switching period is much shorter than the line period. The following analysis is during one charging period of the boost inductors in the time phase of $0 \le \omega t \le \pi/6$, in which the relation of the three-phase voltage is $u_{bn} \le 0 \le u_{an} \le u_{cn}$. The theoretical waveforms and the equivalent circuits of different stages are shown in Fig.2 and Fig.3, respectively.

Stage 1 (before t_0): S_2 and S_3 are turning on, while S_1 and S_4 are turning off. The converter operates in DCM, so the current of the boost inductors has been reduced to zero before t_0, and then the current in both the primary and secondary sides of transformer T is zero. The voltage across the primary side of transformer T: $U_k = nU_o$, $U_{C1} = U_{C2} = nU_o/2$, $U_{S1} = U_{S4} = nU_o$ and $U_{S2} = U_{S3} = 0$. The diodes D_{S1}-D_{S4} are all turning off. In this stage, the output current is only provided by capacitor C.

Stage 2 (t_0–t_1): At t_0, S_1 turns on with a zero current, and S_3 turns off with a zero voltage and current. The diodes D_1, D_3 and D_5 are turned on, and the current of the boost inductors i_{La}, i_{Lb} and i_{Lc} increases linearly. In the snubber circuit, C_1

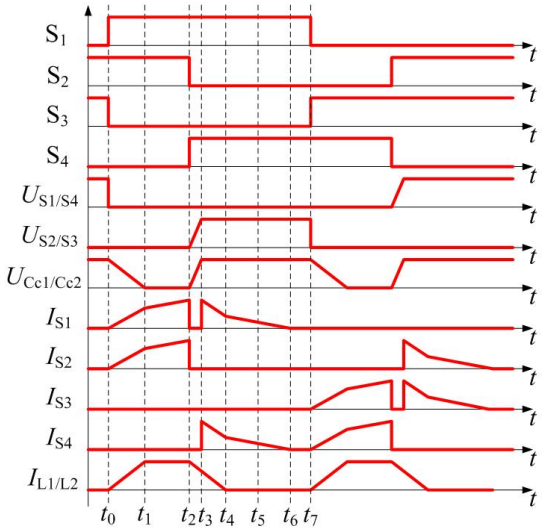


Fig. 2. Theoretical waveforms.

is resonant with L_1 through D_{C1}, S_1 and S_2. Furthermore, C_2 is resonant with L_2 through S_1, S_2 and D_{C2}. Therefore, the voltage of C_1 & C_2 and the current in L_1 & L_2 are:

$$u_{C1/C2}(t) = \frac{1}{2} n U_o \cos \frac{1}{\sqrt{L_1 C_1}} (t - t_0) \tag{1}$$

$$i_{L1/L2}(t) = \frac{nU_o}{2} \sqrt{\frac{C_1}{L_1}} \sin \frac{1}{\sqrt{L_1 C_1}} (t - t_0). \tag{2}$$

At t_1, $U_{C1} = U_{C2} = 0$, and the energy of C_1 and C_2 is transferred to L_1 and L_2 entirely. In this stage, the output current is only provided by capacitor C. The duration of this stage is calculated as:

$$t_{01} = \frac{\pi}{2} \sqrt{L_1 C_1}. \tag{3}$$

Stage 3 (t_1–t_2): In this stage, i_{La}, i_{Lb} and i_{Lc} still increase linearly, and the output current is also provided by capacitor C alone. The voltage of C_1 or C_2 is zero, so diode D_C is turned on, L_1 is connected in series with L_2, and their current flows through D_{C1}, S_1, S_2, D_{C2} and D_C.

Stage 4 (t_2–t_3): At t_2, S_2 turns off, and S_4 turns on with a zero voltage. C_1 and C_2 are charged by L_a, L_b, L_c, L_1 and L_2. The voltage across the bridge leg increases from zero, so S_2 turns off with a zero voltage. The inductance of each boost inductor is large enough, so that the change in their current can be ignored during this small charging period. The voltage expression of C_1 or C_2 is given in (4):

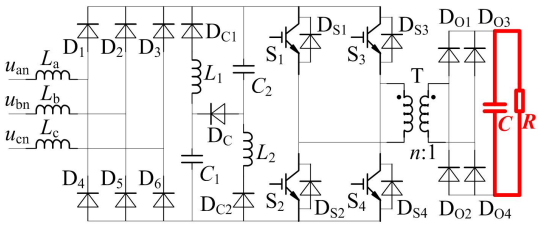
$$u_{C1/C2}(t) = \frac{I_{L1/L2peak} - I_{Lbpeak}}{C_1} (t - t_2) \tag{4}$$

$$I_{L1/L2peak} = \frac{nU_o}{2} \sqrt{\frac{C_1}{L_1}} \tag{5}$$

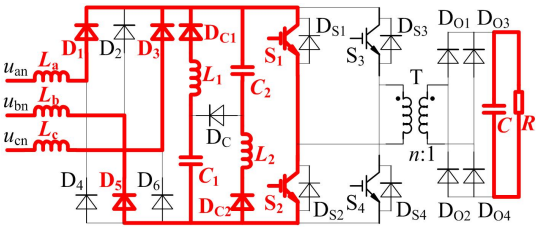
$$I_{Lbpeak} = \frac{u_{bn}}{L} DT \tag{6}$$

where, T is the charging period of the boost inductors, and $D = (t_2 - t_0)/T$ is the duty cycle of the converter.

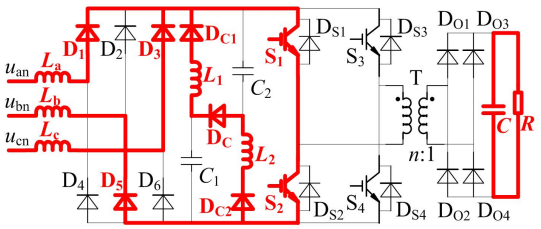
At t_3, the charging process of C_1 and C_2 is over. Therefore, $U_k = -nU_o$, $U_{C1} = U_{C2} = nU_o/2$, $U_{S1} = U_{S4} = 0$ and $U_{S2} =$



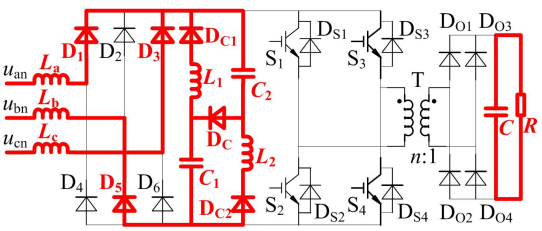
(a) Stage 1 and stage 8.



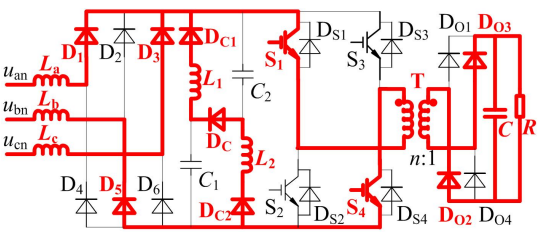
(b) Stage 2.



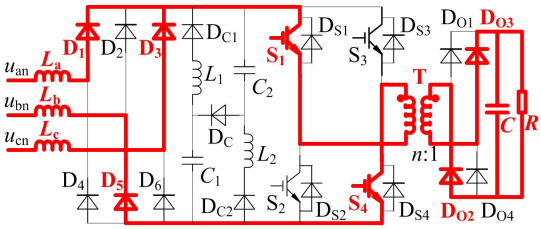
(c) Stage 3.



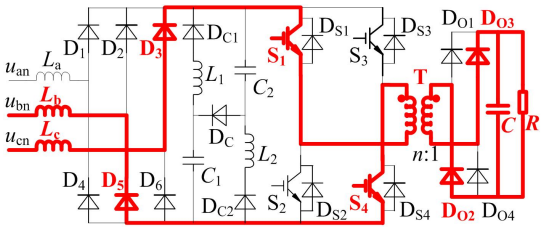
(d) Stage 4.



(e) Stage 5.



(f) Stage 6.



(g) Stage 7.

Fig. 3. Equivalent circuit of each stage.

$U_{S3} = nU_o$. In this stage, the output current is only provided by capacitor C. The duration of this stage is calculated as:

$$t_{23} = \frac{nU_oC_1}{2(I_{L1/L2peak} - I_{Lbpeak})}. \quad (7)$$

Stage 5 (t_3–t_4): In this stage, the current of L_a, L_b, L_c, L_1 and L_2 flows through S_1, S_4 and transformer T to the load, and then it begins to decrease. On the secondary side of transformer T, D_{O2} and D_{O3} turn on. In this stage, the expression of i_{L1} and i_{L2} is:

$$i_{L1/L2}(t) = I_{L1/L2peak} - \frac{nU_o}{2L_1}(t - t_3). \quad (8)$$

At t_4, i_{L1} and i_{L2} reduce to zero, so that the duration of this stage is calculated as:

$$t_{34} = \sqrt{L_1C_1}. \quad (9)$$

Stage 6 (t_4–t_5): In this stage, i_{La}, i_{Lb} and i_{Lc} still decrease. At t_5, i_{La} reduces to zero, and D_1 turns off.

Stage 7 (t_5–t_6): In this stage, i_{Lb} and i_{Lc} still decrease. At t_6, i_{Lb} and i_{Lc} reduces to zero, and D_3, D_5, D_{O2} and D_{O3} turn off.

Stage 8 (t_6–t_7): The equivalent circuit of this stage is the same as that of stage 1. The current on the primary side of the transformer is zero and the output current is only provided by capacitor C.

In the analysis above, it is assumed that u_{an} is large enough that i_{La} reduces to zero after i_{L1} (or i_{L2}). If u_{an} is not large enough, i_{La} will reduce to zero before i_{L1} (or i_{L2}). After t_7, the converter operates in another charging period of the boost inductors, and the switching states between S_1 & S_3 and between S_2 & S_4 are exchanged.

III. Design Considerations

A. Voltage stress of switches S_1~S_4

From the analysis above, it can be seen that when the bridge diagonal-leg switches turn on, the voltage across the bridge is equal to that across the primary side of the transformer (U_k). It is known that under ideal conditions $U_k = nU_o$. However, under real conditions, the voltage inducted by the leakage inductance of the transformer (L_{lk}) must be considered.

At t_2, the bridge diagonal-leg switches turn on. At this moment, the current of the boost inductors increases to the maximum value of one charging cycle, and the boost inductors begins to discharge though the load. The equivalent circuit at this moment is shown in Fig. 4, where $C_C = C_1/2$.

At t_2, $U_{Cc} = 0$, $i_{Llk} = 0$, $i_{Cc} = -i_{Lb}$, and the voltage of C_C begins to increase. The time t_S is defined here. At t_S, the voltage of C_C is increased to nU_o, that is $U_{Cc}(t_S) = nU_o$. As a result, after t_S, i_{Llk} increases, i_{Cc} decreases, and the voltage of C_C continues to increase. The decrease in current $-i_{Lb}$ can

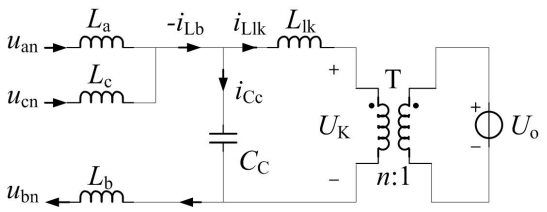


Fig. 4. Equivalent circuit.

be ignored at this point. Therefore, after t_S the following is obtained:

$$i_{\mathrm{Cc}}(t-t_{\mathrm{S}})+i_{\mathrm{Llk}}(t-t_{\mathrm{S}})=-i_{\mathrm{Lb}} \tag{10}$$

$$i_{\mathrm{Cc}}(t-t_{\mathrm{S}})=C_{\mathrm{C}}\frac{\mathrm{d}\Delta u_{\mathrm{Cc}}(t-t_{\mathrm{S}})}{\mathrm{d}t} \tag{11}$$

$$\Delta u_{\mathrm{Cc}}(t-t_{\mathrm{S}})=L_{\mathrm{lk}}\frac{\mathrm{d}i_{\mathrm{Llk}}(t-t_{\mathrm{S}})}{\mathrm{d}t} \tag{12}$$

where, $\Delta u_{\mathrm{Cc}}(t-t_{\mathrm{S}})$ is the increasing value of the voltage of C_C after t_S.

From (10), (11) and (12), the following differential equation is obtained:

$$\Delta u_{\mathrm{Cc}}(t-t_{\mathrm{S}})+L_{\mathrm{lk}}C_{\mathrm{C}}\frac{\mathrm{d}^2\Delta u_{\mathrm{Cc}}(t-t_{\mathrm{S}})}{\mathrm{d}t^2}=0. \tag{13}$$

This equation (13) has the following initial data:

$$\Delta u_{\mathrm{Cc}}(t_{\mathrm{S}})=0 \tag{14}$$

$$i_{\mathrm{Cc}}(t_{\mathrm{S}})=-i_{\mathrm{Lb}} \tag{15}$$

$$i_{\mathrm{Llk}}(t_{\mathrm{S}})=0. \tag{16}$$

As a result, the solution of (13) is:

$$\Delta u_{\mathrm{Cc}}(t-t_{\mathrm{S}})=-i_{\mathrm{Lb}}\sqrt{\frac{2L_{\mathrm{lk}}}{C_1}}\sin\frac{\sqrt{2}t}{\sqrt{L_{\mathrm{lk}}C_1}} \tag{17}$$

Therefore, the voltage of the four switches can be obtained as follows:

$$U_{\mathrm{S}}=nU_{\mathrm{o}}-i_{\mathrm{Lb}}(t)\sqrt{\frac{2L_{\mathrm{lk}}}{C_1}}\sin\frac{\sqrt{2}t}{\sqrt{L_{\mathrm{lk}}C_1}}. \tag{18}$$

B. Design issue of the passive snubber

From (18), the relationship between U_S and C_1 can be obtained as in Fig. 5. It can be see that U_S will decrease as C_1 increases. If the voltage spike (the latter item of (18)) is limited to within 20% nU_o, then C_1 must be larger than C_{11}, C_{12} and C_{13} ($C_{11}<C_{12}<C_{13}$) for different leakage inductances L_{lk1}, L_{lk2} and L_{lk3} ($L_{lk1}<L_{lk2}<L_{lk3}$).

When the bridge diagonal-leg switches turn on, the voltage of C_1 (or C_2) is $U_S/2$ (the voltage inducted by the leakage inductance is considered here). If the voltage spike is limited within $20\%nU_o$, the following is obtained:

$$U_{\mathrm{S}}/2\le 0.6nU_{\mathrm{o}}. \tag{19}$$

From (19), it is known that during the phase when the bridge diagonal-leg switches turn on, the voltage of C_1 (or C_2) is lower than nU_o. When the bridge leg switches are shorted, the voltage of C_1 and C_2 begins to decrease. The operational

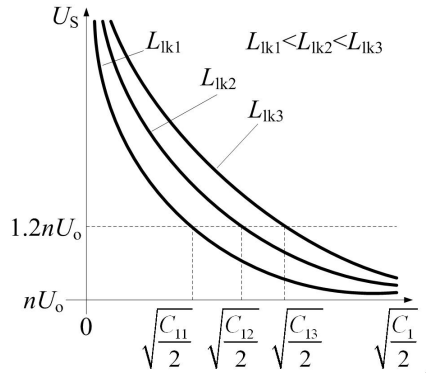


Fig. 5. Relationship between U_S and C_1.

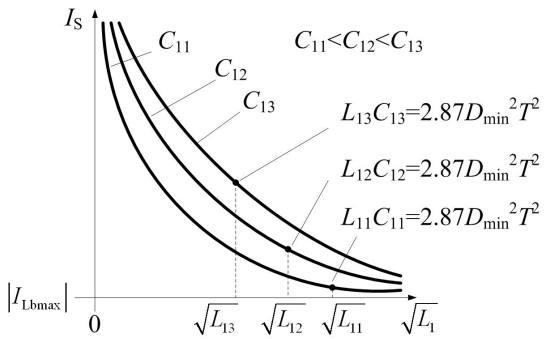


Fig. 6. Relationship between I_S and L_1.

analysis above is under the condition where the converter is operating with a full load. As a result, the voltages of C_1 and C_2 reach to zero at the end of the phase when the bridge leg switches are shorted. On the other hand, if the converter was operating with a light load (under the minimum duty cycle D_{min}), the voltages of C_1 and C_2 can not reach to zero during that phase. To avoid over-voltage on the bridge leg after several charging periods, the voltages of C_1 and C_2 must be lower than $nU_o/2$ at the end of the phase when the bridge leg switches are shorted. As a result the following is obtained:

$$\sqrt{L_1C_1}\arccos\frac{5}{6}\le D_{\mathrm{min}}T. \tag{20}$$

It is equal to:

$$L_1C_1\le 2.87D_{\mathrm{min}}^2T^2. \tag{21}$$

From the above analysis, the current stresses of the four switches can be obtained:

$$I_{\mathrm{S}}=|I_{\mathrm{Lbmax}}|+2I_{\mathrm{L1/L2peak}}=|I_{\mathrm{Lbmax}}|+nU_{\mathrm{o}}\sqrt{\frac{C_1}{L_1}}. \tag{22}$$

From (22), the relationship between I_S and L_1 can be obtained in as in Fig. 6. It can be seen that I_S increases as C_1 increases, and that it will decrease as L_1 increases. It can also be seen that to meet (20), L_1 must be lower than L_{11}, L_{12} and L_{13} ($L_{11}>L_{12}>L_{13}$) for the different capacitances C_{11}, C_{12} and C_{13} ($C_{11}<C_{12}<C_{13}$).

IV. Experimental Results

To verify the theoretical analysis and evaluations mentioned earlier, a 3kW laboratory-made prototype of this converter was built. The basic circuit parameters and the main components

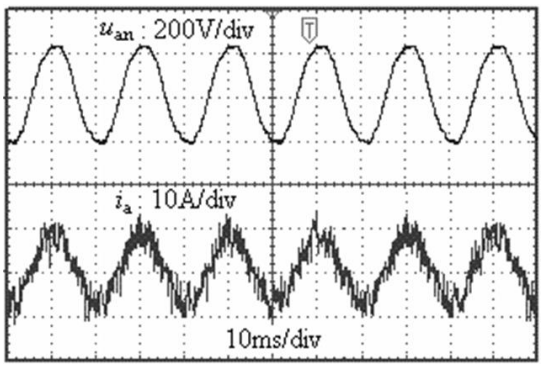


Fig. 7. Input voltage and current of phase A.

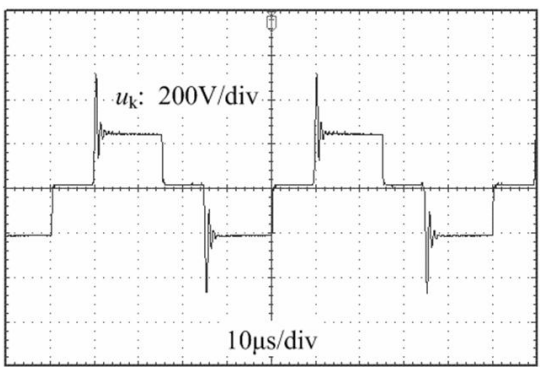


Fig. 8. Voltage across primary side of T without the snubber.

used in this prototype are: $L_a = L_b = L_c = 76\mu$H, $L_1 = L_2 = 150\mu$H, $L_{lk} = 6\mu$H, $C_1 = C_2 = 100$nF, $C = 1000\mu$F, $n = 2$, S_1-S_4: EUPEC BSM75GB120DN2 (the switching frequency is 20kHz).

Fig. 7 shows the input waveforms of phase A, and the current waveform is when a simple LC low-pass filter is introduced. We can see that the input current is sinusoidal and follows the input voltage.

Fig. 8 and Fig. 9 are the voltage waveforms across the primary side of T. To protect the circuit, the experimental result in Fig. 8 is obtained at a very low voltage, and the voltage spike is much smaller than that produced at full load (3kW). The result in Fig. 9 is obtained at full load. We can see that the voltage spike is suppressed greatly after the passive snubber is adopted.

Fig. 10 to 12 show the experimental waveforms of the switches S_1 and S_2 at full load. It can be seen that S_1 achieves ZCS and turns off with a zero voltage, and S_2 achieves ZVS (the switching states of S_3 and S_4 are the same as those of S_1 and S_2, so the related results are not presented here). Fig. 13 gives the voltage waveforms of C_1, which show the charging and discharging processes of C_1.

The experimental efficiency curve is drawn in Fig. 14. As can be seen the prototype converter shows good performance in conversion efficiency, especially under full load (3kW). Compared with other methods it can bee seen that: 1) the efficiency of this snubber is higher than that of a traditional RCD snubber and the passive snubbers in [22], [23], 2) the efficiency of this snubber is similar to that of the active clamping circuits in [17]–[20] and the passive clamping circuit in [21], while the reliability is much higher.

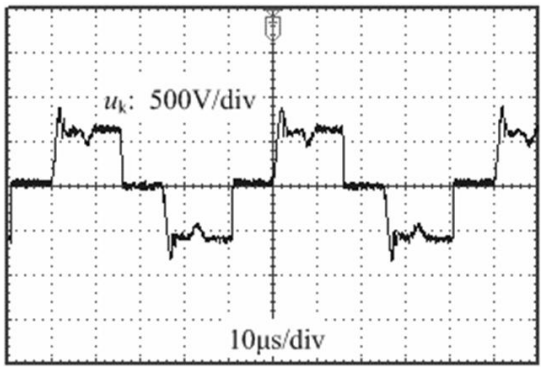


Fig. 9. Voltage across primary side of T with the snubber.

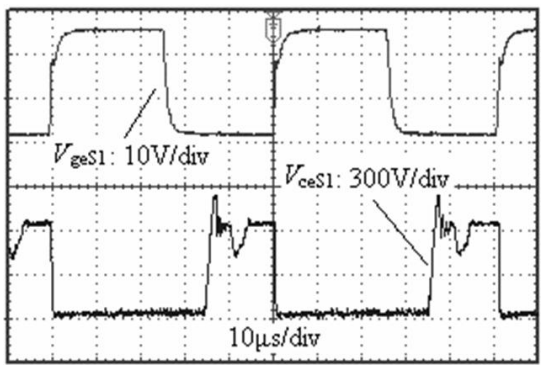


Fig. 10. Driving signal and voltage of S_1.

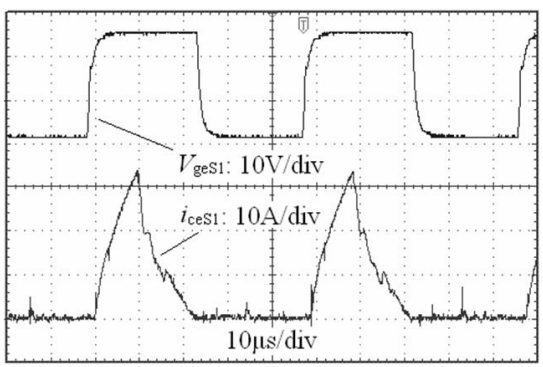


Fig. 11. Driving signal and current of S_1.

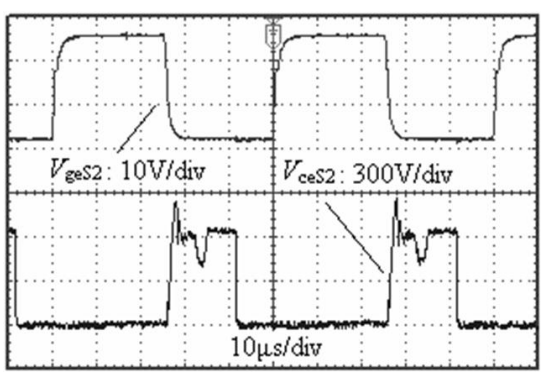


Fig. 12. Driving signal and voltage of S_2.

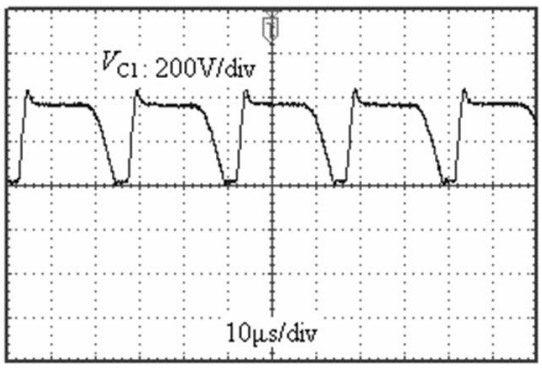


Fig. 13. Voltage of C_1.

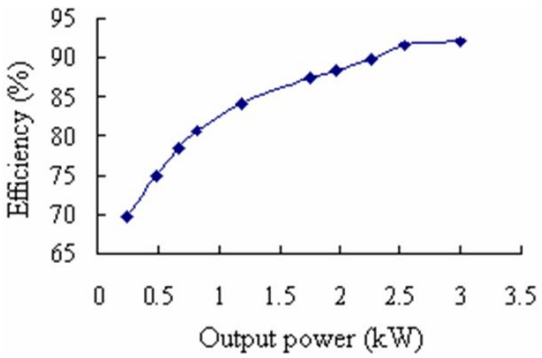


Fig. 14. Efficiency of the prototype.

V. Conclusions

In this paper, a novel passive snubber is proposed and investigated based on a three-phase single-stage isolated full-bridge boost PFC converter. The results show that the adoption of this snubber can realize both the suppression of the voltage spike across bridge leg switches and the energy transfer from the snubber itself to the output side. The operational principles and the design considerations of the passive snubber are discussed in detail. Finally, following the design procedure, a 3kW laboratory-made prototype is built, through which the theoretical analysis and evaluations are verified.

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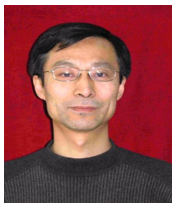

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