

# A High Efficiency Controller IC for LLC Resonant Converter in 0.35 $\mu\text{m}$ BCD

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## Abstract

This paper presents a LLC resonant controller IC for secondary side control without external active devices to achieve low profile and low cost LED back light units. A gate driving transformer is adopted to isolate the primary side and the secondary side instead of an opto-coupler. A new integrated dimming circuitry is proposed to improve the dynamic current control characteristic and the current density of a LED for the brightness modulation of a large screen LCD. A dual-slope clock generator is proposed to overcome the frequency error due to the under shoot in conventional approaches. This chip is fabricated using 0.35  $\mu\text{m}$  BCD technology and the die size is  $2 \times 2 \text{ mm}^2$ . The frequency range of the clock generator is from 50 kHz to 500 kHz and the range of the dead time is from 50 ns to 2.2  $\mu\text{s}$ . The efficiency of the LED driving circuit is 97 % and the current consumption is 40 mA for a 100 kHz operation frequency from a 15 V supply voltage.

**Key Words:** Backlight unit, Clock generator, Dead time, LED driver, LLC resonant controller, Protection, PWM dimming, Soft-start

## I. INTRODUCTION

In recent years, liquid crystal display (LCD) flat panel displays have become one of the fastest growing markets in large screen displays due to various advantages such as low power consumption, long lifespan, low profile and high contrast ratio [1], [2]. Since LCDs are non-emissive display devices, they usually require a backlight unit (BLU) in monitor and TV applications. Recently, light-emitting diodes (LEDs) have become one of the most promising candidates for BLUs and other lighting applications [3]. The power consumption relates directly to screen size in LCD backlighting systems and the demand for large screen LCDs, with a high power density is increasing gradually. As a result, a variety of higher-power topologies have been considered to achieve high efficiency in a compact space with low-EMI generation. LLC resonant converters are popularly adapted in consumer and industrial electronics due to their inherent advantages over contending topologies [4]–[7].

Generally, resonant power transfer systems require galvanic isolation between a relatively high input voltage and low output voltages. The most widely used devices to transfer signals across the isolation boundary are pulse transformers and opto-couplers which are used to provide regulation of the output [8], [9]. Opto-couplers are typically used to isolate the secondary side power supply from the primary side PFM

control.

The drawbacks of primary-side control with opto-coupler feedback are variations in the loop gain due to a wide current transfer ratio (CTR), sensitivity to both time and temperature, and high cost [10]–[12]. Also, primary side control of LED back light units causes the LED driver system to become complicated and bulky because additional OP-Amps, isolation, and discrete devices should be used to sense the load variations on the secondary side and feed this back to the primary side. To remove the opto-coupler from the feedback loop and to achieve fast dynamic performance, a secondary side output regulation method was presented in [13]. However, this method requires an additional chopper circuit to regulate against line variations.

The purpose of this work is to design a simple LED driving circuit and a secondary side LLC resonant controller IC in order to reduce both the complexity and the circuit dimensions. The PFM controller is moved to the secondary side to minimize the number of additional circuits needed for the feedback in the proposed simple LED driving circuit. A gate driving transformer is adopted to isolate the primary side and the secondary side of the LLC resonant converter. A drawback of secondary-side control is that it requires an additional secondary side supply voltage because the control is on secondary side which has to be fully insulated from the primary side [11]. Auxiliary winding from the PFC output on the primary side can be used to solve this problem [14]. If the PFC output is saturated and the supply voltage of the controller IC is stable, the operation of the LLC resonant converter is started. Also, the current transformer (CT) can be used to

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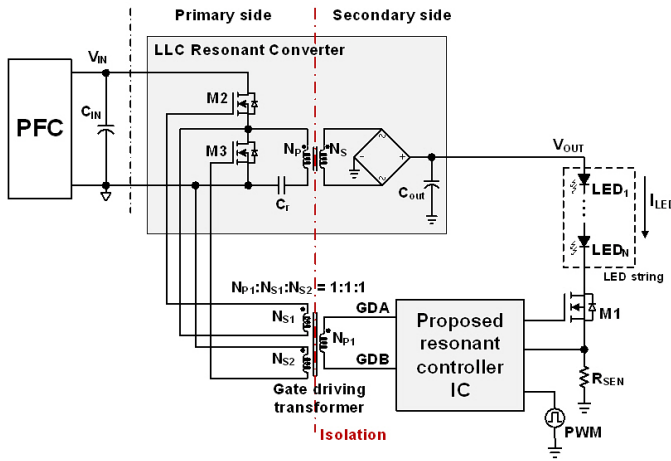


Fig. 1. The proposed half-bridge LLC resonant LED driving circuit.

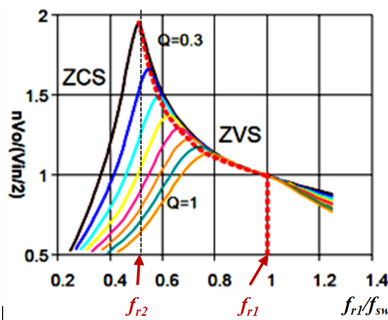


Fig. 2. The gain characteristics of the LLC resonant converter.

compensate for the over current of the primary side [15], [16].

The architecture of the proposed LED driver and controller IC is discussed in Section II, and building blocks are described in Section III. Sections IV and V present the simulations and measurement results and the conclusions, respectively.

## II. PROPOSED LED DRIVER SYSTEM ARCHITECTURE

Fig. 1 shows the proposed half-bridge LLC resonant LED driving circuit. The LLC resonant controller IC is located on the secondary side and the gate driving transformer is used to drive the power MOSFETs, M2 and M3. Also, the gate driving transformer provides isolation between the primary side and the secondary side of the LLC resonant converter and reduces the power consumption for the driving power MOSFET [9]. Because the controller IC is located on the secondary side, the OP-Amps and discrete devices needed for the feedback control can be integrated into the controller IC and eliminated from the printed circuit board (PCB). Thus, the proposed architecture has advantages over the typical architecture in terms of efficiency and cost.

By utilizing the transformer magnetizing inductance, the LLC converter modifies the gain characteristic of the series resonant converter (SRC).

Its voltage gain characteristics for different load conditions ( $R_{LED}$ ) are shown in Fig. 2. Due to the half bridge structure, the output voltage is normalized with half of the input voltage.

Compared to the SRC, the converter can be operated in both buck and boost modes. When the switching frequency is higher than the resonant frequency ( $f_{r1}$ ), the voltage gain

of the LLC resonant converter is always less than one; it operates as an SRC converter and zero voltage switching (ZVS) can be achieved. When the switching frequency is lower than resonant frequency ( $f_{r1}$ ), both ZVS and Zero Current Switching (ZCS) can be achieved for different load conditions. At the boundary of the ZVS and ZCS regions ( $f_{r2}$ ), as shown by the dashed line in Fig. 2, the voltage gain of the converter reaches its maximum value [5]. As a result, the converter must be operated at frequency higher than  $f_{r2}$  depending on the Q value in order to always work in the ZVS region.

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (1)$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}} \quad (2)$$

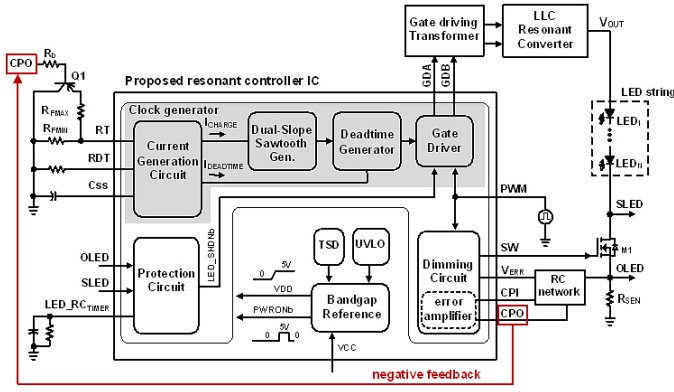
$$Q = \frac{\sqrt{L_r / C_r}}{R_{LED}} \quad (3)$$

where  $f_{r1}$  is the resonant frequency of the converter,  $f_{r2}$  is the minimum frequency to satisfy the ZVS for different load conditions and  $f_{sw}$  is the operating frequency of the converter.

Accordingly, the proposed LED driving circuit is based on the frequency feedback control system to regulate its output. In Fig. 3, the sensing voltage across the resistor,  $R_{SEN}$ , is the feedback to the pnp transistor (Q1) connected to  $R_{FMAX}$  through the error amplifier inside the dimming circuit. The error amplifier compares the voltage across  $R_{SEN}$  with the reference, amplifies the difference, and generates the control signal to Q1. The amplified difference changes the output frequency of the clock generator and compensates for the variations of the sensing voltage of  $R_{SEN}$ . If the voltage across  $R_{SEN}$  is stabilized to the steady reference voltage through the negative feedback, the proportional current to the PWM dimming ratio flows through the LED string in an average sense. For example, if  $R_{SEN}$  is 10  $\Omega$  under a 100% PWM dimming ratio and a steady reference voltage of 1 V is always sensed at the  $R_{SEN}$  resistor, then the current,  $I_{LED}$ , is regulated to 100 mA. The LED PWM dimming will be discussed in section 3 in more detail.

Fig. 3 shows the detailed architecture of the proposed controller IC and LED driving circuit. The controller IC consists of a dual-slope sawtooth generator, a dead time generator, a gate driver, a protection circuit, a current generation circuit, a dimming circuit, and a bandgap reference. When the VCC voltage, which is the external power supply, is higher than the UVLO (under voltage lock out) level and the TSD (thermal shut down) condition is normal, the VDD voltage is generated by the internal bandgap reference. This causes the PWRONb signal to go HIGH and initializes the internal blocks as a power on reset. After an internal capacitor delay, the PWRONb signal goes to LOW and all of the blocks are enabled. The switching frequency of the controller IC is controlled by the internal clock generator. The output frequency of the clock generator is also controlled by the current flowing through the RT node and is proportional to  $I_{CHARGE}$ .

The cross conduction problem is critical in the design of a SMPS (switched-mode power supply), because many of the



|              |   |
|--------------|---|
| RT           | Control the $I_{\text{CHARGE}}$ ( $\alpha$ output frequency of clock generator) |
| RDT          | Control the $I_{\text{DEADTIME}}$ ( $\alpha$ dead time)                         |
| CSS          | Control the soft-start duration   |
| OLED         | Open LED detection  |
| SLED         | Short LED detection   |
| LED_RC_TIMER | The duration of timer for LED open or short                                     |
| GDA/GDB      | Outputs of the gate driver  |
| PWM          | Input of pulse width modulation (for LED dimming)                               |
| SW           | Output of PWM dimming   |
| VERR         | Output of auxiliary amplifier shown in Fig.8                                    |
| CPI          | Input of error amplifier shown in Fig.8   |
| CPO          | Output of error amplifier shown in Fig.8  |

Fig. 3. The architecture of the proposed LLC resonant controller IC and LED driving circuit.

switching circuits fail to meet the performance requirements due to this problem.

Cross conduction causes premature transistor failure, excessive output noise, low efficiency, and excessive heat [12]. The popular method used to prevent cross conduction is to provide a dead time between the complementary driving pulses, GDA and GDB, in order to turn off both of the transistors at the same time. The duration of the dead time is designed to be long enough to assure that the conduction states of the power MOSFETs, M2 and M3 in Fig. 1, do not overlap under any circumstances. Also, the minimum duty ratio of the complementary driving pulses should be guaranteed for each switching cycle. The reason is that for each switching cycle, the body diode of the MOSFET will conduct for some time, and the duty cycle change must be larger than the body diode conduction time [17]. Therefore, the typical dead time is several percent of the driving time in order to insure a safe operating margin, which limits the range of the PFM control. In this paper, a new dead time generator based on the monostable structure is proposed for robust operation with respect to variations.

The gate driver is designed in a totem-pole structure to drive the large input capacitance of M2 and M3 in a short time. A LED protection circuit which detects short conditions is required to protect the power stage from excessive load current. An open LED protection circuit is also required to protect the power stage from excessive output voltage. The dimming circuit controls the external dimming switch, M1, in Fig. 3, by the external PWM input. It also includes an error amplifier to regulate the load current.

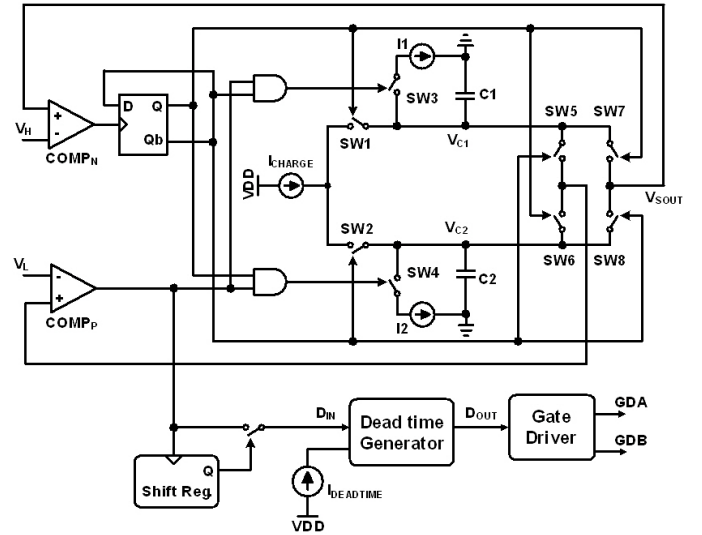


Fig. 4. The block diagram of the proposed dual-slope clock generator.

### III. THE BUILDING BLOCKS

#### A. The dual-slope clock generator

In a conventional dual-slope clock generator, the output frequency and the dead time of the sawtooth wave generator are controlled by the capacitor charging and discharging time, respectively [8], [12]. A conventional dual-slope clock generator has two drawbacks. First, the amplitude error due to the detection circuitries results in nonlinearity of the clock generator since it forms a part of the oscillation period [18]. Second, although the dead time and output frequency are generated by one capacitor, this dead time generation method has an effect on the output frequency.

Fig. 4 shows a block diagram of the proposed dual-slope clock generator to overcome the drawbacks of the conventional approach. The amplitude error can be reduced when compared to those of the conventional approach by switching the output of the triangular waves exclusively [18]. The duration of the dead time does not have an effect on the output frequency, because the sawtooth waves are controlled only by the charging current,  $I_{\text{CHARGE}}$ . The duty ratio of  $D_{\text{IN}}$ , in Fig. 4, is modulated by the dead time generator and is reflected in the asymmetric outputs of GDA and GDB.

In the proposed method, there are four operation phases. These are Phase0 to Phase3, as shown in Fig. 5. Initially,  $V_{C1}$  and  $V_{C2}$  are equal to zero. Phase0 is bypassed by the shift register due to an initial false period. In Phase1, the output of the sawtooth wave generator,  $V_{\text{SOUT}}$ , is connected to  $V_{C1}$  through switch SW7.

$C1$  is charged by the current source,  $I_{\text{CHARGE}}$ , until  $V_{C1}$  reaches  $V_H$ . When  $V_{C1}$  equals  $V_H$ , the connection of  $V_{\text{SOUT}}$  is switched from  $V_{C1}$  to  $V_{C2}$ . In Phase2,  $C2$  is charged by  $I_{\text{CHARGE}}$ , and  $C1$  is discharged by another current source,  $I1$ . When the voltage of  $C1$  reaches  $V_L$ , the discharging of  $C1$  is finished and  $V_{C1}$  is kept as  $V_L$ . In Phase3,  $V_{C1}$  continues to be equal to  $V_L$  and  $C2$  is charged until  $V_{C2}$  reaches  $V_H$ . When  $V_{C2}$  equals  $V_H$ , the connection of  $V_{\text{SOUT}}$  is switched from  $V_{C2}$  to  $V_{C1}$ . The output voltage of the sawtooth wave generator,  $V_{\text{SOUT}}$ , is generated by repeating the above three

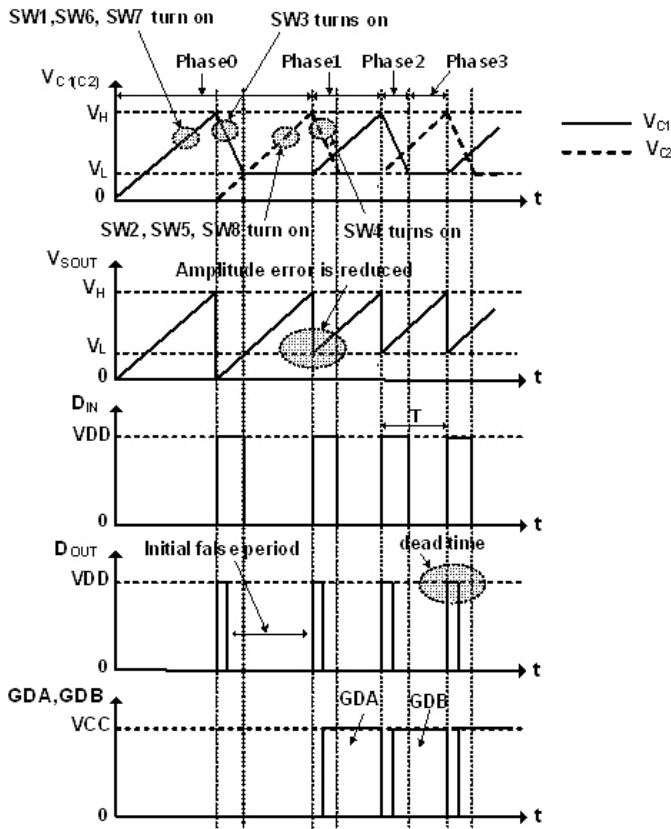


Fig. 5. The output waveforms of the proposed dual-slope clock generator.

phases. The amplitude error is greatly decreased because it is determined only by the switching time. The output frequency  $f_{out}$  of the dual-slope clock generator is determined by (4):

$$f_{out} = \frac{1}{2T} = \frac{I_{CHARGE}}{2 \cdot C_S \cdot (V_H - V_L)} \quad (4)$$

where  $T$  is the period of  $V_{SOUT}$  in Fig. 5 and is the period of the dual-slope sawtooth generator. For example,  $f_{out}$  is 500 kHz when  $I_{CHARGE} = 12 \mu A$ ,  $V_H = 4 V$ ,  $V_L = 1 V$ ,  $C_S = C1 = C2 = 4 pF$ , and  $I1 = I2 = 40 \mu A$ .

**B. The dead time generator**

Fig. 6 and Fig. 7 show the proposed mono-stable dead time generator and its output waveforms, respectively. The proposed circuit uses a stable current source and  $V_{C1}$  can be discharged to zero by the auxiliary MOSFET, M4, in Fig. 6. It must be noted that size of M4 needs to be considered carefully because it can cause an undershoot voltage if there is an excessive discharge current.  $V_{C1}$  changes to  $V_H$  plus the HIGH voltage level of  $V_N$  when  $V_{C1}$  reaches  $V_H$  and  $D_{IN}$  is LOW. Therefore, the zener diode, Z1, is added to the  $V_{C1}$  node to limit the voltage level.

The three steps in Fig. 7, Step0 to Step2, show the operation of the proposed dead time generator. Initially,  $D_{IN}$  and  $D_{OUT}$  are LOW. In Step0,  $V_{C1}$  and  $V_N$  are saturated to VDD in the power-on stage.  $V_d$  and  $D_{OUT}$  remain LOW until  $D_{IN}$  is HIGH. In Step1, when  $D_{IN}$  is HIGH,  $V_N$  and  $V_d$  change to LOW and HIGH, respectively. Also,  $V_{C1}$  is discharged to zero and  $D_{OUT}$  goes to HIGH. In Step2, after a fixed delay,  $T_{dis}$ ,  $V_d$  goes to LOW and  $V_{C1}$  starts to be charged. Then  $D_{OUT}$

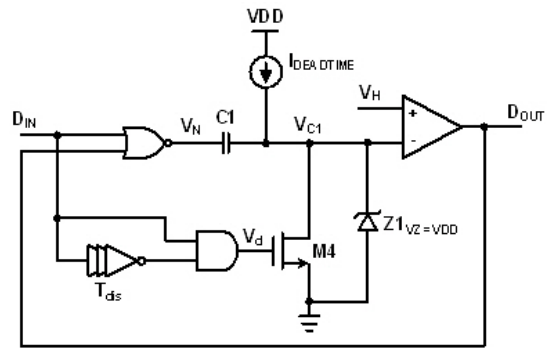


Fig. 6. The proposed dead time generator.

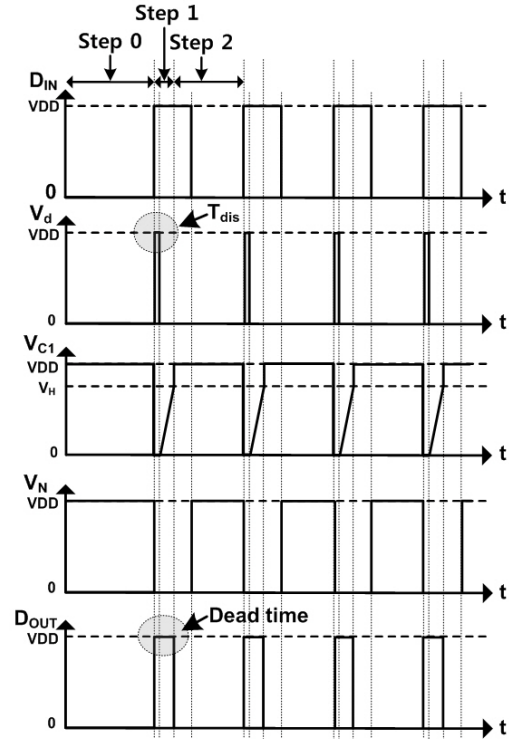


Fig. 7. Output waveforms of dead time generator.

goes to LOW when  $V_{C1}$  reaches  $V_H$ .  $V_N$  changes to HIGH when  $V_{C1}$  reaches  $V_H$  and  $D_{IN}$  is LOW. The dead time,  $D_{OUT}$ , is generated by repeating the two steps, from Step1 to Step2.

The dead time is calculated by (5):

$$Deadtime = T_{dis} + \frac{V_H \times C1}{I_{DEADTIME}} \quad (5)$$

The duty cycle of the dead time should be guaranteed for each switching cycle of the sawtooth generator output because  $D_{OUT}$  is generated at every rising edge of the sawtooth generator output,  $D_{IN}$ , in Fig. 5. As a result, the maximum value of the dead time is limited to a half-period of the output frequency of the gate driver by Eq. (4). If the dead time is larger than a half period of the gate driver output,  $D_{OUT}$  disappears. For example, the dead time is  $2 \mu s$  when  $T_{dis} = 5 ns$ ,  $C1 = 2 pF$ ,  $V_H = 4 V$ , and  $I_{DEADTIME} = 4 \mu A$ . In the resonant circuit design, the dead time should be carefully determined because the minimum duty cycle of the gate driving outputs is related to the conduction time of the body diode of the power MOSFET and the minimum

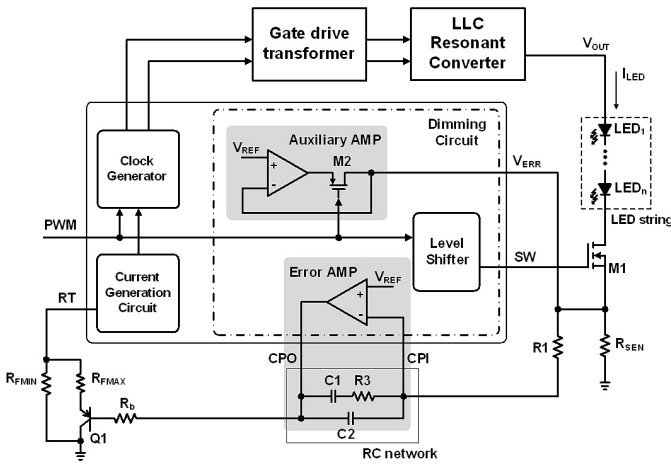


Fig. 8. The dimming circuit and its external components.

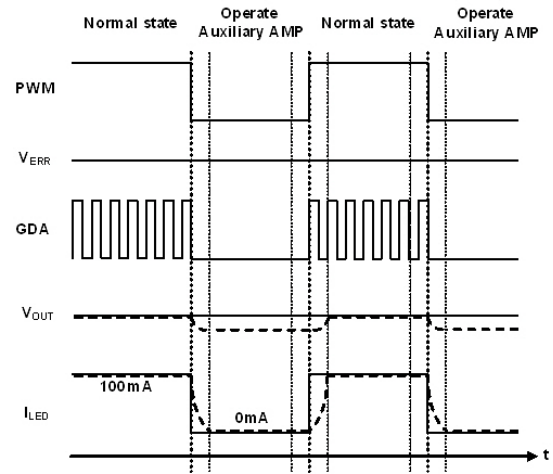


Fig. 9. LED dimming waveforms of the proposed dimming circuit.

dead time is related to the output capacitance of the power MOSFET.

### C. The dimming circuit

The purpose of this work is to design a secondary side controller IC in order to reduce the complexity and dimensions of the backlight unit. The controller IC for a LED driving circuit is moved to secondary side and the external components are integrated into the IC. The proposed controller IC includes dimming circuitry to increase the area efficiency and it can regulate the load current variation. The LED current should be kept constant because variations in the LED current have a serious effect on the lifespan and reliability of the unit. Analog dimming is used to regulate the luminance by adjusting the amplitude of the LED current. On the other hand, PWM dimming controls the average current of the LED by a dimming ratio with a constant current amplitude. The LED brightness intensity of PWM dimming is independent of the color, which makes it suitable for many applications [3], [20], [21]. Accordingly, the proposed circuit adopts PWM dimming to regulate the brightness as shown in Fig. 8. Fig. 9 shows the LED dimming waveforms of the proposed dimming circuit.

In Fig. 8, if the PWM dimming signal is LOW,  $I_{LED}$  is blocked by the switch, M1. This results in a no-load condition in the resonant circuit and causes a load switching transient, which causes an inrush current problem at the LED string when the PWM dimming signal goes from LOW to HIGH. In the proposed IC, the gate driver interruption function is integrated in order to solve this problem. The gate driver interrupt function during the LOW duration of the PWM signal helps to prevent the power transfer to the secondary side and then prevents the load switching transient. Also, the auxiliary amplifier connects  $V_{ERR}$  to  $V_{REF}$  when the PWM is LOW. It reduces time for the voltage across  $R_{SEN}$  to reach  $V_{REF}$  after the PWM goes from LOW to HIGH. In other words, it helps to boost up the saturation time of the  $I_{LED}$  current, as shown in Fig. 9.

On the other hand, when the PWM dimming signal is HIGH, the switch, M2, within the auxiliary amplifier in Fig. 8 is turned off and the sensing voltage across the resistor,  $R_{SEN}$ , is connected to the negative input, CPI, of the error amplifier. If

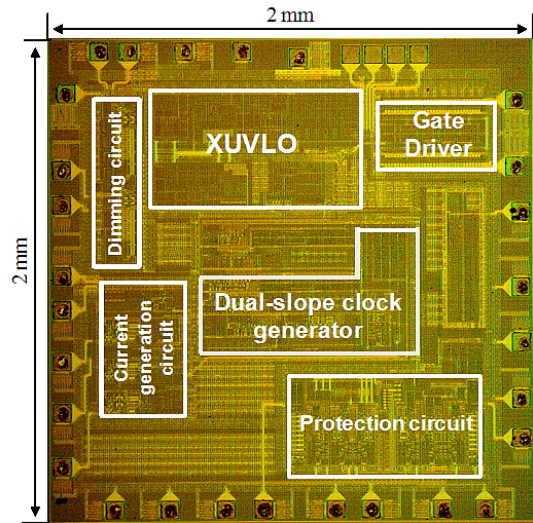


Fig. 10. The chip microphotograph.

the CPI voltage rises above  $V_{REF}$  when the PWM is HIGH, then the RT node current increases through  $R_{FMAX}$ , because the voltage of the CPO drops to a LOW level. Thus, the output frequency of the gate driver rises to the maximum frequency set by  $R_{FMAX}$  and the gain of the LLC resonant converter decreases. The variations of  $I_{LED}$  are compensated in this manner. It is possible to eliminate M1 and use the switches M2 and M3 for the dimming function. This will be an even more cost effective solution because one full power rated switch (M1) will be eliminated. However, if M1 is removed in the schematic,  $V_{OUT}$  will be discharged to the forward voltage of the LED string through the resistor,  $R_{SEN}$ , when the PWM is LOW. As a result,  $V_{OUT}$  needs recharging to the normal state when the PWM is HIGH and it is hard to meet the dynamic current control characteristic shown with a dashed line in Fig. 9.

## IV. EXPERIMENTAL RESULTS

The chip was fabricated using the BCD process with 0.35  $\mu\text{m}$  technology, two poly layers, three metal layers, and the option of a high-voltage MOSFET. The chip microphotograph is shown in Fig. 10.

TABLE I  
THE EXPERIMENTAL CONDITIONS

|   |  |
|---|--|
| PFC output voltage (VIN)                | 385 V  |
| I <sub>LED</sub> @ 100% PWM dimming     | 509 mA   |
| Output Voltage (V <sub>OUT</sub> )      | 32 V   |
| Power efficiency of LED driving circuit | 97 %   |
| PWM dimming frequency                   | 200 Hz   |
| Output Capacitor (C <sub>OUT</sub> )    | 120 $\mu$ F / 50V                                      |
| The transformer winding turns ratio     | $N_p : N_s = 48 : 8$                                   |
| Resonant Tank                           | $L_M = 680 \mu$ H,<br>$L_r = 170 \mu$ H, $C_r = 15$ nF |

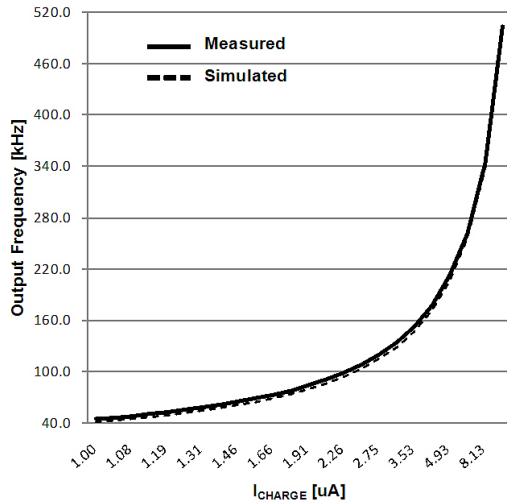


Fig. 11. The relationship between the output frequency of the gate driver and  $I_{CHARGE}$ .

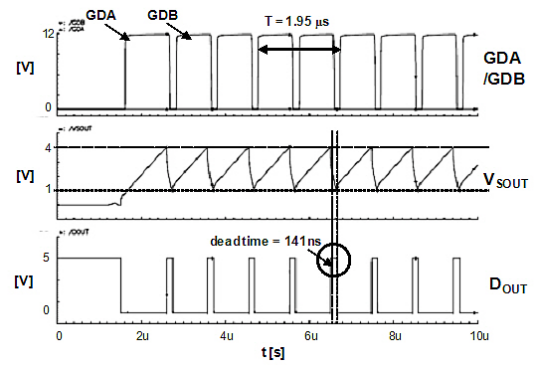
The die area of the controller IC is  $2 \times 2 \text{ mm}^2$ . The experimental conditions for the proposed LED driving circuit are summarized in Table I.  $N_p$  and  $N_s$  are the transformer winding turns ratios in Fig. 1, respectively.  $L_M$  is the transformer magnetizing inductance and  $L_r$  is the series leakage inductance with a series capacitance,  $C_r$ . The PWM dimming frequency is 200 Hz in the experiment. The output power is 32 W. The power dissipated by  $R_{SEN}$  is 1 W, since  $R_{SEN}$  is 1  $\Omega$  and the voltage across  $R_{SEN}$  is kept at 1 V for any dimming ratio by the operation of the error amplifier in the dimming circuit.

Thus, the power efficiency of the LED driving circuit is 97% regardless of the dimming ratio. In the conventional approach, the clock generator has two drawbacks. These are an amplitude error and a dependency of the output frequency on the dead time. Fig. 11 shows the measured output frequency of the gate driver versus the  $I_{CHARGE}$  current. It can be varied from 44.7 kHz to 503.5 kHz depending on the  $I_{CHARGE}$  current, which corresponds to the currents ranging from 1.04  $\mu$ A to 12.05  $\mu$ A.

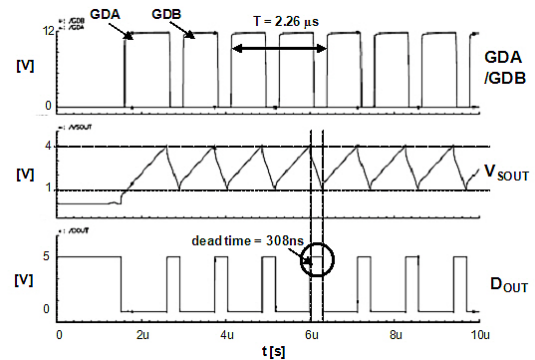
These measurements show that the proposed dual-slope clock generator has 3 % accuracy at its programmable maximum switching frequency, 503.5 kHz with  $I_{CHARGE} = 12.5 \mu$ A.

Fig. 12 (a) and (b) show the effect of the dead time generation method of the conventional dual-slope clock generator on the output frequency. The period of the output of the gate driver is 1.95  $\mu$ s which corresponds to a frequency of 513 kHz when the dead time is 141 ns in Fig. 12(a).

However, if the dead time is increased to 308 ns, the period



(a) Dead time = 141 ns.



(b) Dead time = 308 ns.

Fig. 12. The effect of the dead time generation method of the conventional dual-slope generator on the output frequency.

of the output of the gate driver is changed into 2.26  $\mu$ s which corresponds to a frequency of 442 kHz, as can be seen in Fig. 12(b).

These results show that the conventional dead time generation method has effects on the output frequency.

On the contrary, Fig. 13 shows the effect of the dead time generation method of the proposed dual-slope clock generator on the output frequency.

The frequency of the output of the proposed dual-slope clock generator is kept constant at 2.09  $\mu$ s in both cases when the dead times are 53 ns and 603 ns, as shown in Fig. 13 (a) and (b).

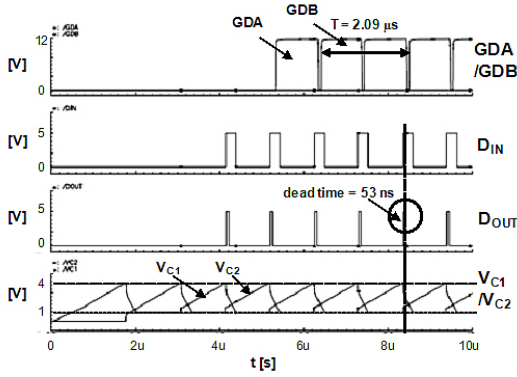
Fig. 14 shows the soft-start operation at the power-on stage. The soft-start duration is controlled by the external capacitor  $C_{SS}$  and it is finished when the voltage across the capacitors  $C_{SS}$  and  $V_{CSS}$ , reach 2 V.

$V_{OUT1}$  is gradually increased during the soft-start duration. This reduces the start-up transient in the output stage of the LLC resonant converter.

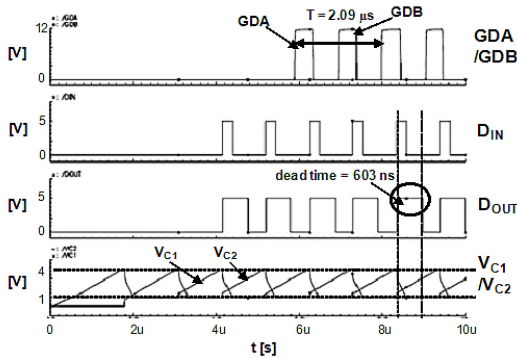
Fig. 15 shows the resonant waveforms at the steady-state and it can be seen that the voltage-second balancing of the series inductance current  $I_{Lr}$  is achieved for a small load.

Fig. 16 shows the measured waveforms when the PWM dimming ratios are 2%, 10 %, 50 %, and 100%. As shown in Fig. 16, the amplitude of the LED current is regulated to 509 mA regardless of the PWM dimming ratio, and the LED luminance is changed by the LED average current depending on the PWM duty ratio.

Fig. 17 is the measured relationship between the LED



(a) Dead time = 53 ns.



(b) Dead time = 603 ns.

Fig. 13. The effect of the dead time generation method of the proposed dual-slope clock generator on the output frequency.

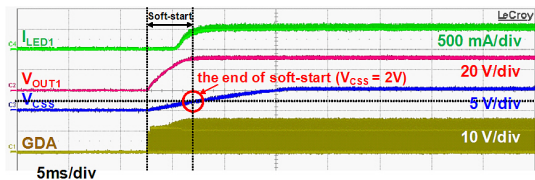


Fig. 14. The soft-start operation at power-on stage.

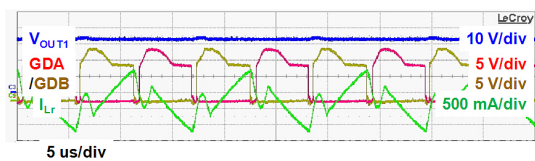


Fig. 15. Resonant waveforms.

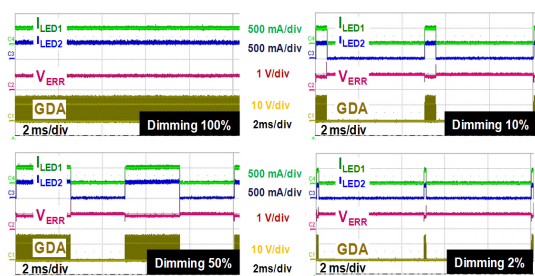


Fig. 16. Measured waveforms with respect to the various PWM dimming ratios.

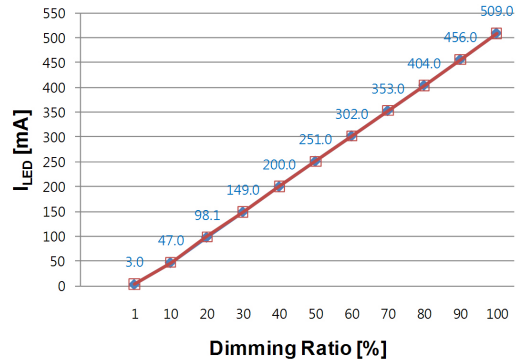


Fig. 17. Measured relationship between the LED current ( $I_{LED}$ ) and the dimming ratio.

TABLE II  
THE COMPARISON TO PRIOR WORKS

|  | [8]              | [9]              | This work          |
|--|------------------|------------------|--------------------|
| Power supply   | 20 V             | 15 V             | 15V                |
| Current consumption  | 40mA @ 100 kHz   | N/A              | N/A                |
| Location of LLC resonant controller IC                                     | Primary side     | Primary side     | Secondary side     |
| Dependency of the output frequency of the clock generator on the dead time | Dependent        | N/A              | Independent        |
| Frequency control range of clock generator                                 | 50 kHz ~ 500 kHz | 30 kHz ~ 350 kHz | 44.7 kHz ~ 500 kHz |
| Dead time  | ~ 2 μs           | ~ 920 ns         | ~ 2.2 μs           |
| LED dimming circuit  | No               | No               | Integrated         |

current,  $I_{LED}$ , and the dimming ratio, which shows the good linearity between them.

Table II shows the performance comparison results with prior works. The proposed controller IC uses a single 15 V power supply and the current consumption is 40mA with a 100 kHz output frequency.

Because the controller IC is located on the secondary side, the proposed IC integrates the dimming and protection circuits.

Thus, it has advantages over the conventional architectures in terms of its dimensions and cost. With the proposed dead time generator, the output frequency of the clock generator is independent of the variations in dead time and it has a wide control range of 50 kHz ~ 500 kHz. Also, the high efficiency LED dimming circuit is integrated to implement a more cost effective system.

### V. CONCLUSIONS

This paper presents a cost-effective secondary side LLC resonant controller IC for LED backlight units. The proposed secondary side controller IC includes most of the circuits for output regulation and LED dimming. As a result, it is possible to design a more simple and small LED backlight unit. Also, a gate driving transformer is adopted in the LED driving circuit for isolation instead of an opto-coupler. This chip is fabricated using 0.35 μm BCD technology and the die size is 2 × 2 mm<sup>2</sup>. The operation frequency range of the clock generator is from 50 kHz to 500 kHz and the range of the dead time is from 50 ns to 2.2 μs. The efficiency of the LED driving circuit is

97 % and the current consumption is 40 mA for a 100 kHz operation frequency from a 15 V supply voltage.

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