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Active Frequency with a Positive Feedback Anti-Islanding Method Based on a Robust PLL Algorithm for Grid-Connected PV PCS

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Abstract

This paper proposes an active frequency with a positive feedback in the *d-q* frame anti-islanding method suitable for a robust phase-locked loop (PLL) algorithm using the FFT concept. In general, PLL algorithms for grid-connected PV PCS use *d-q* transformation and controllers to make zero an imaginary part of the transformed voltage vector. In a real grid system, the grid voltage is not ideal. It may be unbalanced, noisy and have many harmonics. For these reasons, the *d-q* transformed components do not have a pure DC component. The controller tuning of a PLL algorithm is difficult. The proposed PLL algorithm using the FFT concept can use the strong noise cancelation characteristics of a FFT algorithm without a PI controller. Therefore, the proposed PLL algorithm has no gain-tuning of a PI controller, and it is hardly influenced by voltage drops, phase step changes and harmonics. Islanding prediction is a necessary feature of inverter-based photovoltaic (PV) systems in order to meet the stringent standard requirements for interconnection with an electrical grid. Both passive and active anti-islanding methods exist. Typically, active methods modify a given parameter, which also affects the shape and quality of the grid injected current. In this paper, the active anti-islanding algorithm for a grid-connected PV PCS uses positive feedback control in the *d-q* frame. The proposed PLL and anti-islanding algorithm are implemented for a 250kW PV PCS. This system has four DC/DC converters each with a 25kW power rating. This is only one-third of the total system power. The experimental results show that the proposed PLL, anti-islanding method and topology demonstrate good performance in a 250kW PV PCS.

Key Words: Anti-Islanding, Grid-Connected, Photovoltaic PCS, PLL

I. INTRODUCTION

Renewable energy resources have become an increasingly important part of power generation in recent years. In addition to assisting in the reduction of greenhouse gas emissions, they add much needed flexibility to the energy resource mix by decreasing dependence on fossil fuels. Due to their modular nature, ease of installation, and because they can be located closer to end users, PV systems have great potential as a distributed power source to utility companies [1], [8], [10].

For utility applications, islanding is a condition in which a portion of the utility system, which contains both a load and distributed generation (DG), is isolated from the remainder of the utility system and continues to operate. If a DG inverter system is not designed for islanding operation, from the point of view of the utility, it requires the detection of unintentional islanding on the DG inverters. This is due to the fact that the utility cannot control the voltage and frequency in the island, creating the possibility of damage to customer equipment in a situation over which the utility has no control. Islanding may also create a hazard for utility line-workers and the public by causing a line to remain energized when it is assumed to be disconnected from all energy sources.

There are numerous islanding detection methods for grid-connected PV systems reported in the technical literature [21]–[23]. They can be classified into two broad categories. These include passive and active which can be either inverter built or utility supported. However, passive methods have a number of weaknesses including the inability to detect islanding. An excellent overview report on both passive and active methods is available in [21]. Active methods have been developed in order to overcome the limitations of passive methods. In simple terms, active methods introduce perturbations into the inverter output power for a number of parameters as follows:

- Output power variation either real or reactive [22].
- Active frequency drift or frequency shift up/down [21],[23].
- Sliding mode or slip-mode frequency shift [21], [23].
- Sandia frequency shift, accelerated frequency drift or

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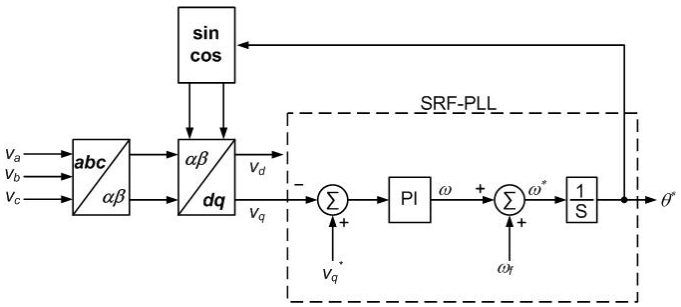

Fig. 1. Synchronous Reference Frame PLL Algorithm [2].

active frequency drift with positive feedback [23].
- Impedance measurements [21]–[23].
- Detection of impedance at a specific frequency or monitoring of harmonic distortion [21].
- Sandia voltage shift [21].
- Frequency jump [21].

The proposed method is intended to achieve successful anti-islanding with a minimized nondetection zone (NDZ), a non-compromised power quality, and no additional equipment requirements.

The other key concept of a grid-connected distributed generation system is to obtain the position of the grid voltage in order to successfully connect to the utility. In general industrial environments the grid voltage is distorted and unbalanced because of nonlinear loads like diode/thyristor rectifiers [9]. The scheme used to obtain the voltage position strongly influences the performance and stability of a grid-connected PCS. For this reason, this scheme must be robust against all disturbances from the utilities [11]-[20]. There are various solutions for obtaining the voltage position of the grid voltage including:

- Synchronous Reference Frame PLL (SRF-PLL) [2].
- Double Synchronous Reference Frame PLL (DSRF-PLL) [3], [4].
- Synchronous Reference Frame PLL with a Positive Sequence Filter (PSF-PLL).
- Synchronous Reference Frame PLL with a Sinusoidal Signal Integrator (SSI-PLL) [5].
- Double Second Order Generalized Integrator PLL (DSOGI-PLL) [6].

The SRF-PLL scheme shown in Fig. 1 is extremely simple but it is sensitive to voltage distortions or unbalances. The others were proposed to overcome of the drawbacks of the SRF-PLL scheme but some of them are complicate and hard to implement.

In this paper, a robust PLL algorithm is proposed which is totally different from the general PLL schemes mentioned above. Since the proposed algorithm uses the FFT concept, it is very robust to disturbance like unbalances, harmonics, and high frequency switching noise. Also an active frequency drift anti-islanding method for grid-connected PV PCS using positive feedback control in the *d-q* frame is proposed.

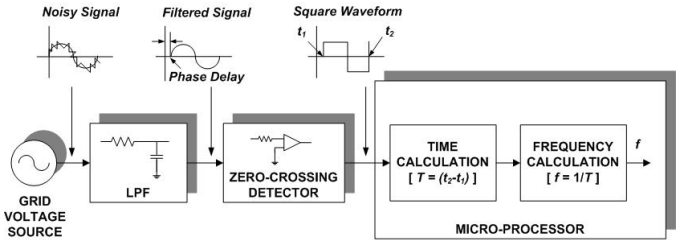

Fig. 2. Precision frequency detector.

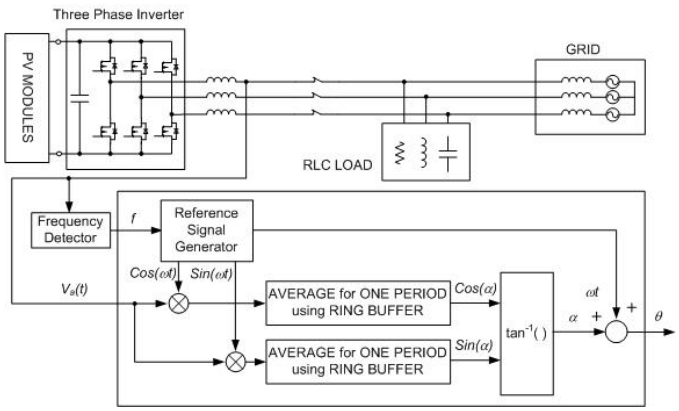

Fig. 3. The proposed PLL algorithm using FFT concept.

II. Proposed Robust PLL Algorithm using the FFT Concept for a Grid-Connected PV PCS

For the proposed PLL algorithm (KERI-PLL), the frequency needs to be detected with precision. Since the grid voltage may have many noisy components like harmonics, a strong low pass filter is used to eliminate them. The phase information of the grid voltage is influenced by the low pass filter but the frequency information is not. The square waveform signal passed to the zero-crossing detector is input to the high speed input port of a DSP microprocessor. The frequency information of the grid can be obtained with high resolution.

The period and frequency of the grid voltage are calculated precisely in the DSP microprocessor as follows:

$$T = (t_2 - t_1), \quad f = \frac{1}{T} \tag{1}$$

where T and f are the period time and frequency of the grid voltage, and t_1 and t_2 are the rising and falling times of the square waveform signal passed to the zero-crossing detector.

Since various loads exist on the real grid, the grid voltage has many harmonics and noisy components. To synchronize with the fundamental component of the grid voltage, an extraction algorithm for the fundamental component, which can cancel out the noisy components including harmonics, is needed.

The grid voltage $v_a(t)$ with harmonics is described with the Fourier series as follows:

$$\begin{aligned} v_a(t) &= V_m \cos(\omega t + \alpha) \\ &\quad + \sum_{n=2}^{\infty} V_{mn} \cos(n\omega t + \alpha_n) + \sum_{n=2}^{\infty} V_{mn} \sin(n\omega t + \alpha_n) \\ &= V_m \cos(\omega t + \alpha) + harmonics \end{aligned} \tag{2}$$

where V_m and V_{mn} are the magnitude of the fundamental component and the n-th harmonic components of the grid

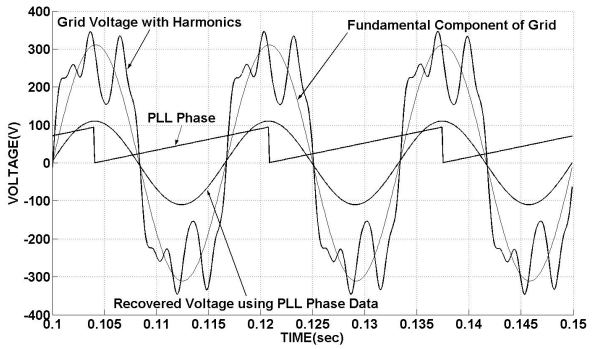

Fig. 4. Noise cancellation characteristics of the proposed PLL.

voltage and α and α_n are the phase components of the fundamental and the n-th harmonic components.

The reference signals $\cos(\omega t)$ and $\sin(\omega t)$ can be generated using the grid frequency obtained from the frequency detector as follows:

$$\begin{aligned} V_{REFCOS}(t) &= \cos(2\pi f t) \\ V_{REFSIN}(t) &= \sin(2\pi f t). \end{aligned} \tag{3}$$

Since these signals are generated by a DSP microprocessor, they are noise free. After the product grid voltage and the reference signals are derived, the following equation is obtained:

$$\begin{aligned} V_{GridCos}(t) &= v_a(t) \times V_{REFCOS}(t) \\ &= [V_m \cos(\omega t + \alpha) + harmonics] \times \cos(\omega t) \\ &= \frac{V_m}{2}[\cos(\alpha) + \cos(2\omega t + \alpha)] + harmonics \times \cos(\omega t) \\ V_{GridSin}(t) &= v_a(t) \times V_{REFSIN}(t) \\ &= [V_m \cos(\omega t + \alpha) + harmonics] \times \sin(\omega t) \\ &= \frac{V_m}{2}[\sin(\alpha) + \sin(2\omega t + \alpha)] + harmonics \times \sin(\omega t). \end{aligned} \tag{4}$$

Since the last two terms are periodic signals, the average value for one period is to be zero. After averaging for one period, only the dc term remains as follows:

$$\begin{aligned} V_{GridCosAvg}(t) &= \int_0^T V_{GridCos}(t)dt = \frac{V_m}{2}\cos(\alpha) \\ V_{GridSinAvg}(t) &= \int_0^T V_{GridSin}(t)dt = \frac{V_m}{2}\sin(\alpha). \end{aligned} \tag{5}$$

The phase difference α between the grid voltage and the reference signals can be obtained using the arctangent function as shown in Fig. 2.

$$\alpha = \tan^{-1}\left(\frac{V_{GridSinAvg}(t)}{V_{GridCosAvg}(t)}\right). \tag{6}$$

We can get the current position of the grid voltage by adding the reference phase ωt and α as follows:

$$\theta = \omega t + \alpha \tag{7}$$

where θ is the current position of the grid voltage.

The proposed algorithm is simulated to prove its effectiveness using the MATLAB simulation program.

Fig. 4 shows the robustness of the proposed PLL algorithm with respect to noisy signals. The source signal has many harmonics but the proposed PLL algorithm detects the phase

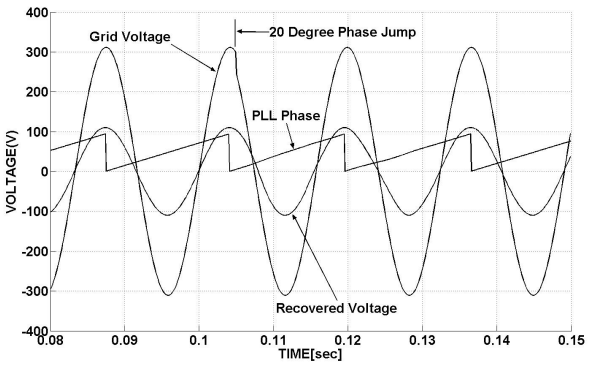

Fig. 5. Phase jump characteristics.

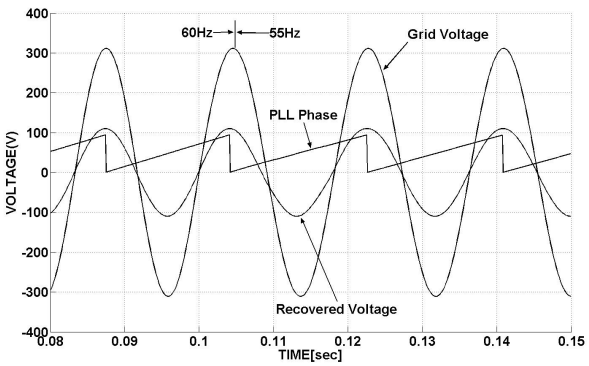

Fig. 6. Frequency jump characteristics from 60Hz to 55Hz.

of the fundamental signal of the noisy source signal exactly. Fig. 4 shows that the recovered fundamental signal using the detected phase is in phase with the fundamental component of the noisy source signal. Fig. 5 shows the response of the proposed PLL algorithm in the case of a source signal with a 20 degree phase jump.

Fig. 6 and 7 show the responses of frequency jumps of the source signals. In the grid application of a PV PCS, the normal operating range of the frequency is as follows:

$$59.3\text{Hz} \leq f \leq 60.5\text{Hz}$$

The operating range of the grid frequency is very narrow with respect to the application of grid-connected applications. Fig. 6 and 7 shows that the proposed PLL algorithm can be stably operated without fluctuations in the PLL phase within the normal frequency operating range. The characteristics of the proposed robust PLL algorithm are as follows:

- Since the proposed algorithm does not use information on the grid voltage magnitude, it is robust under conditions such as, sags or voltage unbalances on the grid.
- Since it uses a noise free reference signal generated by a DSP microprocessor and the FFT concept for extracting the target frequency component, the proposed PLL algorithm can assure stable operation with noisy signals that include harmonics and high frequency noise components.
- It uses single phase voltage information only. Therefore, this algorithm can be applied to single and three phase systems without revision.
- It has no controller like the PI controller in SRF-PLL and

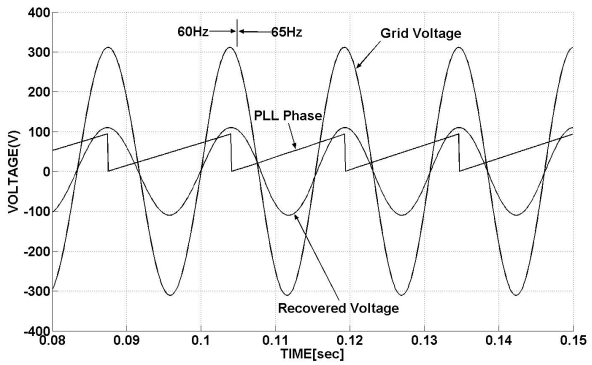

Fig. 7. Frequency jump characteristics from 60Hz to 65Hz.

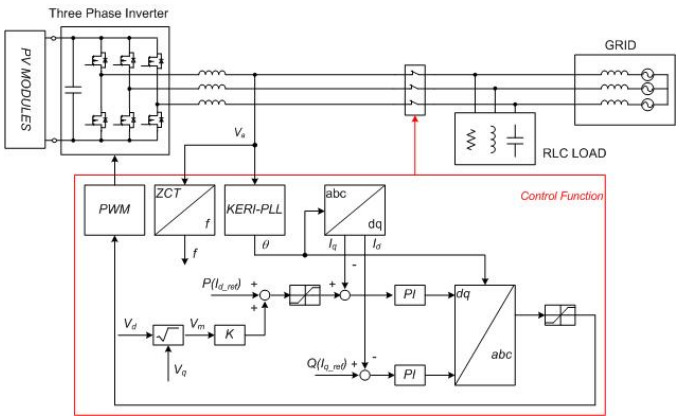

Fig. 8. Block diagram of the proposed active voltage positive feedback anti-islanding method.

other algorithms. Therefore, there is no PI controller's gain tuning process.

This algorithm can be easily implemented using a DSP microprocessor.

III. Proposed Active Positive Feedback Anti-Islanding Method in the D-Q Frame

Active inverter-resident methods use a variety of techniques in an attempt to cause an abnormal condition in the PCC voltage that can be monitored to detect islanding [21]. Voltage, current or frequency disturbances are injected into the supply system to perturb the load circuit. Then the islanding conditions are detected based on a change that indicates that the distribution network, with its stable voltage, stable frequency and low impedance, has been disconnected. Fig. 8 is a block diagram of the proposed active voltage positive feedback anti-islanding method. When the inverter supplies power to the grid, the consequence of adding $K \cdot V_m$ to $P\left(I_{dref}\right)$ is observed as a reference signal on the P axis.

The proposed islanding detection method is based on the detection of grid voltage changes. The positive feedback signal on the active power axis (P axis or d axis) is proportional to the magnitude of the grid voltage in the d-q frame.

The principle behind the proposed method is described as follows:

$$I_{d_{anti-islanding}} \text{ or } P_{anti-islanding} = K\left[V_m(t) - V_m(t-1)\right] \quad (8)$$

where K is the controller gain and $V_m(t)$ and $V_m(t-1)$ are the magnitudes of the voltage at the sampling time. Fig. 9. Block diagram of the proposed active frequency positive feedback anti-islanding method.

Fig. 9 shows block diagrams of the proposed active frequency positive feedback anti-islanding method. The method is based on a change in the inverter frequency. The positive feedback signal on the reactive power axis (Q axis or q axis) is proportional to the difference between a basic 60Hz frequency and the grid frequency. Reactive power has no power loss because of the LC characteristics under ideal conditions. The principle of the proposed method is described as follows:

$$\begin{aligned} Q &= V^2\left(\omega C - 1/\omega L\right) \\ \Delta f &= f - f_o \end{aligned} \quad (9)$$

When the inverter supplies power to the grid, the consequence of adding $K \cdot \Delta f \cdot I_{dref}$ to $Q\left(I_{qref}\right)$ is observed as a reference signal on the Q axis. The proposed islanding detection method is based on the detection of these grid frequency changes.

IV. A Novel PV 250kW PCS Implemented using The Proposed Algorithm

In general, since the lowest voltage of a PV module is lower than the required voltage to connect to the grid directly, there is always a difference between the PV module output voltage and the required DC link voltage of an inverter. From another point of view, obtaining the required DC link voltage of an inverter is possible if the difference in voltage is added to the output voltage of the PV module. Fig. 10 shows the proposed topology using the high efficiency DC/DC converter in [7] and [13], which is able to produce a high DC link voltage for the inverter.

The required power for the DC/DC power conversion stage can be calculated as follows:

$$\begin{aligned} IDC &= \frac{PPV}{VDC} \\ PC &= IDC(VDC - VPV) = PPV\frac{VDC - VPV}{VDC} \\ &= P_{PV}\frac{V_C}{V_{DC}} \end{aligned} \quad (10)$$

where P_C is the required power of the DC/DC power conversion stage, V_{DC} is the constant required DC link voltage of the inverter, P_{PV} is the PV module output power, I_{DC} is the DC link input current at V_{DC} and V_{PV} is the PV module output voltage.

The small isolated DC/DC converter generates only the difference in voltage between the PV module output voltage and the required DC link voltage of the inverter. Therefore, since the DC/DC power conversion stage does not need to generate the entire required DC link voltage of the inverter in the proposed topology, the required rated power of the DC/DC power conversion stage is dramatically reduced. As the PV module output voltage approaches the required DC link voltage of the inverter, the power of the converter is steeply reduced. The design specifications of the PV system are as follows:

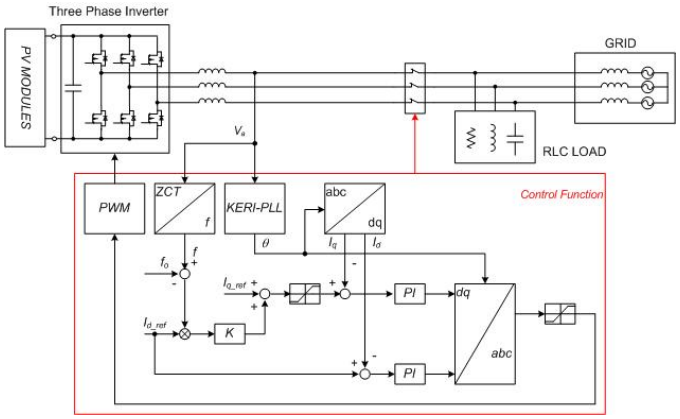

Fig. 9. Block diagram of the proposed active frequency positive feedback anti-islanding method.

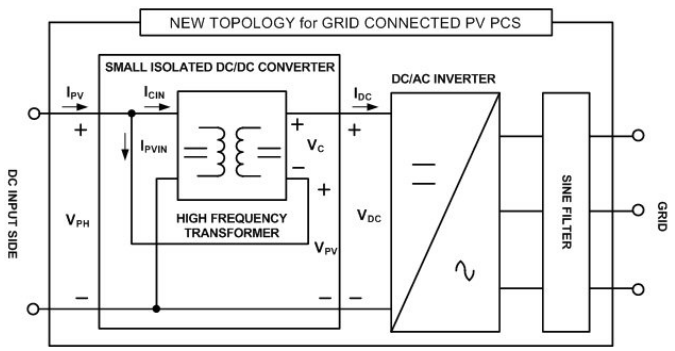

Fig. 10. PV PCS topology implemented the proposed PLL algorithm.

- MPPT range: 450–850V_{DC}.
- Required DC link voltage of the inverter: 630V_{DC}.
- The output voltage of the inverter and the 3ϕ grid line voltage: 380V_{AC}.
- Rated power of the PCS: 250kW.

At the lowest PV voltage, the maximum amount of power is required from the DC/DC power conversion stage. Using equation (10) and the above specifications, the maximum power of the converter is obtained as follows:

$$V_{PV} = 450\text{V},$$
$$P_{PV} = 250\text{kW},$$
$$P_C = 250\text{kW}\frac{630\text{V} - 450\text{V}}{630\text{V}} = 71.4\text{kW}.$$

The required converter power is only 28.7% of the rated power of the PCS. In the proposed topology, the required converter power can be significantly reduced. The efficiency of the proposed converter is described as follows:

$$\eta_{new} = p + (1-p)\eta_C$$
$$p = \frac{P_S - P_C}{P_S} \tag{11}$$

where:

η_{new}: the total efficiency of the proposed converter.

η_C : the efficiency of the DC/DC power conversion stage

P_S: the total system power.

P_C: the power of the DC/DC power conversion stage.

p: the ratio of the direct power, $(P_s - P_c)$, over the total power, P_S.

Assume that the PV output voltage is 450V and the efficiency of the DC/DC power conversion stage, η_C, is 95%. In this case, the power sharing ratio $(1-p)$, from equation (9), of the DC/DC power conversion stage is about 28.6% (=180V/630V) of the rated power of the PV PCS. From the viewpoint of the DC/DC power conversion stage, the load of the DC/DC power conversion stage is heavy. Therefore, the efficiency of the DC/DC power conversion stage is high. Using equation (11) the total efficiency of the proposed converter is obtained as follows:

$$\eta_{new} = p + (1-p)\eta_C = 0.714 + (1-0.714) \times 0.95 = 0.986.$$

On the contrary, in a case where the PV output voltage is 600V and the efficiency of the DC/DC power conversion stage is 80%, the converter efficiency is relatively low because the DC/DC power conversion stage has a light load in this region. The power sharing ratio $(1-p)$ is about 4.8% (=30V/630V) of the rated power of the PV PCS. Then the total efficiency of the proposed converter is obtained as follows:

$$\eta_{new} = p + (1-p)\eta_C = 0.952 + (1-0.952) \times 0.80 = 0.990.$$

In spite of the low efficiency of the DC/DC converter under light load conditions, the proposed topology for the DC/DC conversion stage can still maintain a high overall efficiency. In the small power sharing region, that is, in the region where p is large, since most of the power is directly provided from the PV module to the DC link side of the inverter, the load of the power conversion stage is light and the power conversion stage efficiency is low. However, the total efficiency of proposed power conversion stage is still very high because the contribution of the DC/DC power conversion stage efficiency can be neglected in the low power sharing region of the DC/DC power conversion stage, that is, when $(1-p)$ is very small [7], [13]. The total PV PCS efficiency is described as follows:

$$\eta_S = \eta_{new} \cdot \eta_i \tag{12}$$

where η_S is the total PV PCS efficiency and η_i is the inverter efficiency. Suppose that the inverter efficiency η_i is the same as conventional inverter efficiency. Then the converter efficiency has a strong influence on the total PCS efficiency. In a conventional converter, the efficiency has a large variation depending on the load status. However, in the proposed converter topology, since the converter efficiency is very high despite large variations in load, the total efficiency of PCS is very high throughout the entire load range [7], [13].

V. Experimental Results

The proposed robust PLL algorithm shown in Fig. 3 is implemented with a TMS320F2812 DSP microprocessor. The reference signals $\cos(\omega t)$ and $\sin(\omega t)$ are generated using the frequency from the detector shown in Fig. 2. The grid voltage signal sensed by the A/D converter is multiplied by the reference signals in equation (5). An averaging function is needed to obtain the dc components except for the harmonic components from equation (6). This function is implemented with a ring buffer as shown in Fig. 11. By using a ring buffer, the averaging value can be continuously obtained in each of

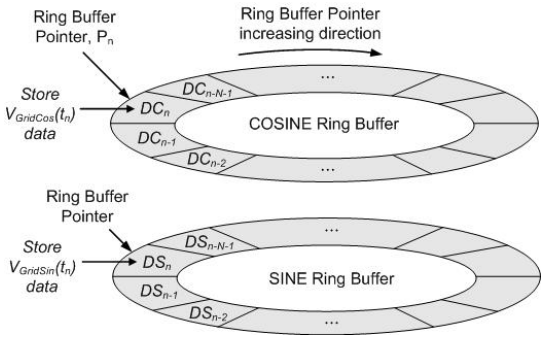

Fig. 11. Ring buffer for one period averaging function.

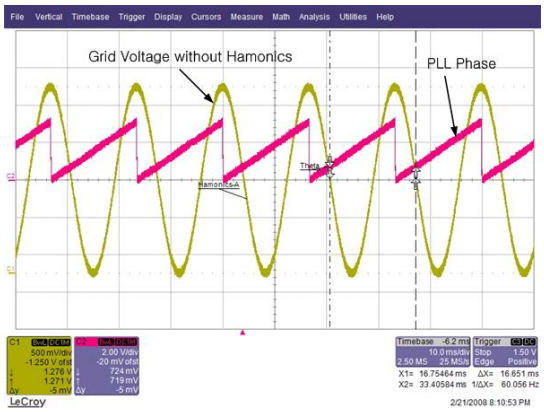

Fig. 12. PLL characteristics for grid voltage without harmonics.

the sampling intervals. The following equation (13) describes the averaging algorithm:

$$\begin{aligned} SC_n &= SC_{n-1} + DC_n - DC_{n-N} \\ V_{GridCosAvg}(t_n) &= \frac{2}{N} SC_n \\ SS_n &= SS_{n-1} + DS_n - DS_{n-N} \\ V_{GridSinAvg}(t_n) &= \frac{2}{N} SS_n \end{aligned} \tag{13}$$

where n is the current sample time, N is the number of buffers, and SC_n and SS_n are the sum of the cosine and sine component buffers at the sample time. The number of buffers is obtained using equation (14).

$$N = \frac{T}{T_s} \tag{14}$$

where T is the period of the grid voltage and T_s is the sampling time. A value of T_s is selected so that N is an integer. The position of the grid voltage is obtained using equation (15) as follows:

$$\begin{aligned} \alpha_n &= \tan^{-1}\left(\frac{V_{GridCosAvg}(t_n)}{V_{GridSinAvg}(t_n)}\right) \\ \theta_n &= \omega t_n + \alpha_n. \end{aligned} \tag{15}$$

Fig. 12 shows that the proposed PLL algorithm demonstrates good performance for producing clear grid voltage waveforms without harmonics. The harmonics independency of the proposed PLL algorithm is shown in Fig. 13. The grid voltage has the following harmonics: 3rd Harmonics: 20%, 5th Harmonics: 10%, 7th Harmonics: 10%.

The distortion of the grid voltage is very serious but the performance of the proposed robust PLL algorithm is not degraded.

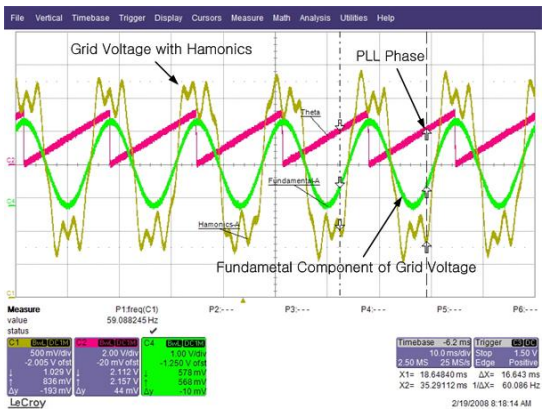

Fig. 13. Harmonics cancellation characteristics of the proposed PLL.

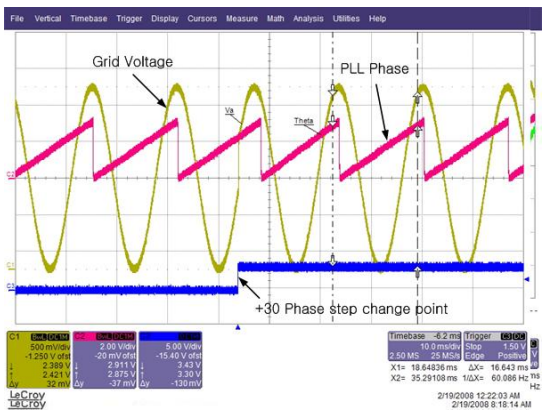

Fig. 14. +30 degree phase jump characteristics of the proposed PLL.

Fig. 14 shows the characteristics of a phase jump in the grid voltage. The proposed PLL algorithm tracks the changed grid voltage well. The performance of the frequency change in the grid voltage is shown in Fig. 15 and 16. The proposed PLL algorithm can track the changed frequency without any fluctuations in the phase information.

Based on the requirements of IEEE standard 929-2000, it is essential that any method of anti-islanding be tested to establish its performance when a parallel RLC load with a specific quality factor Q is used. Fig. 17 shows the experimental equipment consisting of a PV simulator, a grid simulator, a grid impedance and a RLC load for the testing of a photovoltaic power conditioning system in the laboratory.

Fig. 18 shows Case 1 where a parallel RLC load with a quality factor of 1.0 in accordance with the IEEE Standard 1547.1 was used. As can be seen, the islanding detection performs very well. Fig. 19 represents Case 2 where a parallel RLC load with a quality factor of 2.5 in accordance with the IEEE Standard 929-2000 was used. The proposed method proved to be both robust and effective.

A complete grid-connected 250kW PCS consisting of four high efficiency DC/DC power conversion stages is shown in Fig. 20.

A complete system with four high efficiency DC/DC converters is shown in Fig. 21. The experimental waveforms of the grid voltage and output current of a PCS at 250kW PCS output is shown in Fig. 22. The THD of the output current is under 3% in rated power region. The proposed robust PLL algorithm implemented on the 250kW PV PCS has stable performance.

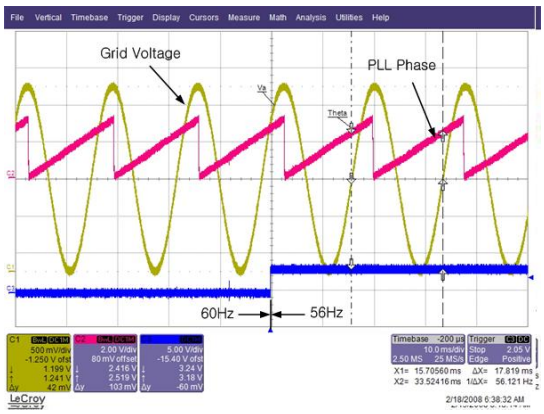

Fig. 15. Frequency jump characteristics of the proposed PLL from 60Hz to 56Hz.

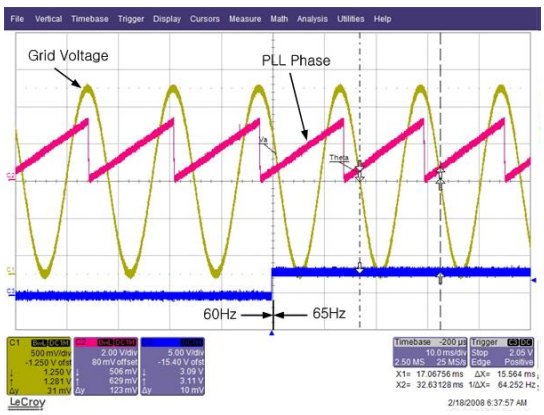

Fig. 16. Frequency jump characteristics of the proposed PLL from 60Hz to 65Hz.

Fig. 17. Experimental equipment for PV PCS test.

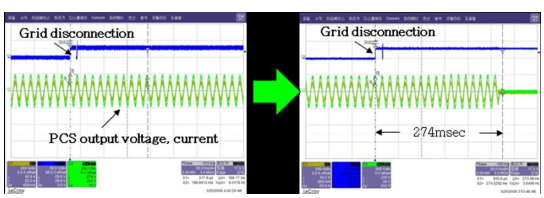

Fig. 18. Islanding detection in the case of RLC load with a Q=1.0.

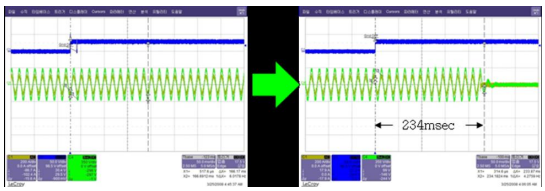

Fig. 19. Islanding detection in the case of RLC load with a Q=2.5.

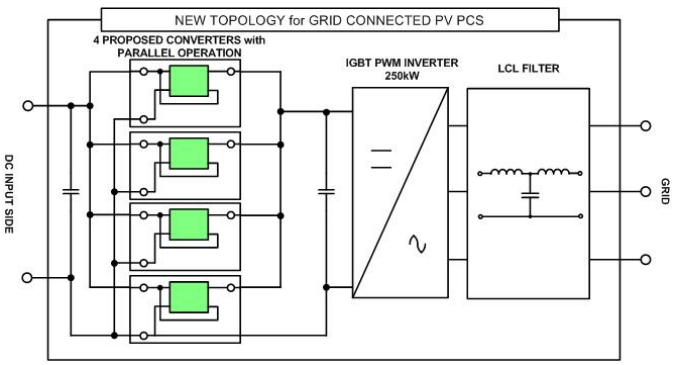

Fig. 20. System diagram of 250kW grid connected PV PCS.

In a PV system, since the load of the system changes from light to heavy daily, the light load characteristics of the PCS are very important to get the maximum energy from a PV generation system. As shown in Fig. 23, the proposed system has a very high European efficiency in the normal operating range of a PV generation system over 550V. From this point of view, the proposed topology is very good for a PV PCS.

VI. Conclusions

In this paper, an active voltage and frequency with a positive feedback in the *d-q* frame anti-islanding method suitable for a robust phase-locked loop (PLL) algorithm using the FFT concept was proposed. Since the FFT concept, which can extract only the fundamental component from a noisy source signal is used, the proposed PLL algorithm is very robust under noisy conditions. The proposed algorithm has no PI gain tuning processor and is not influenced by the swell, sag, unbalance conditions or harmonics of the grid. The programming method of the proposed algorithm is proposed using the ring buffer in a DSP microprocessor. This PLL algorithm can be applied to single phase systems without any changes. Islanding prediction is a necessary feature for inverter-based photovoltaic (PV) systems in order to meet the stringent standard requirements for interconnection with the electrical grid. Both passive and active anti-islanding methods exist. Typically, active methods modify a given parameter, which also affects the shape and quality of the grid injected current. In this paper, an active voltage and frequency with a positive feedback in the *d-q* frame anti-islanding algorithm was proposed. To prove the effectiveness of the proposed algorithm, the robust PLL algorithm was implemented for a 250kW PV PCS. The simulations and experimental results show that the proposed PLL and the anti-islanding algorithm demonstrate good performance.

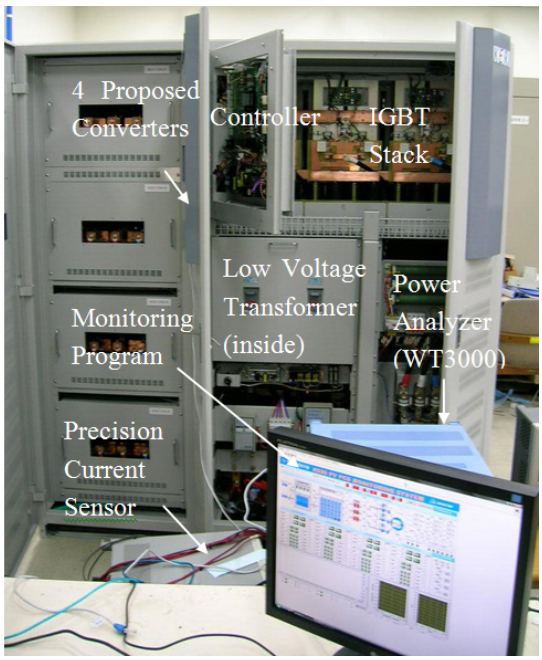

Fig. 21. Implemented 250kW PV system with the proposed algorithm.

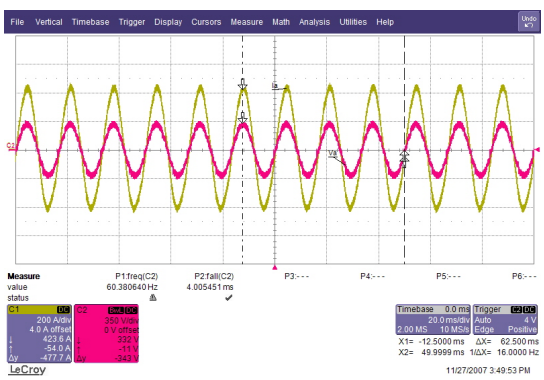

Fig. 22. Experimental waveforms of grid voltage and output current of PCS at 250kW PCS output(C1: PCS output current(200A/div), C2:Grid phase voltage(200V/div).

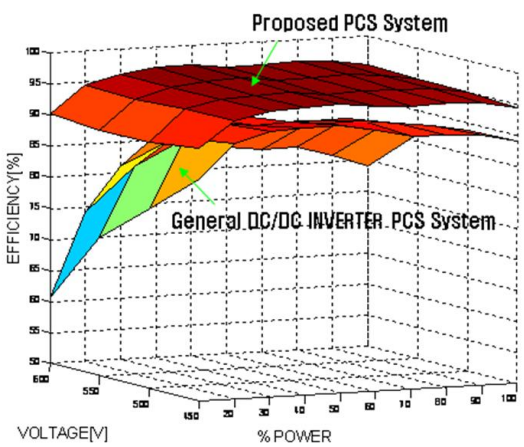

Fig. 23. Efficiency curve of Implemented 250kW PV system with the proposed algorithm.

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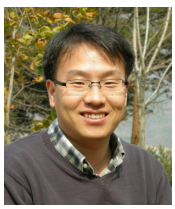

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