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Enhanced Dynamic Response of SRF-PLL System for High Dynamic Performance during Voltage Disturbance

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Abstract

Usually, a LPF (low pass filter) is used in the feedback loop of a SRF (synchronous reference frame) - PLL (phase locked loop) system because the measured grid voltage contains harmonic distortions and sensor noises. In this paper, it is shown that the cut-off frequency of the LPF should be designed to suppress the harmonic ripples contained in the measured voltage. Also, a new design method for the loop gain of the PI-type controller in the SRF-PLL is proposed with consideration of the dynamics of the LPF. As a result, a better transient response can be obtained with the proposed design method. The LPF frequency and the PI controller gain are designed in coordination according to the steady state and dynamic performance requirements. Furthermore, in the proposed method, the controller gain and the LPF cut-off frequency are changed from their normal value to a transient value when a voltage disturbance is detected. This paper shows the feasibility and usefulness of the proposed methods through the computer simulations and experimental results.

Key Words: Linearized modeling, Modeling of PLL System, Unbalanced fault, Variable gain

I. INTRODUCTION

The phase angle and magnitude of grid voltage should be determined accurately for grid connected operation of all kinds of distributed resources. The important transient periods include not only the transients of the grid connection but also the abrupt changes in grid voltage due to grid faults. The phase-locked loop (PLL) is the most common technique for grid connected power converters and power quality interface devices such as UPS, APF, and UPQC. [1], [4]

To avoid steady state errors, many conventional PLL systems determine the phase angle using a PI-type feedback controller in the synchronous reference frame. However, a LPF (low-pass filter) is used in the feedback loop of a SRF (synchronous reference frame) - PLL (phase locked loop) system because the measured grid voltage contains harmonic distortions and sensor noises. Also, in case of unbalanced voltage conditions, such as a single line ground fault, only the positive sequence component of the output voltage is used for the calculation of the feedback voltage in the synchronous reference frame.

Due to nonlinear loads connected to the power system, grid voltage contains low-order harmonics such as the 5th, 7th, 11th and 13th harmonics.

Also voltage measurement can be influenced by the switching operations of nearby power electronics due to a switching frequency of several kHz with high power ratings.

Therefore, the response of a PLL system is investigated for voltage harmonics and voltage disturbances with a step change of voltage magnitude and phase angle. The phase detection method in [1] has two features for effective angle detection during voltage distortions. Fig.1 is a computation block of the positive sequence voltage for unbalanced voltage conditions. The other is a low pass filter for the voltage in the synchronous reference frame for the reduction of voltage harmonics. However, the design guidelines for the PI controller gain or the LPF cut-off frequency meet the requirements of the dynamic response of a PLL system.

In [2], it is shown that the phase angle can be calculated accurately by the decoupling of the cross-coupling voltages in the double synchronous reference frame. However, the configuration of the decoupling compensation can be complex if the source voltage contains various orders of harmonics. Also, the dynamic response to the phase jump of the voltage source can be degraded due to the different response characteristics of the LPF which is located at the output of each synchronous reference frame.

A linearized model of a SRF-PLL system is presented to analyze the dynamic response of the PI-type feedback

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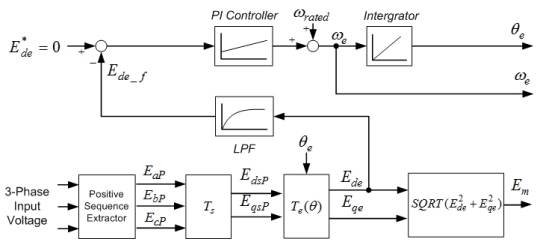

Fig. 1. Block diagram of conventional three-phase PLL system.

controller in the system. The optimized closed loop bandwidth of the PLL system is increased up to 1 kHz [4]. The analysis does not considered an LPF which is common in real world applications for the effective and robust filtering of voltage harmonics and sensor noises. The worse angle detection performance is obtained in the case of voltage unbalance and harmonics without an LPF. This paper shows the feasibility and usefulness of the proposed methods through computer simulations and lab-scale experiments.

II. Design of the SRF-PLL System

A. A Conventional SRF-PLL System with a Positive Sequence Extractor

Fig. 1 shows a block diagram of a conventional SRF-PLL system with a positive sequence extractor in the d-axis synchronous reference frame voltage. To eliminate the voltage unbalance effects, a positive sequence extractor is used as an input of the SRF-PLL system [1].

When input 3-phase voltages contain only fundamental components, the synchronous reference frame voltages have pure dc values.

However, the grid voltage usually contains harmonics due to nonlinear elements such as transformers and rectifier loads. Also the measurement of grid voltage can contain switching noise and ripples.

If low-order harmonics such as the 5th, 7th, 11th, and 13th are dominant in the system voltage, the 4th, 6th, 10th and 12th order ripples are invariantly contained in the feedback signal of the SRF-PLL system.

As the phase angle is aligned to the q-axis synchronous voltage, the reference value of the d-axis synchronous voltage is always zero. The PI controller outputs the frequency for the compensation of the phase error without steady state errors. The feedforward term of the rated frequency (60Hz) helps the dynamic performance of the PI controller because the PI controller only needs to take care of the deviation of the phase angle.

In some applications both the phase angle and the magnitude of grid voltage are necessary. In that case, the square root of the sum of the squares of the d-axis and q-axis voltages represents the magnitude as shown in Fig. 1.

B. Effective Low-Pass Filtering of Voltage Harmonics

It is assumed that the three phase voltage, E_a, E_b, E_c contains 5% of 5th-order and 5% of 7th-order harmonics from the moment of 100msec in Fig. 2(a).

The amount of ripple voltage contained in the input is shown in Fig. 2(b). Even though the phase angle, θ_e error can not

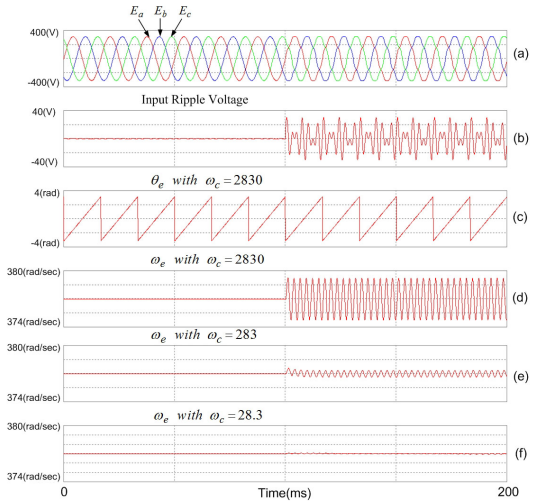

Fig. 2. Reduction of harmonics with LPF cut-off frequency ($k_p = 0.0909$, $K_i = 1.2861$). (a) Grid voltage. (b) Harmonics(5th and 7th). (c) Grid phase angle($\omega_c = 2830\,[rad/\sec]$). (d) Grid frequency ($\omega_c = 2830\,[rad/\sec]$). (e) Grid frequency ($\omega_c = 283\,[rad/\sec]$). (f) Grid frequency ($\omega_c = 28.3\,[rad/\sec]$).

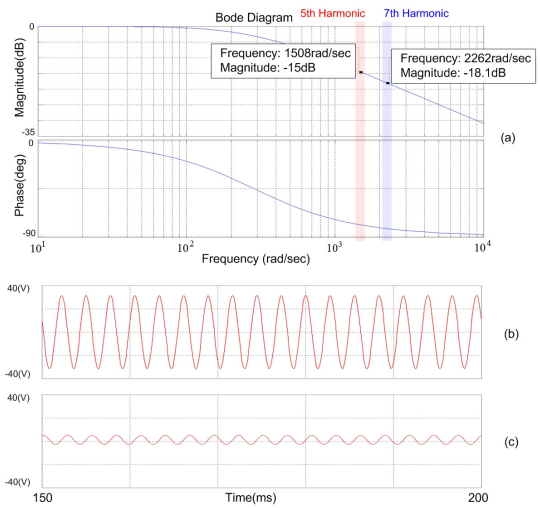

Fig. 3. LPF bode plot and E_{de_f}. (a) LPF bode plot ($\omega_c = 283\,[rad/\sec]$). (b) E_{de_f} without LPF. (c) E_{de_f} with LPF ($\omega_c = 283\,[rad/\sec]$).

be recognized well in Fig. 2 (c), the output frequency, ω_e which is the derivative of the phase angle, θ_e shows a large ripple at 5th order harmonic frequency with the LPF cut-off frequency $\omega_c = 2830\,[rad/\sec]$in Fig. 2(d). For a comparison, the output frequencies with the LPF cut-off frequencies $\omega_c = 283\,[rad/\sec]$ and $\omega_c = 28.3\,[rad/\sec]$ are shown in Fig. 2(e) and (f) respectively.

It is shown that the low-order harmonics can be suppressed effectively by the selection of a low cut-off frequency for the LPF.

Fig. 3 provides a guideline for the selection of a cut-off frequency for the LPF. When the lowest order harmonic attenuation level is decided, the cut-off frequency of the first order LPF can be chosen.

In this example, to obtain -15dB of the 5th order harmonic frequency, the selected cut-off frequency of the LPF is 283 [rad/sec] using the bode plot in Fig. 3(a).

In Fig. 3(b) the d-axis synchronous reference frame voltage shows a large ripple.

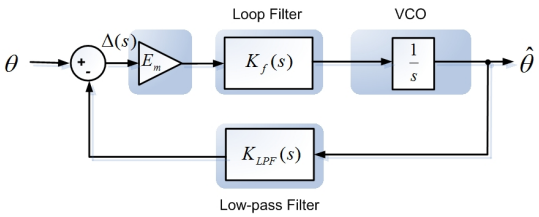

Fig. 4. Linearised PLL model with consideration of LPF.

On the other hand, the voltage ripple in Fig. 3(c) is reduced down -15dB with the LPF($\omega_c = 283[rad/\sec]$).

However the reduced value of the LPF cut-off frequency can cause a delay in the feedback voltage of the PLL. As a result the dynamic response of the PLL system is limited due to the low cut-off frequency of the LPF even though the PI controller gain is high enough. The slow dynamic response of the PLL system during voltage transient can be a problem when a fast control response is required such as with LVRT (low voltage ride through) applications for distributed generators.

C. Modeling of a PLL System with the Consideration of a LPF

The linearized modeling of a SRF-PLL system without a LPF was introduced in [4]. The linearized modeling method of a SRF-PLL system is based on a couple of assumptions.

Assumption 1: The coordinate transformation and the positive sequence extractor are ideal.
Assumption 2: The voltage variation in the synchronous reference frame can be regarded as linear with respect to the phase angle deviation.

If these assumptions meet the requirements, the closed loop PLL system can be modeled as in Fig. 4.

The loop filter in a general PLL system is replaced with a PI controller as (1) and the VCO is represented as an integrator.

$$K_f = K_p \cdot (\frac{1+s\tau}{s\tau}). \tag{1}$$

Note that the magnitude of the voltage, E_m is located in the middle of the loop. The low pass filter is a first order digital filter with the cut-off frequency, ω_c in (2).

$$K_{LPF}(s) = \frac{\omega_c}{s+\omega_c}. \tag{2}$$

The open-loop transfer function T(s) is in (3) and the closed-loop transfer function is in (4) including the LPF model in the denominator. Because of the low-pass filter, the closed loop transfer function has been 3rd order. In order to meet the desired dynamic response of the PLL system, the prototype transfer function was used as (5). Namely, the first term in (5) is used for the pole-zero cancellation method and the closed loop dynamics can be simplified to a 2nd order prototype transfer function form. As a result, the dynamics of the PLL system are determined by ω_n and ζ.

$$T(s) = E_m \cdot \ K_f(s) \cdot \ \frac{1}{s} \tag{3}$$

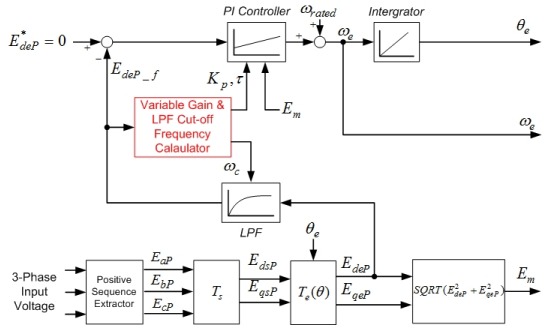

Fig. 5. Block diagram of proposed variable parameter PLL system.

$$H_{c\_LPF} = \frac{T(s)}{1+T(s)\cdot K_{LPF}(s)} \tag{4}$$

$$H_{c\_LPF\_\text{model}} \cong \frac{s+\alpha}{s+\alpha} \cdot \frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}. \tag{5}$$

When $\alpha = 1$, (6) and (7) can be obtained from (4) and (5). (6) should have a relationship with the low-pass filter cutoff frequency and the PLL system bandwidth. The proportional gain (K_p) and time constant (τ) of the PI-type loop filter controller can be decided as (7).

$$\omega_c = 1+2\zeta\omega_n \tag{6}$$

$$K_p = \frac{2\zeta\omega_n}{E_m}, \tau = \frac{E_m \cdot K_p \cdot \omega_c}{\omega_n^2}. \tag{7}$$

III. Proposed Variable Parameter PLL Method

Typically, an accurate phase angle is important because the voltage phase angle is used for control in 3-phase grid connected inverter when the grid voltage magnitude and the phase angle are suddenly changed during a grid fault. However, it is hard to pick up the phase detection speed in a PLL system, because feedback loop of a PLL system includes a LPF. To resolve this problem, this paper proposes a method using the variable controller gain and the LPF cut-off frequency.

The controller gain and the LPF cut-off frequency are changed from normal values to transient values when a voltage disturbance is detected. Since the steady-state error of a PLL system is almost zero and only a ripple, the criterion of the normal range was set up to be less than 5% of the phase voltage.

If you want a faster transient response, the criterion of the normal range considering the d-axis voltage ripple in the synchronous reference frame should be chosen.

Fig. 5 shows a block diagram of the proposed variable parameter PLL system. The proposed parameter calculation block in the form of a flowchart is shown in Fig. 6. The PLL input error, E_{deP_f} does not exceed the set limits to determine the normal condition. In this case, the values of the normal controller bandwidth and the LPF cutoff frequency are set to reduce the effects of the 5th and 7th harmonics and noises.

However, E_{deP_f} exceeding the set value is determined as a transient state. In this case, the controller bandwidth and the LPF cutoff frequency is set to reduce delays and enhance the detection speed.

In the proposed method, the controller gain and the LPF cut-off frequency are changed from the normal value to

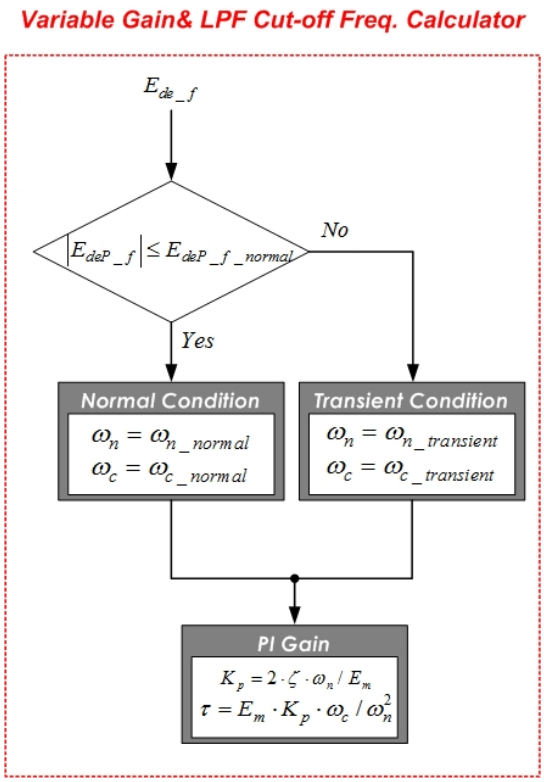

Fig. 6. Calculation flowchart of the variable controller gain and LPF cut-off frequency.

TABLE I
SIMULATION PARAMETERS

Symbol	Description	Value
T_{samp}	Digital sampling time	100[usec]
$E_{de\_f\_normal}$	Criterion of normal range	10[V]
ω_{n_normal}	Controller bandwith in normal state	200[rad/sec]
$\omega_{n\_transient}$	Controller bandwith in transient state	1413[rad/sec]
ω_{c_normal}	LPF Cutoff frequency in normal state	283[rad/sec]
$\omega_{c\_transient}$	LPF Cutoff frequency in transient state	2000[rad/sec]

the transient value when a voltage disturbance is detected. Therefore, the PLL system is robust for noise and harmonic influence in the steady state and fast in the transient state.

IV. SIMULATION

To verify the response of the PLL system with the proposed design method, various simulations have been performed. The parameters for the simulations are given in Table 1. In this paper, the steady-state voltage is assumed to contain 10% harmonics. Out of consideration for the 5th and 7th harmonics ripple and margin, the criterion of the normal range was set to 3% of the phase voltage. This criterion for the normal range can be adjusted depending on the grid conditions. The simulation package used in this study is PSIM with a C language interface using the DLL (dynamic link library).

A comparison is made between the dynamic responses of PLL systems during voltage disturbances with the conventional and the proposed design methods. As shown in Fig. 7 (a), an abrupt voltage disturbance is applied with a 1 phase fault for 0.1sec (6 cycles). It is found that the step phase jump is one of the most severe conditions among the voltage disturbances for the test of the PLL system dynamics. In Fig. 7 and Fig. 8, the LPF is included in the simulation model with ω_c=283

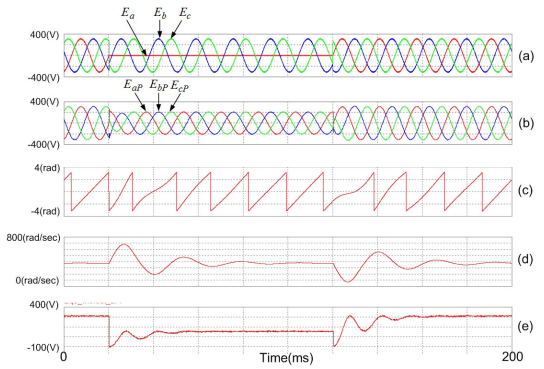

Fig. 7. PLL dynamics simulation without the consideration of LPF. (a) Grid voltage (b) Positive sequence voltage. (c) Phase angle. (d) Frequency. (e) SRF-Q axis voltage.

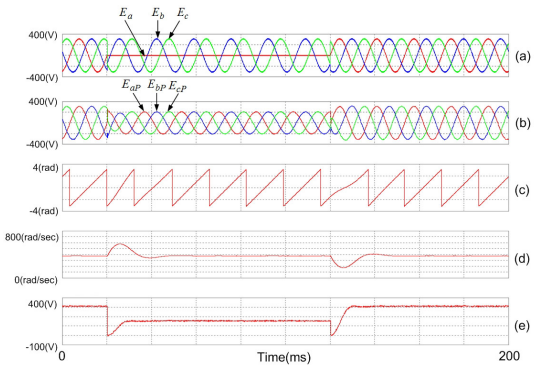

Fig. 8. PLL dynamics simulation with the consideration of LPF. (a) Grid voltage. (b) Positive sequence voltage. (c) Phase angle. (d) Frequency. (e) SRF-Q axis voltage.

rad/sec. The difference comes from the design method of the PI controller gain. The K_p and the tau are calculated from the 2nd order prototype transfer function without consideration of the LPF resulting in K_p = 0.909 and τ= 0.0071 in Fig. 7. The phase angle, θ_e in (c) and the frequency, ω_e in (d) have large oscillations. The Q-axis voltage is plotted in Fig. 7 (e). Even though the phase angle and the q-axis voltage have oscillations due to the phase angle error in the transient, the magnitude of the voltage directly calculated from the d-axis voltage and the q-axis voltage has almost a perfect response to the actual voltage magnitude.

Correct calculation of the voltage magnitude is very important for both the dynamic current control and for the correct design of the PI controller gain of the PLL system because the magnitude is included in (7).

On the other hand, the PLL response during the same conditions as Fig. 7 is shown in Fig. 8 with consideration of the LPF. The PI controller gain is $K_p = 0.909$ and $\tau = 2.01$ in Fig.8. The transient time in this case is about 16msec (1 cycle) with a system bandwidth of ω_n=200 rad/sec.

For a better dynamic response, both the system bandwidth and the cut-off frequency of the LPF should be increased at the expense of the loss of the attenuation effect of the voltage harmonics and noises.

The dynamic response of the PLL system with different system bandwidths and cut-off frequencies of the LPF are compared in Fig. 10 during the same voltage disturbance condition. The voltage disturbance in Fig. 10 is the same as

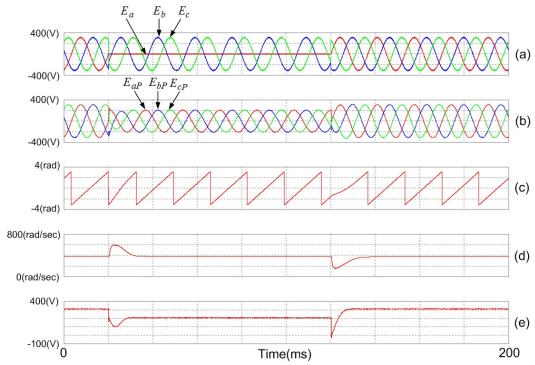

Fig. 9. PLL dynamics simulation with the proposed method. (a) Grid voltage. (b) Positive sequence voltage. (c) Phase angle. (d) Frequency. (e) SRF-Q axis voltage.

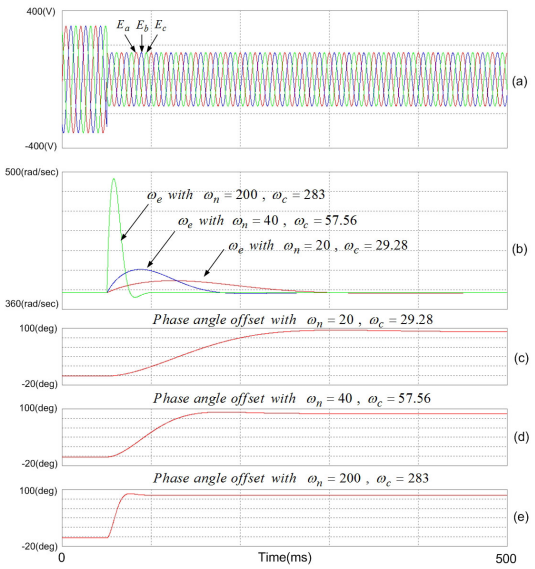

Fig. 10. Comparison of the dynamic responses of the PLL system with the proposed design method for PI controller under the same voltage disturbance. (a) Grid voltage. (b) Frequency. (c) Phase angle offset ($\omega_n = 20, \omega_c = 29.28$). (d) Phase angle offset ($\omega_n = 40, \omega_c = 57.56$). (e) Phase angle offset ($\omega_n = 200$, $\omega_c = 283$).

the case in Fig. 8, which is a 1 phase fault. In Fig. 10 (c), the phase angle offset (the integral of the output of the PI controller) is plotted when the system bandwidth is 20 rad/sec and the cut-off frequency of the LPF is 29.28 rad/sec. The phase angle offset with a system bandwidth of 40 rad/sec and a cut-off frequency of 57.56 rad/sec is plotted in Fig. 10 (d). The same graph is plotted with a system bandwidth of 200 rad/sec and a cut-off frequency of 283 rad/sec in Fig. 10 (e). The output frequencies of these three cases are compared in Fig. 10 (b), which shows that the proposed design method for the PLL dynamics is very effective.

Fig. 9 shows the proposed PLL response during the same conditions as in Fig. 7. The normal PI controller gain is $K_p = 0.909$, $\tau = 2.01$, $\omega_c = 283\,[rad/\sec]$ and the transient PI controller gain is $K_p = 6.42$, $\tau = 2.001$, $\omega_c = 2000\,[rad/\sec]$ in Fig. 9. The transient time in this case is about 8msec (0.5 cycle)

V. Experimental Results

An experimental set-up is prepared for the test of the proposed method as shown in Fig. 11. Due to the limitations in

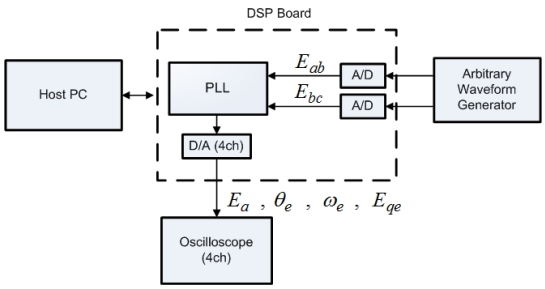

Fig. 11. Experimental setup for PLL Dynamics Test.

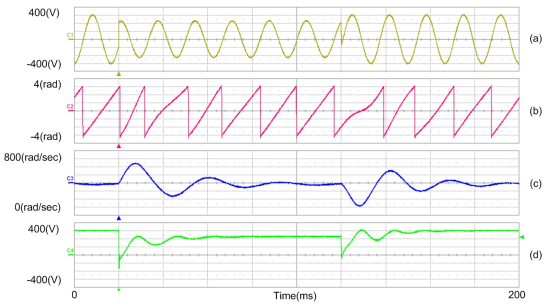

Fig. 12. PLL dynamics experiment result with the consideration of LPF. (a) Positive sequence voltage (E_{aP}). (b) Phase angle. (c) Frequency. (d) SRF-Q axis voltage.

the number of channels in the arbitrary waveform generator and the oscilloscope, only 4 variables are displayed in the experimental results in Fig. 12 , Fig. 13 and Fig. 14.

The positive sequence a-phase voltage waveform with the same conditions as the simulation is shown in Fig. 12 (a). The phase angle and the output frequency and the q-axis SRF voltage are shown in Fig. 12 (b), (c), and (d), respectively, when the PI controller gain is selected without consideration of the LPF. The same variables are plotted in Fig. 13 with the PI controller gain calculated from (7). Like the simulation results, the experimental results prove the excellence of the proposed design method for a PLL system when compared to the conventional one.

VI. Conclusions

A new method is proposed and evaluated to improve the dynamic response of a SRF-PLL system which is one of the most important features for the robust operation of a distributed generation system during grid voltage disturbances. A LPF is usually used in a SRF-PLL system for the suppression of voltage harmonics and noises having a wide spectrum of frequencies. A new design method for the system bandwidth and the loop gain according to the cut-off frequency of the LPF is proposed. The dynamic response of the PLL system is improved using the proposed method when a voltage disturbance occurs. The desired dynamic response of the PLL system can be obtained with the proper combination of the system bandwidth and the cut-off frequency of the LPF. Furthermore, the proposed variable parameter PLL system has automatic changes in the loop parameters during voltage disturbances which results in further improvement of the dynamic response of the phase angle detection. The feasibility and performance is tested and verified through computer simulations and DSP-based experiments.

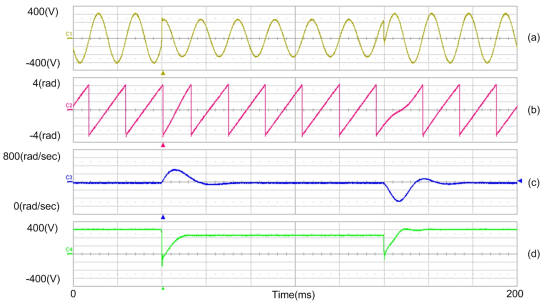

Fig. 13. PLL dynamics experiment result with the consideration of LPF. (a) Positive sequence voltage (E_{aP}). (b) Phase angle. (c) Frequency. (d) SRF-Q axis voltage.

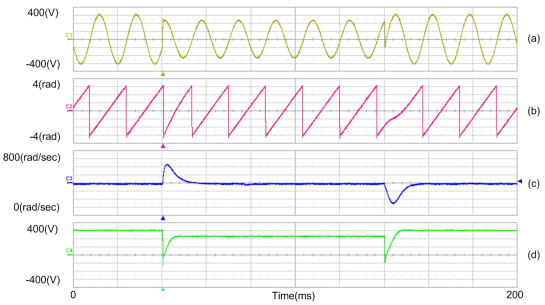

Fig. 14. PLL dynamics experiment result with the proposed method. (a) Positive sequence voltage (E_{aP}). (b) Phase angle. (c) Frequency. (d) SRF-Q axis voltage.

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