

A Three-Phase High Frequency Semi-Controlled Battery Charging Power Converter for Plug-In Hybrid Electric Vehicles

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Abstract

This paper presents a novel analysis, design, and implementation of a battery charging three-phase high frequency semi-controlled power converter feasible for plug-in hybrid electric vehicles. The main advantages of the proposed topology include high efficiency; due to lower power losses and reduced number of switching elements, high output power density realization, and reduced passive component ratings proportionally to the frequency. Additional advantages also include grid economic utilization by insuring unity power factor operation under different possible conditions and robustness since short-circuit through a leg is not possible. A high but acceptable total harmonic distortion of the generator currents is introduced in the proposed topology which can be viewed as a minor disadvantage when compared to traditional boost rectifiers. A hysteresis control algorithm is proposed to achieve lower current harmonic distortion for the rectifier operation. The rectifier topology concept, the principle of operation, and control scheme are presented. Additionally, a dc-dc converter is also employed in the rectifier-battery connection. Test results on 50-kHz power converter system are presented and discussed to confirm the effectiveness of the proposed topology for PHEV applications.

Key Words: Battery control strategy, Plug-in hybrid electric vehicles, Power factor control, Three-phase PWM rectifiers

I. INTRODUCTION

Plug-in hybrid electric vehicles (PHEVs) are gaining popularity because of the environmental consideration “Go green” factor. PHEV is a hybrid electric vehicle (HEV) with a very high capacity battery pack that can be recharged by plug-in to the power in a local grid, where the power generation source can be in the form of renewable energy such as wind, solar, etc [1]. The Electric Power Research Institute (EPRI) projects that by 2050, 62% of the entire US vehicle fleet would consist of PHEVs [2]. Other than having the environmental benefits and lessening the nation’s dependence on oil, PHEVs also have the potential for providing peak power shaving via V2G (Vehicle to Grid) and powering home in emergency situations via V2H (Vehicle to Home).

Although most of the HEVs currently available on the market are equipped with Ni-MH batteries, the lead-acid batteries are still attractive and used in the mild HEVs, which have relatively restricted functions and require consideration of cost effectiveness. Lead-acid batteries represent both reasonable cost and high reliability in automotive applications, but they generally show some drawbacks in cycle life, power character-

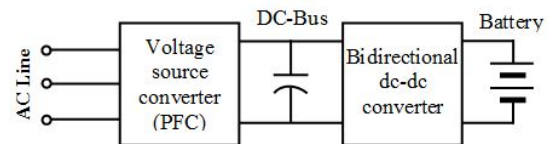


Fig. 1. Block diagram of battery charger for PHEV.

istics, and weight, etc. Studies to improve their performance are being continuously performed, and different viewpoints have arisen providing resolutions other than strictly improving the battery itself [3]-[6]. Moreover, further improvement could be achieved when a proper storage device is selectively used corresponding to respective charging status and vehicle driving conditions, which can be called an advanced Hybrid Energy Storage System (advancedHESS) [7].

High frequency (HF) operation of power converters have become a mature technology with several international manufacturers of power electronic devices [8]-[13]. Recent power converters tend to increase switching frequency to reduce the size and volume of the passive components; inductors and capacitors. However, HF operation increases semiconductor device switching loss, which is proportional to the switching frequency [14]. The latest power semiconductor devices have a fast turn-on and turn-off capability to reduce the switching loss at HF operation [15]-[17].

A PHEV requires an ac outlet charging system for charging the battery. Usually ac-dc converters are used in a number

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of applications such as power supply, household electric appliances, battery charger, etc. Depending on the switching frequency they are classified as converters with low switching frequency and those with high switching frequency [18], [19].

Conventional uncontrolled rectifiers and line commutated phase controlled rectifiers so far have dominated the ac-dc power conversion. Such converters have inherent drawbacks such as harmonics in the input current and output voltage; low input power factor especially at low output voltage since these conventional rectifiers draw non-sinusoidal currents from the grid [20]. Since power devices demand reactive power in addition to active power, a charger with low power factor increases burden on the connecting power system.

On the other hand, harmonics have a negative effect in the operation of the electrical system. Therefore, an increasing attention is paid to their mitigation and control. The problems due to harmonics in conventional rectifiers have resulted in the establishment of standards such as IEC 61000-3-2 and IEEE Std 519TM-1992 [21], [22]. Thus, a PHEV charger with a Power Factor Correction (PFC) based ac-dc converter is desirable.

Voltage source converter or synchronous link converter is the best solution under such situation, which has both rectification and regeneration capability. The input current in these converters flows through the inductor which can be wave shaped with appropriate current mode control. These converters have high efficiency and inherent power quality improvement at the ac input and dc output [23].

In this paper, a new battery charging topology feasible for PHEV applications is proposed. This topology consists of a three-phase high frequency semi-controlled rectifier and dc-dc converter. The block diagram of this battery charger is shown in Fig. 1. Robustness, simplicity, low cost, and high efficiency are inherent characteristics because high frequency and few semiconductor elements are used. The operating principle, theoretical analysis, as well as experimental results obtained from a 50-kHz prototype are presented and discussed.

This paper is organized as follows: The proposed conversion topology dynamic modeling is explained in Section II. In Section III, PI controller design for maintaining the dc link voltage and hysteresis controller design for the current control is described. In Section IV, the hardware implementation and experimental results for the proposed PHEV charging system are illustrated. Some conclusions are given in Section V.

II. THE PROPOSED CONVERSION TOPOLOGY

The semi-controlled rectifier structure, which is proposed here, uses three insulated-gate bipolar transistors (S1-S3 IGBTs) and three diodes (D1-D3), is shown in Fig. 2 [8]. The main advantages of the proposed topology over the traditional fully-controlled topology are:

- 1) All switches are connected to the same reference in rectifier stage; simplifying the command circuit.
- 2) Protection; as short-circuit through a leg is not possible.
- 3) Higher efficiency; due to less number of switches.
- 4) Smaller size; since passive elements are reduced proportionally due to high frequency operation.
- 5) Unity power factor (UPF) operation can be achieved.

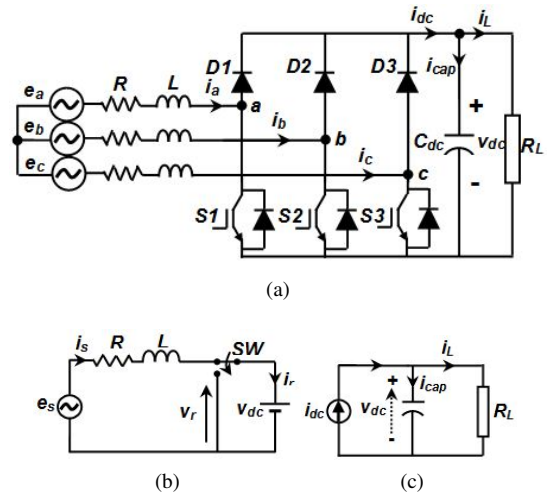


Fig. 2. Ac-dc PWM semi-controlled rectifier. (a) Power circuit, (b) per-phase input equivalent circuit, (c) output equivalent circuit.

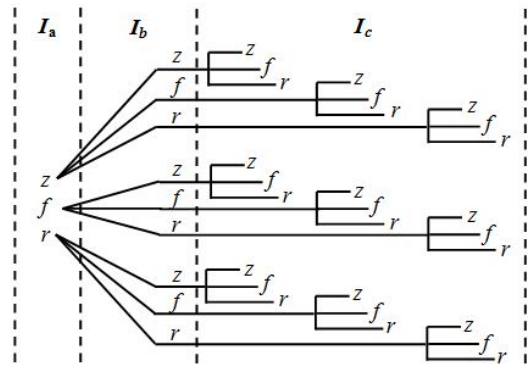


Fig. 3. All possible combinations for converter current flow.

A. Power Transfer Operation

The proposed rectifier in Fig. 2 operates as a boost rectifier. When any switch S1, S2, or S3 is turned on then the current will flow through it and respective input inductor current will increase, while respective diode D1, D2, or D3 is reverse biased (off). On the other hand, when S1, S2, or S3 is turned off then the current will flow through the respective diode D1, D2, or D3 (forward biased) and energy will be transferred to dc-bus.

According to current direction, three states are representing each phase current I_a , I_b , and I_c . These states can be simplified as: zero (z), forward (f), and reverse current flow (r), resulting in 27 different states as shown in Fig. 3. Only 12 states are physically implemented as shown in Table I. There are three states (10, 11, and 12) will not be implemented for rectification mode of operation; since no power will be transferred to dc-bus. The other nine states can be subdivided into three groups; (1, 4, and 7), (2, 5, and 8), and (3, 6, and 9). Therefore, states 1-3 will be repeated with 4-6 as well as 7-9.

Fig. 4 shows the current waveforms for all rectification

TABLE I
THE PHYSICAL VALID CURRENT FLOW FOR RECTIFIER OPERATION

	1	2	3	4	5	6	7	8	9	10	11	12
I_a	f	F	f	f	z	r	r	r	z	f	r	r
I_b	f	Z	r	r	r	z	f	f	f	r	f	r
I_c	r	R	z	f	f	f	f	z	r	r	r	f

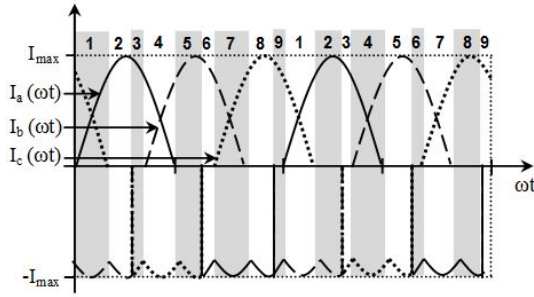


Fig. 4. Theoretical current waveforms for the nine rectification physical states.

possible states 1-9 where only the positive half cycle is modulated while negative half cycle is uncontrolled.

B. Rectifier Dynamic Model

The semi-controlled rectifier structure, which is proposed here, uses three insulated-gate bipolar transistors (S1-S3 IGBTs) and three diodes (D1-D3). A power circuit, per-phase and output equivalent circuits of a three-phase semi-controlled rectifier are shown in Fig. 2. It is assumed that a resistive load R_L is connected to the output terminal. An input voltage equation is derived from Fig. 2(b):

$$e_s = Ri_s + L \frac{di_s}{dt} + v_r \quad (1)$$

where e_s is the source voltage, i_s is the ac-current, v_r is the rectifier input voltage, and R, L are the resistance and inductance of the boosting inductor, respectively. The instantaneous average voltages (V_{s1} , V_{s2} , and V_{s3}) seen by each phase are given by:

$$\begin{bmatrix} V_{s1}(t) \\ V_{s2}(t) \\ V_{s3}(t) \end{bmatrix} = \begin{bmatrix} (1 - D_{s1}(t)) \\ (1 - D_{s2}(t)) \\ (1 - D_{s3}(t)) \end{bmatrix} V_{dc} \quad (2)$$

where $D_{s1}(t)$, $D_{s2}(t)$, and $D_{s3}(t)$ are instantaneous functions of the effective duty cycle of switches $S1$, $S2$, and $S3$, respectively. Considering the ac-source voltages balanced and the presence of the neutral conductor, and applying the Kirchhoff's law and Laplace transform, the dynamic model of the rectifier is obtained and given in matrix form by:

$$\begin{bmatrix} I_a(s) \\ I_b(s) \\ I_c(s) \end{bmatrix} = \frac{1}{3L_s} \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix} \begin{bmatrix} V_{s1}(s) \\ V_{s2}(s) \\ V_{s3}(s) \end{bmatrix} \quad (3)$$

For fast voltage control, the input power should supply instantaneously the sum of load power and charging rate of the capacitor energy. On the dc-output side in Fig. 2(c):

$$i_{dc} = C_{dc} \frac{dv_{dc}}{dt} + i_L \quad (4)$$

where v_{dc} , i_{dc} , C_{dc} are the dc-link output voltage, current, and filter capacitor, respectively. i_L is the load current.

C. Bidirectional DC-DC Converter

Bidirectional (regenerative) power flow can be obtained with a current-bidirectional two quadrant realization of the switch network. An example is illustrated in Fig. 5, in which a dc-dc converter interfaces batteries to the main dc power bus of a

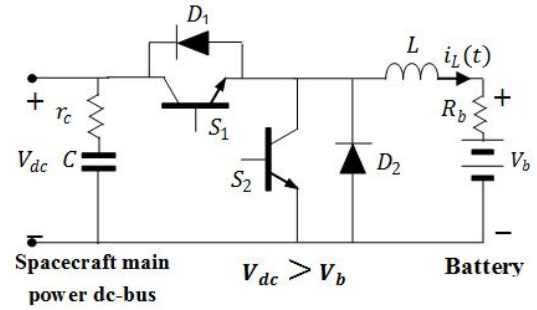


Fig. 5. A buck converter with two-quadrant switches and bidirectional power flow. Battery charger / discharger example.

spacecraft. The anti-parallel-connected transistors and diodes form current-bidirectional switches. Switch $S2$ is driven with the complement of the $S1$ drive signal, such that $S2$ is off when $S1$ is on, and vice-versa. To charge the battery, the inductor current $i_L(t)$ is positive and flows through transistor $S1$ and diode $D2$. To discharge the battery, the current $i_L(t)$ reverses polarity, and flows through transistor $S2$ and diode $D1$. In both cases, the battery voltage is less than the main dc bus voltage. The magnitude and polarity of the battery current can be controlled via adjustment of the duty cycle D .

To design the control system of a converter, it is necessary to model the converter dynamic behavior.

In particular, it is of interest to determine how variations in the power input voltage V_{dc} , the load current i_L , and the duty cycle D affect the output voltage. Unfortunately, understanding of converter dynamic behavior is hampered by the nonlinear time-varying nature of the switching and pulse-width modulation (PWM) process. These difficulties can be overcome through the use of waveform averaging and small signal modeling techniques [24]. A well-known converter modeling technique known as state-space averaging is briefly described here. The model equations are derived below. When state switch $S1$ is on and $S2$ is switched off, based on Kirchhoff's laws:

$$\begin{bmatrix} pV_c \\ pI_L \end{bmatrix} = \begin{bmatrix} -1/Cr_c & 0 \\ 0 & -R_b/L \end{bmatrix} \begin{bmatrix} V_c \\ I_L \end{bmatrix} + \begin{bmatrix} 1/Cr_c & 0 \\ 1/Lr_c & 1/L \end{bmatrix} \begin{bmatrix} V_{dc} \\ V_b \end{bmatrix} \quad (5)$$

The state space equation in the matrix form for the converter during off state is given by:

$$\begin{bmatrix} pV_c \\ pI_L \end{bmatrix} = \begin{bmatrix} -1/Cr_c & 0 \\ 0 & -R_b/L \end{bmatrix} \begin{bmatrix} V_c \\ I_L \end{bmatrix} + \begin{bmatrix} 1/Cr_c & 0 \\ 0 & 1/L \end{bmatrix} \begin{bmatrix} V_{dc} \\ V_b \end{bmatrix} \quad (6)$$

where p is the derivative operator; i.e. $p = d/dt$. Combining the two subsystems the averaged state space equation can be written as:

$$\begin{aligned} \dot{X} &= Ax + bV_{dc} + eV_b \\ A &= A_1d + A_2(1-d) \\ B &= b_1d + b_2(1-d) \\ E &= e_1d + e_2(1-d). \end{aligned} \quad (7)$$

The state space equation for the output can be written as:

$$\begin{aligned} Y &= Cx + Du \\ C &= C_1d + C_2(1-d) \\ D &= D_1d + D_2(1-d) \end{aligned} \quad (8)$$

where d is the duty cycle and the matrices are given by:

$$\begin{aligned} A_1 &= \begin{bmatrix} -d/Cr_c & 0 \\ 0 & -dR_b/L \end{bmatrix} \\ A_2 &= \begin{bmatrix} -(1-d)/Cr_c & 0 \\ 0 & -(1-d)R_b/L \end{bmatrix} \\ b_1 &= \begin{bmatrix} b/Cr_c \\ d/Lr_c \end{bmatrix}, & b_2 &= \begin{bmatrix} (1-d)/Cr_c \\ 0 \end{bmatrix} \\ e_1 &= \begin{bmatrix} 0 \\ d/L \end{bmatrix}, & e_2 &= \begin{bmatrix} 0 \\ (1-d)/L \end{bmatrix} \\ C_1 &= \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} & C_2 &= \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \\ D_1 &= [0 \ 0]^T & D_2 &= [0 \ 0]^T \end{aligned}$$

The input to output transfer function can be written as:

$$\frac{\tilde{y}(s)}{\tilde{u}(s)} = C_{av}[SI - A_{av}]^{-1}B_{av} + D_{av} \quad (9)$$

where $\tilde{y}(s)$ is the output and $\tilde{u}(s)$ is the input in Laplace form. Also the averaged matrices are given by:

$$\begin{aligned} C_{av} &= \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} & A_{av} &= \begin{bmatrix} -1/Cr_c & 0 \\ 0 & -R_b/L \end{bmatrix} \\ B_{av} &= \begin{bmatrix} 1/Cr_c & 0 \\ d/Lr_c & 1/L \end{bmatrix} & D_{av} &= \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{aligned}$$

III. THE CONTROL SYSTEM

Fig. 6 shows the schematic diagram for the overall proposed PHEV charging system. The diagram is involving the control strategy for each conversion stage as follows:

A. Rectifier Control

Using PI-voltage controller, the dc-voltage can be regulated by choosing the dc-current reference, $i_{ref}(t)$ such that,

$$i_{ref}(t) = K_p^v \cdot [V_{dc}^r - V_{dc}(t)] + K_i^v \cdot \int [V_{dc}^r - V_{dc}(t)] dt \quad (10)$$

where V_{dc}^r is the desired dc-voltage, K_p^v , K_i^v are the constant gains of the PI-voltage controller. Fig. 7 shows the dc-bus voltage controller operation. Through simulation studies, it was verified that constant frequency PWM controllers tend to increase the current THD due to the duty cycle discontinuities.

Then, the rectifier control system uses the principle of hysteresis control as shown in Fig. 8. The input currents through each phase (I_{abc}) are measured and compared to the respective reference currents (I_{abc}^r). The reference current shapes are obtained from the respective input voltages, and their peak values are given the voltage controller. A second order software phase-locked loop (SPLL) is proposed here to precisely detect the ac-source phase angle and multiply it by the current peak values in order to obtain the reference current signal for the hysteresis current controller. Switching operation occurs when the current limits are reached, as shown in Fig. 9. With this technique, the obtained line currents achieve low THD with a simple control circuitry. The main disadvantage of the hysteresis control is the variable switching frequency. However, switching frequency can be maintained within acceptable range by adjusting the hysteresis band (HB).

The HB method switches the IGBTs (S1-S3) when the error between I_{abc}^r and I_{abc} exceeds a fixed magnitude: the hysteresis band. As can be seen in Fig. 8, this type of control needs a single comparator with hysteresis per phase. In this case the switching frequency is not determined, but its maximum value can be evaluated such that [25]:

$$F_s^{max} = \frac{V_{dc}}{4h \cdot L_1} \quad (11)$$

where F_s^{max} is the maximum switching frequency, L_1 is the line input inductor, and h is the HB magnitude.

B. Battery Control

The primary goal of the battery converter is to regulate the common dc-bus voltage which must be regulated to stay within a stable region regardless of the battery-current variation. To do this, a modified hysteresis-control strategy is applied. The concept of this strategy is to regulate the common dc voltage within a specific band, for example, a hysteresis band. Therefore, the battery charger/discharger is controlled in such a way that the dc-bus voltage should not violate the specified upper and lower limits, V_{dc_up} and V_{dc_low} , as shown in Fig. 9.

A decision criterion for charging/discharging becomes the level of the common dc-bus voltage and the battery buck-boost operates according to the scheme as below:

$$\begin{aligned} \text{If } V_{dc} > V_{dc_up}, & \text{ then charging: } V_{dc}^r = V_{dc_up} \\ \text{If } V_{dc} < V_{dc_low}, & \text{ then charging: } V_{dc}^r = V_{dc_low} \\ \text{If } V_{dc_low} \leq V_{dc} \leq V_{dc_up}, & \text{ then no control (rest).} \end{aligned} \quad (12)$$

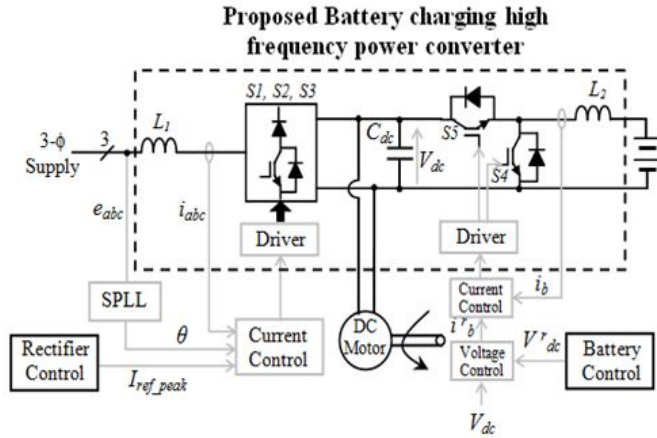
When the common dc voltage V_{dc} becomes larger than the upper limit, charging mode begins with the voltage command V_{dc}^r equal to the upper limit and continues until the dc voltage reaches the limit. If V_{dc} goes below the lower limit, then the voltage target is bound at the lower limit and the converter starts operating in boost mode. Accordingly, the battery-mode control block in Fig. 6 can be built as shown in Fig. 11.

There is another reason for such hysteresis control other than voltage regulation of the dc bus. It is intended to protect the battery storage against excessive charging frequency and current variation. Not by bounding dc-bus voltage at a constant value but by allowing a hysteresis band; the battery can take a rest during the rest interval in Fig. 10. Energy that can be extracted or stored across the hysteresis band in a dc-bus capacitor ΔE_c is described as follows:

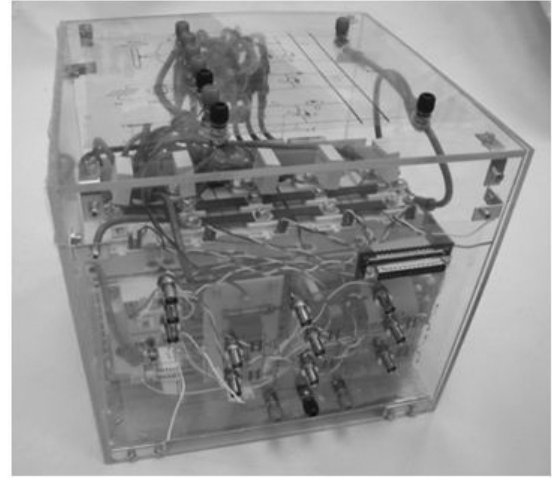
$$\Delta E_c = \frac{1}{2} C_{dc} (V_{dc_up}^2 - V_{dc_low}^2). \quad (13)$$

C. Efficiency Estimation

A main part of total losses is the switching and conduction losses which depend on switching times and switching frequency. Fig. 12 shows the waveforms for switching times. The switching loss can be reduced by decreasing the switching time, but fast switching increases dv/dt and di/dt which affects electromagnetic interference (EMI) noise.



(a)



(b)

Fig. 6. The proposed battery charging converter and its control strategy. (a) Schematic diagram, (b) hardware converter module.

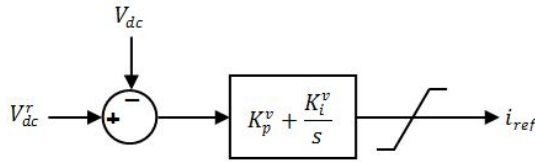


Fig. 7. Voltage controller for rectifier operation.

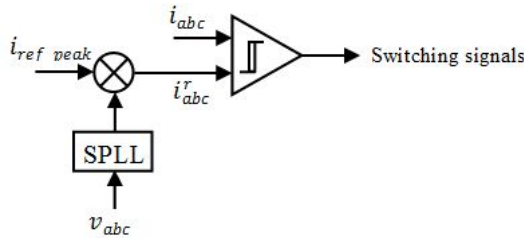


Fig. 8. Hysteresis current controller for rectifier operation.

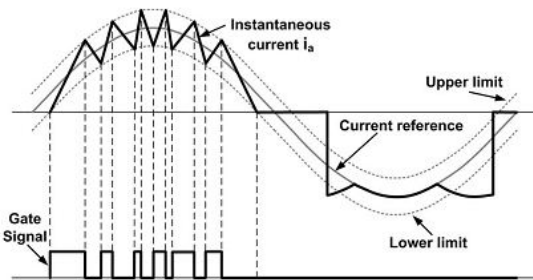


Fig. 9. Switching pattern of the hysteresis control applied to the rectifier stage.

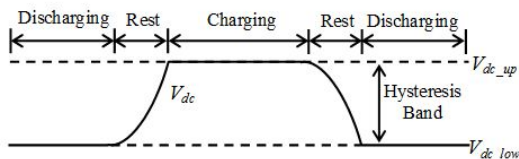


Fig. 10. Modified hysteresis battery control strategy.

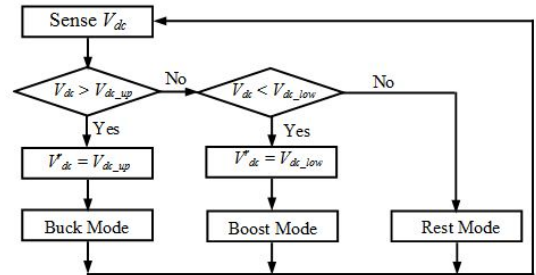


Fig. 11. Battery-mode control block (modified hysteresis).

The average power loss in a switch over one switching cycle is given by the following equation which consists of the conduction and switching losses:

$$\bar{P}_s = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_{sw} v_{sw} dt = \bar{P}_{cond} + \bar{P}_{sw}. \quad (14)$$

Assuming that the on and off switching times are small compared to switching cycle, T_{sw} , and the leakage current is negligible, $I_{off} = 0$. Thus the conduction loss is given by:

$$\bar{P}_{cond} = V_{on} I_{on} D, \quad D = \frac{t_{on}}{T_{sw}} \quad (15)$$

where t_{on} is the time when the switch is in on-state, V_{on} is a voltage drop across the switch, I_{on} is a current through the switch assuming it is constant in magnitude and D is a duty cycle. The switching loss should be calculated based on instantaneous current and voltage waveforms as follows:

$$\bar{P}_{sw} = f_{sw} \left(\int_0^{t_{sw_{on}}} v_{sw} i_{sw} dt + \int_0^{t_{sw_{off}}} v_{sw} i_{sw} dt \right) \quad (16)$$

where $t_{sw_{on}}$ and $t_{sw_{off}}$ are turn-on and turn-off switching times.

Also, the total average power losses can be calculated as follows:

$$P_{av_{loss}} = f_{sw} \left[\frac{1}{2} V_d I_{on} t_{sw_{on}} + \frac{1}{2} V_d I_{on} t_{sw_{off}} + V_{on} I_{on} D \right]. \quad (17)$$

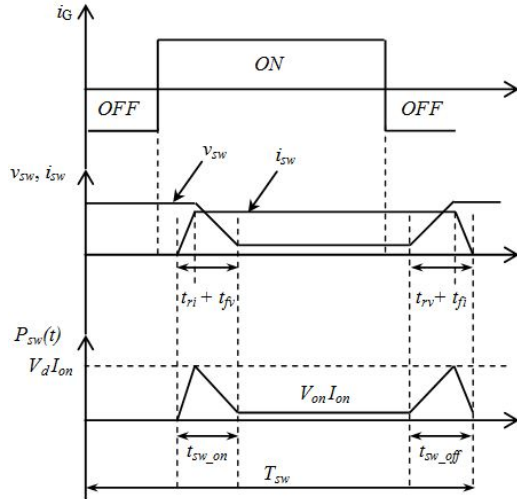


Fig. 12. The voltage, current, and power waveforms for power switches.

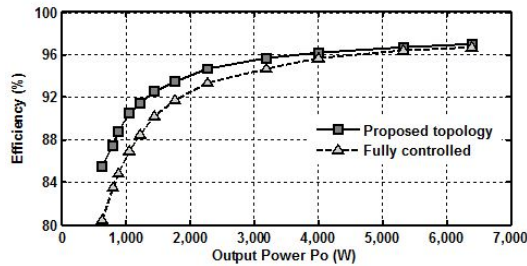


Fig. 13. Estimated efficiencies for the proposed topology (η_1) and the fully-controlled topology (η_2).

In a power electronic system, there are other circuits such as gate drives, controllers, sensors and passive filters which consume power. The total losses are the sum of all losses and the efficiency of a system (η) can be calculated based on input power (P_{in}) and total losses (P_{loss}) as given below:

$$\eta = \frac{\bar{P}_{out}}{\bar{P}_{in}} = \frac{\bar{P}_{in} - \bar{P}_{loss}}{\bar{P}_{in}} = 1 - \frac{\bar{P}_{loss}}{\bar{P}_{in}}. \quad (18)$$

In order to estimate the efficiency of the proposed rectifier, a loss analysis was performed, considering the developed equations, the semiconductors, and parameters given in Table II and the respective datasheets. Fig. 13 compares the estimated efficiency of the proposed rectifier stage (η_1) with the fully-controlled rectifier topology (η_2). In the fully controlled bridge structure, the currents can be modulated in both half cycles which leads to less input current harmonic distortion when compared to the proposed half controlled bridge topology. However, it has more complicated operation and control process; since it has larger switching losses and it requires the use of bootstrap-integrated circuits. Moreover, the occurrence of eventual short-circuits through the leg is possible. It can be seen that the proposed rectifier has improved efficiency over the entire power range, due to the fewer number of semiconductors, which is an interesting advantage in PHEV applications.

IV. EXPERIMENTAL RESULTS

A 60-kW prototype of the proposed battery charging high frequency power converter was developed. Fig. 6 shows

TABLE II
SEMICONDUCTOR DEVICES AND ITS PARAMETERS

Proposed topology		Fully-controlled topology	
Parameter	Specification	Parameter	Specification
S_1-S_3, D_1-D_3	SKM 50GAL125D	S_1-S_6	SKM 50GB125D
V_{switch}	1200V	V_{switch}	1200V
I_{switch}	50A	I_{switch}	50A
Power rating	60 kW	Power rating	60 kW

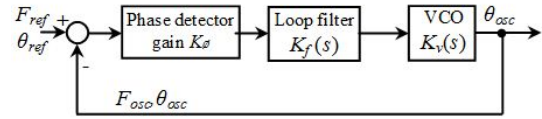


Fig. 14. Basic PLL block diagram.

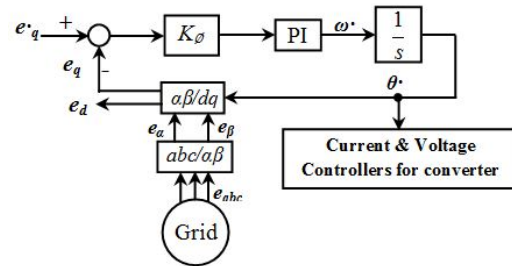


Fig. 15. SPLL applied for ac-grid voltage.

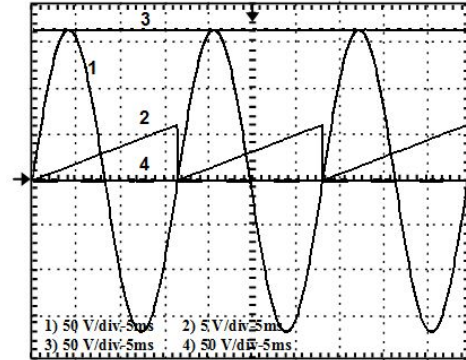


Fig. 16. Grid voltage (1-50 V/div, 5ms), phase angle (2-5V/div, 5ms), and synchronous frame dq voltage waveforms (3, 4-50 V/div, 5ms) for phase “a”.

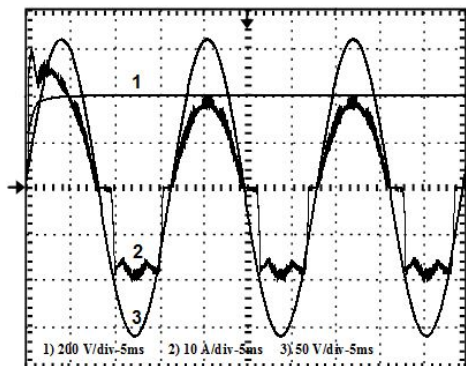


Fig. 17. DC-bus output voltage (1-200 V/div, 5ms), rectifier current (2-10 A/div, 5ms), and grid voltage (3-50 V/div, 5ms) for phase “a”.

TABLE III
RECTIFIER SPECIFICATIONS AND PARAMETERS

Parameter	Specification
Input voltage range	70-208 V _{rms}
Line input inductor (L_1)	0.3 mH
Inductor internal resistance	0.012 Ω
DC-bus capacitor (C_{dc})	1000 μ f
DC-bus voltage (V_{dc})	400 V
Switching frequency (f_{sw})	30-45 kHz

TABLE IV
BATTERY AND DC-DC CONVERTER SPECIFICATIONS & PARAMETERS

DC-DC Converter		Battery Bank	
Parameter	Specification	Parameter	Specification
V_{dc}	400 V	rated voltage	160 V
L_2	0.15 mH	Connection	10-series
Switch	IGBT	rated capacity	100 AH
f_{sw}	50 kHz	Battery type	Lead-acid
Control	Bulk/absorption/float	Total power	12 kW

the prototype schematic diagram and a photograph for its hardware implementation. The high frequency power converter module has been designed and implemented in the energy systems research laboratory (ESRL). It is composed of a semi-controlled rectifier and a bidirectional dc-dc converter. The individual converters are controlled by their own TMS320F28335-based control platforms. The specifications and parameters used in the prototype are shown in Tables III and IV.

A. Second Order SPLL for Phase Angle Detection

A good detection of the phase angle of the ac power is highly recommended in PHEV systems utilizing converter-inverter unites. A fully software PLL for the phase angle detection of the three phase voltage is proposed here using the dq synchronous reference frame. Fig. 14 shows a basic block diagram of the applied PLL. The output of the voltage controlled oscillator (VCO), F_{ref} , is fed-back to the phase frequency detector input, and comparison continue until both frequency and phase are made the same and the phase and frequency of the VCO are in locked state with reference signal i.e. $F_{osc} = F_{ref}$, $\theta_{osc} = \theta_{ref}$. The closed loop transfer function of the PLL system of Fig. 14 can be expressed as:

$$W(s) = \frac{\theta_{osc}(s)}{\theta_{ref}(s)} = \frac{K_\phi K_f(s) K_v(s)}{1 + K_\phi K_f(s) K_v(s)}. \quad (19)$$

The VCO transfer gain $K_v(s)$ is a function of time, since phase is the time integral of frequency, it may be written as:

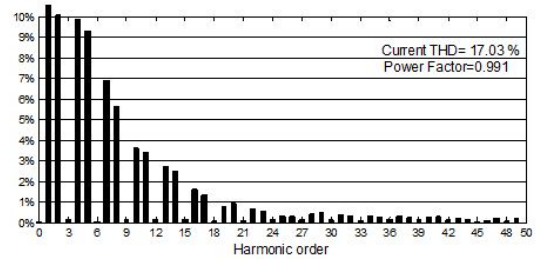
$$K_v(s) = \frac{K_v}{s}. \quad (20)$$

The phase frequency detector gain, K_ϕ , is assumed to be independent of frequency. With unity VCO gain, $K_v = 1$, (19) can be rewritten as:

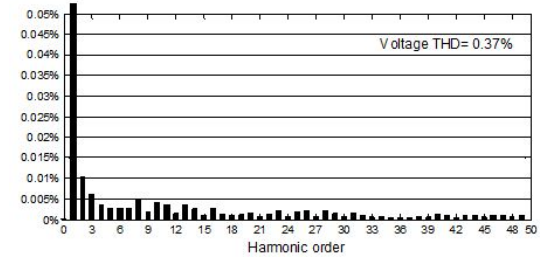
$$W(s) = \frac{K_\phi K_f(s)}{S + K_\phi K_f(s)}. \quad (21)$$

There are several methods to design the loop filter. The 2nd order loop filter is commonly used as a good trade-off of the filter performance and system stability [26]. The 2nd order PI-loop filter can be expressed in the form:

$$K_f(s) = K_p + K_i/s \quad (22)$$



(a)



(b)

Fig. 18. Harmonic spectrum of (a) The generator voltage, (b) the input current.

where K_p and K_i denote the gain parameters of the PI loop filter, therefore:

$$W(s) = \frac{K_\phi K_p s + K_\phi K_i}{s^2 + K_\phi K_p s + K_\phi K_i}. \quad (23)$$

The general form of the closed loop transfer function of the second order system is given by:

$$W(s)_{General} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}. \quad (24)$$

A second-order loop filter design was proposed here as a good trade-off of the filter performance and system stability. The main objective of this design is to precisely detecting the phase angle during presence of the 5th and 7th harmonics. Comparing (23) with (24):

$$K_i = \frac{\omega_n^2}{K_\phi} \quad \text{and} \quad K_p = \frac{2\xi\omega_n}{K_\phi}. \quad (25)$$

The PI-filter gain parameters were designed and analyzed to meet the time domain specification: minimum overshoot, minimum settling time and minimum steady-state error such that the natural frequency (ω_n) = 314 rad/sec and the damping ratio (ξ) = 0.707.

Accordingly, the gain parameters have been calculated from (25) such that $K_p = 2.62$ and $K_i = 580.98$. The configuration of the PLL system using the dq components in the synchronous reference frame of the three phase input voltage is shown in Fig. 15. Figure 16 shows the response of the SPLL system at 60Hz, 110V. The synchronous reference frame dq voltage appears as dc-values.

B. Rectifier Performance

Fig. 17 shows the dc-bus voltage, the current through phase "a," and the respective grid phase voltage. The dc-bus voltage has no overshoot and low voltage ripple of 2.3%. Fig. 18 shows the harmonic spectrum of the grid voltage

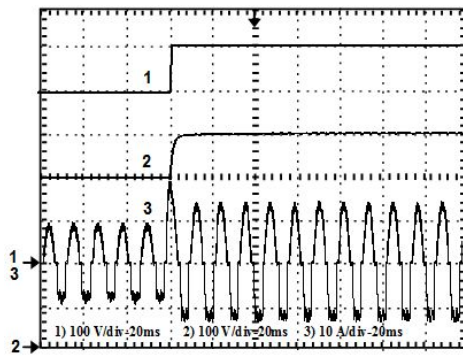


Fig. 19. The reference and actual dc-bus voltage (1, 2-100 V/div, 20ms), and rectifier current (3-10 A/div, 20ms) under step change of dc-bus voltage level.

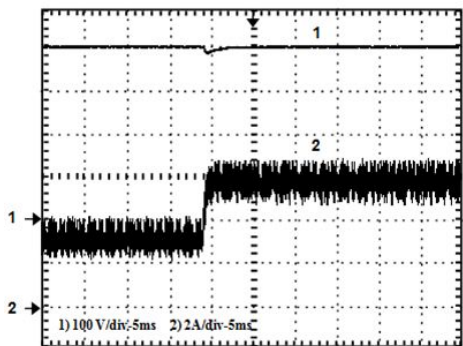


Fig. 20. Loading change effect. (a) DC-bus output voltage (1-100 V/div, 5ms), (b) load current (2-2 A/div, 5ms).

(THD=0.37%) and rectifier current (THD=17.03%), where the second-, fourth-, and fifth-order components are the most relevant. UPF operation was investigated (PF=0.991); since the rectifier current and the phase voltage are in phase. In conventional uncontrolled diode rectifiers, typical power factor and THD are about 0.94 and 35%, respectively [27]. This improvement in the power factor represents more economic utilization of grid power.

C. DC Reference Change Test

Fig. 19 shows the reference voltage, V_{dc}^r and the actual voltage, V_{dc} under dc-bus voltage reference change. The main objective of this test is to investigate the control system performance under dc-bus voltage level change to large values for medium-voltage distribution applications. The dc-bus is connected to a 3-hp dc-motor operated at full load. A reference step change is applied and set to be increased from 400 V to 500 V. The corresponding rectifier current at rated power (2.5 kW) is also shown in Fig. 19. According to gain parameters design, it is noticed that the control operation has over damped transient response and there is no overshoot. Therefore, the overall dynamic performance has been greatly improved.

D. Loading Effect

The system performance is also investigated under load variation test. Fig. 20 shows the test results of the power converter under step change in the load current (from half to full load). We can notice that the load current is increased from 3 to 6A. On the other hand, dc-bus voltage still tracking its reference value with a small transient dipping of 4 V (1%).

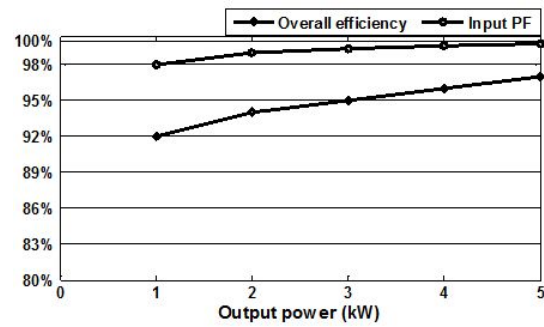


Fig. 21. Efficiency and input PF versus output power.

Fig. 21 shows the measured efficiencies. This demonstrates the expected improvement when compared with similar works.

E. Application Considerations

Practically, during initial voltage controller adjustment with the dc-bus capacitor uncharged, the initial dc-level will be very high, if it is above the capacitor voltage rating, it can destroy it. Avoiding that can be done by initially charging the dc-bus capacitor to 60% of the reference dc-voltage. The free-wheeling diodes of the IGBT module is working as a diode bridge rectifier during an initial charging. Once the capacitor is charged, the converter switching control signals should be connected, allowing the total power to flow through the IGBT switches.

V. CONCLUSIONS

In this paper, a new battery charging high frequency power converter module was developed for PHEV systems. The proposed three-phase semi-controlled rectification topology reduces the switching and conduction losses when compared to fully-controlled topology. A UPF operation (0.981) was achieved for better economic utilization of the grid absorbed power. The high efficiency operation was verified due to reduced number of switches (average 95%). A second order SPLL was accurately designed for accurately detecting the phase angle during presence of the 5th and 7th harmonics. A fast control dynamic response was achieved (0.1 second) under different possible conditions; dc-reference step change and load variation. All the obtained results confirm the effectiveness of the proposed system for PHEV application.

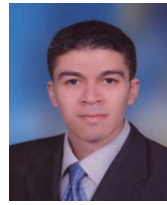
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