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Analysis, Design and Implementation of a New Chokeless Interleaved ZVS Forward-Flyback Converter

Meghdad Taheri†, Jafar Milimonfared*, Alireza Namadmalan*,
Hasan Bayat*, and Mohammad Kazem Bakhshizadeh*

†* Dept. of Electrical Eng., Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran

Abstract

This paper presents an interleaved active-clamping zero-voltage-switching (ZVS) forward-flyback converter without an output choke. The presented topology has two active-clamping circuits with two separated transformers. Because of the interleaved operation of the converter, the output current ripple will be reduced. The proposed converter can approximately share the total load current between the two secondaries. Therefore, the transformer copper loss and the rectifier diodes conduction loss can be decreased. The output capacitor is made of two series capacitors which reduces the peak reverse voltage of the rectifier diodes. The circuit has no output inductor and few semiconductor elements, such that the adopted circuit has a simpler structure, a lower cost and is suitable for high power density applications. A detailed analysis and the design of this new converter are described. A prototype converter has been implemented and experimental results have been recorded with an ac input voltage of 85-135Vrms, an output voltage of 12V and an output current of 16A.

Key Words: Active clamping circuit, Forward-flyback converter, Interleaved converter, Zero-voltage switching

I. INTRODUCTION

Forward and flyback converters have been widely used in the power supply industry because of their simplicity, good efficiency and low cost. The transformer in a flyback converter is used to isolate the electric signal and to store the magnetic energy. The transformer in a forward converter is adopted to achieve circuit isolation and energy transformation. The hard switching operation of forward and flyback converters imposes high voltage and current spikes on their switches, due to the presence of transformer leakage inductance. Furthermore, the switching losses result in a low conversion efficiency. A passive-clamping circuit can be added for dissipation of the stored energy in the leakage inductance [1], which reduces the voltage stress on the switch. However, the conversion efficiency of the converter will not be greatly improved. In recent years, active-clamping techniques have been proposed for both types of converters [2]–[14] to absorb the energy stored in the leakage inductance and to suppress the voltage spikes on the switch. Furthermore, in the forward converter, it completes the energy reset process. In comparison with conventional forward and flyback converters, the active-clamping converters have a higher efficiency because of the zero-voltage-switching (ZVS) operation of the main switch, which is fulfilled with the help of the auxiliary switch. Unfortunately, the DC offset current of an active clamp flyback converter, deteriorates the transformer utilization and increases the transformer size, which results in the low power density of the converter.

The power losses and current stress on the switch devices can be evenly distributed by paralleling two or more converters. Using interleaved structures, the output current ripple can be significantly reduced, or equivalently, the output inductance and capacitance can be halved under the same output rating. However, in interleaved active-clamping converters a total of four switches, four diodes and more magnetic components including transformers and inductors are required, which increases the circuit size, complexity and cost [15]–[21].

This paper presents a new interleaved active-clamping zero-voltage-switching forward-flyback converter without an output choke. Two converter modules are connected in parallel on the input and output sides to reduce the current stresses on the output diodes and windings of the transformers. The main switch of any converter acts as an auxiliary switch for the other one. As a result, only two switches are required and there is no need for additional switches to achieve ZVS operation. The output capacitor is made of two series capacitors which reduces the reverse voltage of the rectifier diodes. The proposed circuit has no large output inductor. Therefore, the adopted circuit has a simpler structure, a lower cost and is capable of a high power

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† Corresponding Author: meghdadtaheri@aut.ac.ir
Tel: +98-21-64543350, Amirkabir University of Technology
* Dept. of Electrical Eng., Amirkabir University of Technology (Tehran Polytechnic), Iran

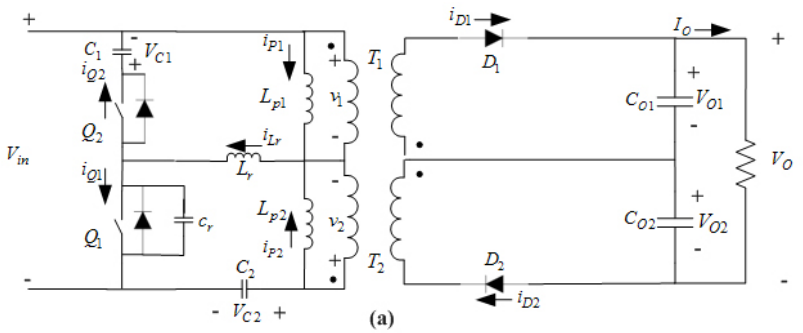

Fig. 1. Schematic of the proposed choke-less interleaved ZVS forward-flyback converter.

density. Based on the above mentioned reasons, the proposed converter is suitable for high-voltage and high-current output applications.

The circuit configuration, the principle of operation and the design considerations of the proposed converter are discussed in detail. Finally, experimental results based on a 180 W (12V/15A) prototype circuit are presented to verify the circuit performance.

II. Circuit Configuration

Fig. 1 shows a schematic of the proposed topology which is composed of an active-clamping forward converter parallel with an active-clamping flyback converter. The flyback converter includes V_{in}, T_1, Q_1, Q_2, C_1, D_1, C_{o1} and C_{o2}. Similarly, the forward converter consists of V_{C2}, T_2, Q_1, Q_2, C_1, D_2, C_{o1} and C_{o2}. L_r is the sum of the leakage inductances of T_1 and T_2. L_{P1} and L_{P2} are the magnetizing inductances of T_1 and T_2. V_{in} and V_o are the input voltage source and the output voltage, respectively. C_{o1} and C_{o2} are the output capacitors. C_r is equivalent to the parallel combination of the output capacitances of Q_1 and Q_2 and the parasitic capacitances of the transformer primary windings. The auxiliary switch Q_2 and the clamp capacitor C_1 represent the active clamp circuit to absorb the surge energy due to the leakage inductance L_r.

III. Principles of Operation

Based on the on/off states of Q_1, Q_2, D_1 and D_2, the proposed converter has eight operating modes during one switching cycle. Fig. 2 depicts the key waveforms of the proposed converter. In the following analysis, the governing current and the voltage equations are derived for each state. The conduction paths for each operating state are shown in Fig. 3

State 1 (t_0-t_1): Q_1 is turned on. As shown in Fig. 3(a) for the flyback part, v_1 is n_{vO2} and D_1 is reverse biased. The input energy is stored in the primary magnetizing inductance L_{P1} and i_{P1} increases linearly. For the forward part, v_2 is n_{vO2}. Thus, i_{P2} increases linearly. The diode D_2 is on and the input power is delivered to the secondary. In this state, the primary currents i_{P1}, i_{P2} and resonant inductor current i_{Lr} can be expressed as:

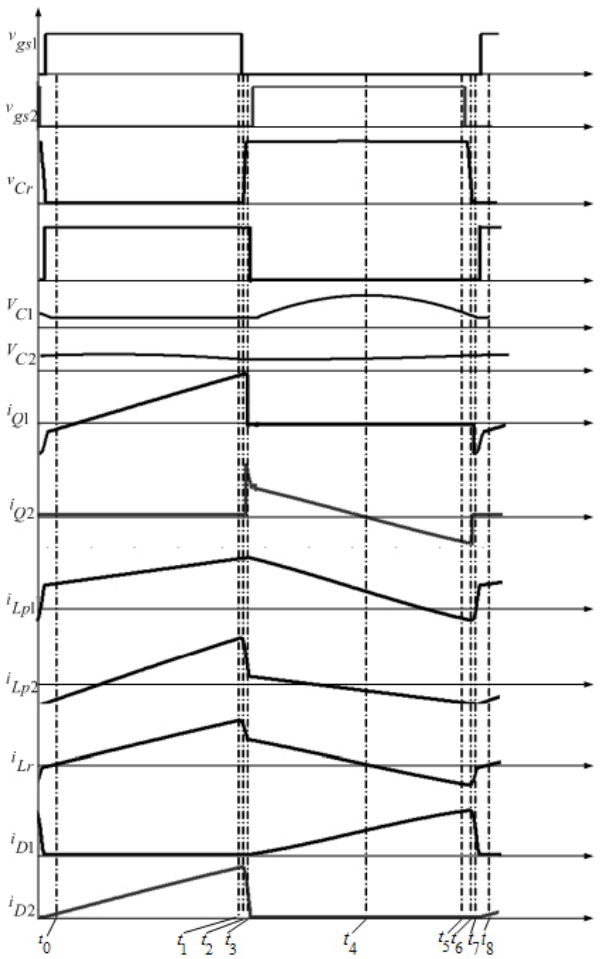

Fig. 2. Key waveforms of the proposed converter.

$$i_{p1} = \frac{nV_{O2}}{L_P}t + i_{p_1}(t_0) \tag{1}$$

$$i_{p2} = \frac{nV_{O2}}{L_P}t + \frac{i_{D2}}{n} + i_{p2}(t_0) \tag{2}$$

$$i_{Lr} = \frac{V_{in} - nV_{O2}}{L_r}t + i_{Lr}(t_0). \tag{3}$$

State 2 (t_1–t_2): This state starts at t_1 when Q_1 is turned off. As shown in Fig. 3(b), for the flyback part D_1 is still off. The resonant inductor current i_{Lr} charges the resonant capacitor C_r from zero to $V_{in} + V_{C1}$. For the forward part i_{D2} is linearly

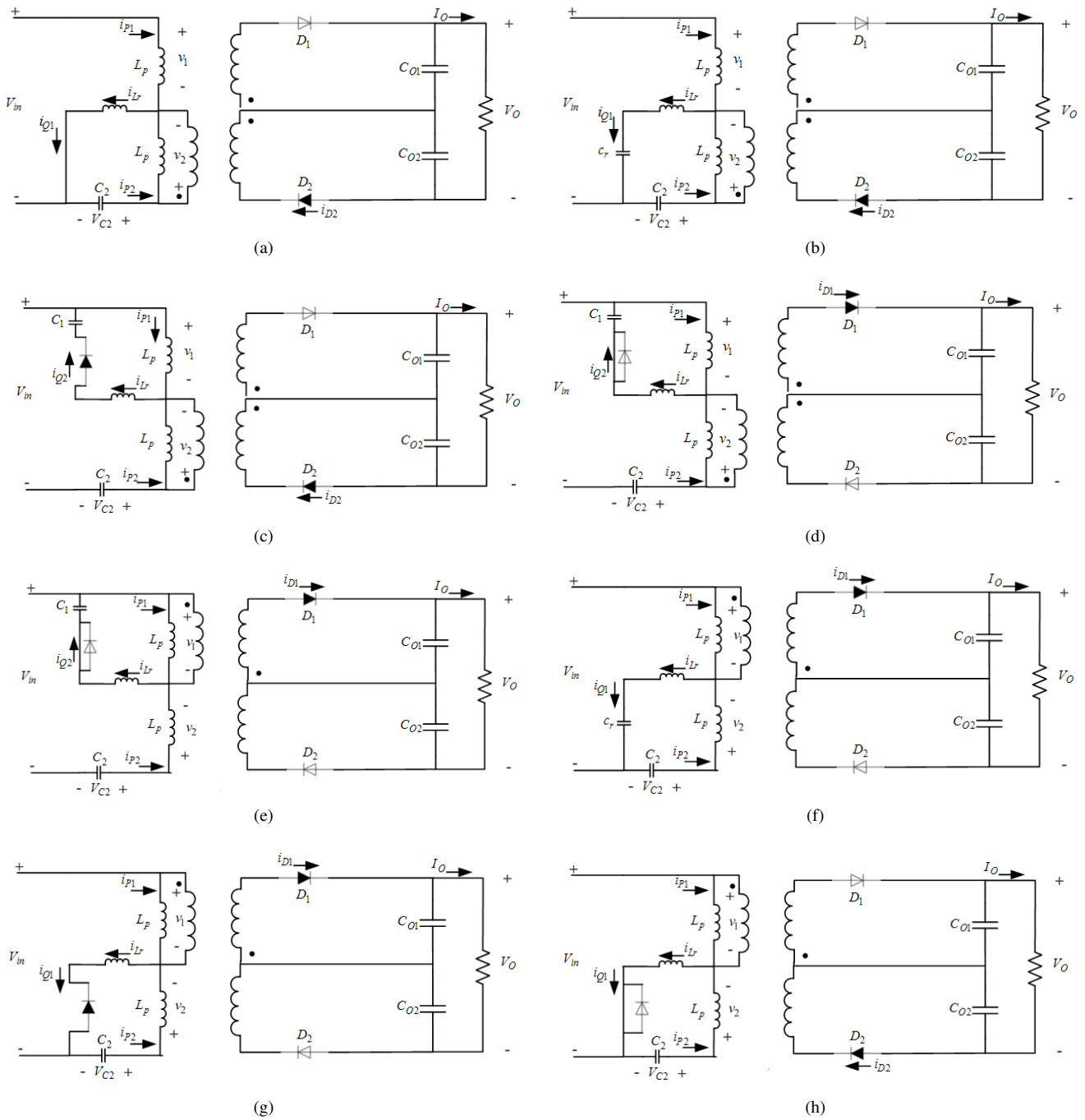

Fig. 3. Conduction paths of (a) state 1, (b) state 2, (c) state 3, (d) state 4, (e) state 5, (f) state 6, (g) state 7, and (h) state 8 for the proposed converter during one switching period.

decreasing. In this state, the resonant inductor current i_{Lr} and the resonant capacitor voltage v_{Cr} can be written as:

$$i_{Lr} = w_0 C_r (V_{in} - nV_{o2}) \sin w_0 (t - t_1) + i_{Lr}(t_1) \cos w_0 (t - t_1) \tag{4}$$

$$v_{Cr} = \frac{i_{Lr}(t_1)}{w_0 C_r} \sin w_0 (t - t_1) + (V_{in} - nV_{o2}) [1 - \cos w_0 (t - t_1)] \tag{5}$$

Where

$$w_0 = \sqrt{\frac{1}{L_r C_r}}. \tag{6}$$

The time interval of this state can be expressed as:

$$(t_2 - t_1) = \frac{C_r}{i_{Lr}(t_1)} (V_{in} + V_{C1}). \tag{7}$$

State 3 (t_2–t_3): After t_2, the resonant capacitor voltage v_{Cr} is clamped at $V_{in} + V_{C1}$. For the flyback part i_{P1} is increasing and D_1 is still reverse biased. For the forward part i_{P2} and i_{D2} is linearly decreasing. The resonant inductor current iLr

decreases linearly while flowing through the body diode of Q_2, as shown in Fig. 3(c), to charge the clamping capacitor C_1. Q_2 can now be turned on. Since C_1 is assumed to be much larger than C_r, V_{C1} remains almost constant. In this state, i_{Lr} can be written as:

$$i_{Lr} = i_{Lr}(t_2)\cos w_1(t-t_2) - nV_{O1}\sqrt{\frac{2C_1}{L_P+2L_r}}\sin w_1(t-t_2) \tag{8}$$

Where

$$w_1 = \sqrt{\frac{2}{(L_P+2L_r)C_1}}. \tag{9}$$

This interval ends when v_1 and v_2 equal $(-nv_{O2})$ at t_3.

State 4 (t_3–t_4): As shown in Fig. 3(d), at t_3, i_{D2} decays to zero. i_{D1} is linearly increasing and the energy stored in L_{P1} is transferred to the output load. The resonant inductor L_r and the clamping capacitor C_1 begin to resonate. In order to ensure the ZVS operation of Q_2, Q_2 should be turned on before it becomes negative. In this state, the primary currents i_{P1} and i_{P2} and resonant inductor current i_{Lr} can be expressed as:

$$i_{p1=} - \frac{nV_{o1}}{L_P}(t-t_3) - \frac{i_{D1}}{n} + i_{p1}(t_3) \tag{10}$$

$$i_{p2=} - \frac{nV_{o1}}{L_P}(t-t_3) + i_{p2}(t_3) \tag{11}$$

$$i_{Lr} = w_2C_1(nV_{O1}-V_{C1})\sin w_0(t-t_3) + i_{Lr}(t_3)\cos w_0(t-t_3) \tag{12}$$

$$w_2 = \sqrt{\frac{1}{L_rC_1}}. \tag{13}$$

State 4 is accomplished when i_{Lr} is zero.

State 5 (t_4–t_5): The circuit operations in this interval are the same as those in State 4, except that the direction of i_{Lr} is reversed. As a result, Q_2 conducts instead of its body diode. This state is accomplished when Q_2 is turned off.

State 6 (t_5–t_6): The auxiliary switch Q_2 is turned off at t_5. The resonant capacitor C_r is discharged via the current i_{Lr} at the same time. For the flyback part D_1 is still on and v_1 is $(-nv_{O1})$. For the forward part v_2 is $(-nv_{O1})$ and D_2 is reverse biased. The resonant current i_{Lr} and the resonant capacitor voltage V_{Cr} can be derived as:

$$\begin{aligned} i_{Lr} = {} & w_0C_r(V_{in}+nV_{o1}-v_{cr}(t_5))\sin w_0(t-t_5) \\ & + i_{Lr}(t_5)\cos w_0(t-t_5) \end{aligned} \tag{14}$$

$$\begin{aligned} v_{Cr} = {} & \frac{i_{Lr}(t_5)}{w_0C_r}\sin w_0(t-t_5) - \\ & (V_{in}+nV_{o1}-v_{cr}(t_5))\cos w_0(t-t_5) + V_{in}.+nV_{o1} \end{aligned} \tag{15}$$

To ensure the ZVS operation for Q_1, the initial energy stored in L_r must be greater than the energy stored in C_r. That is:

$$\frac{1}{2}L_ri_{Lr}^2(t_5) \geq \frac{1}{2}C_r(V_{in}+V_{C1})^2. \tag{16}$$

This state ends at t_6 when the voltage V_{Cr} decreases to zero.

State 7 (t_6–t_7): At t_6, V_{Cr} decreases to zero. As shown in Fig. 3(h), the body diode of Q_1 is conducting and Q_1 can be turned on to achieve the ZVS operation. For the flyback part v1 is $(-nv_{O1})$, but the secondary current through D_1 is linearly decreasing. For the forward part, v_2 is $(-nv_{O1})$ and D_2 is still reverse biased. In this state, the primary currents i_{P1} and i_{P2} and the resonant inductor current i_{Lr} can be expressed as:

$$i_{p1} = -\frac{nV_{o1}}{L_P}(t-t_6) - \frac{i_{D1}}{n} + i_{p_1}(t_6) \tag{17}$$

$$i_{p2} = -\frac{nV_{o1}}{L_P}(t-t_6) + i_{p2}(t_6) \tag{18}$$

$$i_{Lr} = \frac{V_{in}+nV_{o1}}{L_r}(t-t_6) + i_{Lr}(t_6). \tag{19}$$

This state ends at t_7 when Q_1 is on.

State 8 (t_7–t_8): This stage begins at t_7 when Q_1 is turned on and ends at t_8 when i_{D1} equals zero. The equivalent circuit of this stage is the same as the equivalent circuit in stage 7.

IV. Design Consideration

Based on the voltage-second balance across the secondary side of T_1 and T_2, the output capacitor voltages are given as

$$V_{O1} = DV_O \tag{20}$$

$$V_{O2} = (1-D)V_O. \tag{21}$$

Based on the voltage–second balance on the primary side of T_1 and T_2 the average clamp voltages V_{c1} and V_{c2} can be obtained as:

$$V_{C1} = \frac{D}{1-D}V_{in} \tag{22}$$

$$V_{C2} = V_{in}. \tag{23}$$

Based on the voltage–second balance of the leakage inductances of T_1 and T_2, the voltage conversion ratio M is expressed as

$$M = \frac{V_O}{V_{in}} = \frac{1}{n(1-D)}. \tag{24}$$

The turns ratio of the transformer primary winding to the secondary winding is equal to

$$n = \frac{N_P}{N_S} = \frac{V_{in,\min}}{(V_o+V_f)(1-D_{\max})} \tag{25}$$

where is V_f the voltage drop of the rectifier diode. The maximum voltage stresses of Q_1 and Q_2 are approximated as

$$V_{DS1,\max} = V_{DS2,\max} = V_{in}+V_{C1} = \frac{V_{in}}{1-D}. \tag{26}$$

The peak currents of Q_1 and Q_2 are expressed as

$$I_{Q1,\max} = I_{Q2,\max} = 2\left[\frac{I_{o,\max}}{n} + \frac{V_{in,\min}}{L_P}D_{\max}T_S\right]. \tag{27}$$

To ensure the ZVS operation for Q_1, the initial energy stored in L_r must be greater than the energy stored in C_r. That is:

$$L_r \geq \frac{C_r(V_{in}+nV_{C1})^2}{i_{Lr}^2(t_5)} \simeq \frac{C_r(V_{in}+V_{C1})^2}{{i_{Q1,\max}}^2}. \tag{28}$$

The voltage stresses of the secondary rectifier diodes are

$$V_{D1,\max} = V_{D2,\max} = V_O. \tag{29}$$

This equation shows that the voltage stresses of the rectifier diodes reduces significantly in comparison to [20].

The peak secondary diode currents are expressed as

$$I_{D1,\max} = I_{D2,\max} = 2I_{o,\max} \tag{30}$$

The root mean square currents of the rectifier diodes are

$$I_{D1,rms} = \frac{2}{\sqrt{3}} I_{o,\max} \sqrt{1-D} \tag{31}$$

$$I_{D2,rms} = \frac{2}{\sqrt{3}} I_{o,\max} \sqrt{D}. \tag{32}$$

If the current ripples of the magnetizing inductors are given, the magnetizing inductance can be obtained as

$$L_{P1} = \frac{nV_{O2}DT_s}{\Delta i_{LP1}} = \frac{nV_O(1-D)DT_s}{\Delta i_{LP1}} \tag{33}$$

$$L_{P2} = \frac{nV_{O1}(1-D)T_s}{\Delta i_{LP2}} = \frac{nV_O(1-D)DT_s}{\Delta i_{LP2}}. \tag{34}$$

V. Design Consideration

To verify the principle of the proposed converter shown in Fig. 1, a 200w prototype converter is constructed in the laboratory. The experimental results are obtained with the following parameters:

Input dc voltage range	V_{in} =120-190V
Output voltage	V_O=12
Rated output current	I_O=20A
Switching frequency	f_s=100 kHz
Maximum duty cycle	D_{max}=.45
Turns ratio	n= 76:4
Clamping capacitances	C_1=C_2=2.2uF
Output capacitance	C_{O1}=C_{O2}=330uF
Conversion efficiency	$\eta \geq .8$

Fig. 4 shows the experimental results of the gate signal, the leakage inductance current i_{Lr} and the switch currents i_{Q1} and i_{Q2}. Before Q_1 is turned on, i_{Lr} is equal to the current i_{Q2}. The negative i_{Lr} discharges the output capacitor C_r across Q_1 in order to achieve ZVS operation in the dead time. After Q_1 is turned on, the primary current i_{Lr} is equal to the current i_{Q1}.

Fig. 5 illustrates the measured results of the clamping capacitor voltages V_{C1} and V_{C2}. It is shown that when Q_2 is turned on the clamping capacitor is resonating with the resonant inductor.

Fig. 6 shows the ZVS operation for Q_1, in full load and half load conditions. Fig. 5(a) and (c) show the measured results of the gate-to source and the drain-to-source voltages for Q_1. It is seen that before the gate voltage of Q_1 is turned on, the drain to- source voltage vDS1 is zero. Therefore, Q_1 is turned on under ZVS. Fig. 5(b) and (d) give the measured waveforms of the gate voltage and the drain current for Q_1. It can be observed that the drain current is negative before the gate voltage v_{GS1} is positive. The intrinsic body diode of Q_1 is conducting the negative drain current i_{Q1}, and the switch

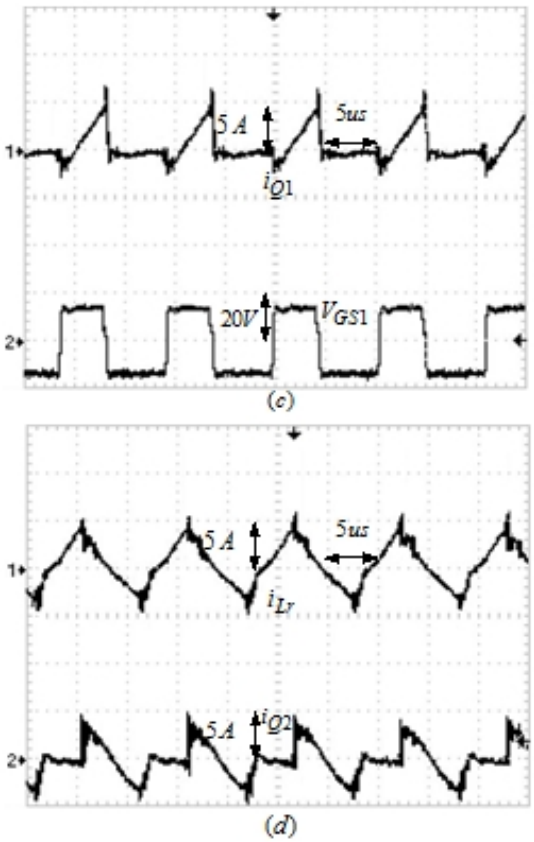

Fig. 4. Waveforms of iQ1, iQ2, VGS1, ilr.

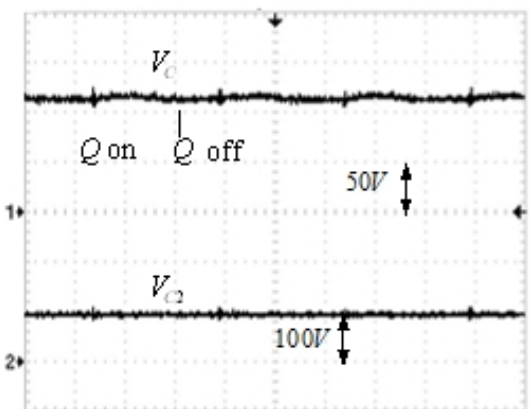

Fig. 5. Waveforms of clamping capacitor VC1and VC2.

Q_1 is turned on to ensure ZVS operation. In the same manner, the measured gate voltage, the drain voltage and the switch current of Q2 are shown in Fig. 7.

Fig. 8 shows the experimental results for the secondary-side currents i_{D1} and i_{D2} for different loads. When Q_1 is turned on the secondary-side current $i_{D2} = i_{CO2} + I_O$ and $i_{D1} = 0$. On the other hand, $i_{D1} = i_{CO1} + I_O$ and $i_{D1} = 0$ when Q_2 is on and Q_1 is off.

Fig. 9 shows the measured efficiencies of the proposed interleaved active-clamping ZVS forward-flyback converter without an output inductor at different load levels. The average efficiency is above 87.8%. Under the rated full load, the conversion efficiency is about 86%.

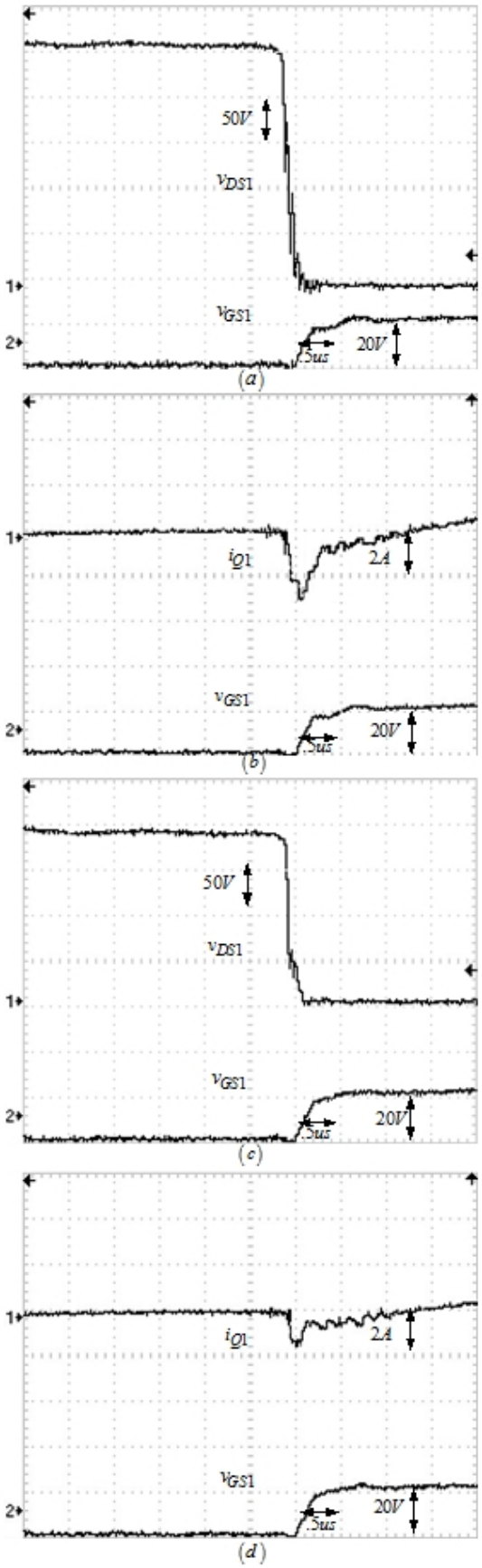

Fig. 6. ZVS operation for Q1, a, b at full load and c, d at half load.

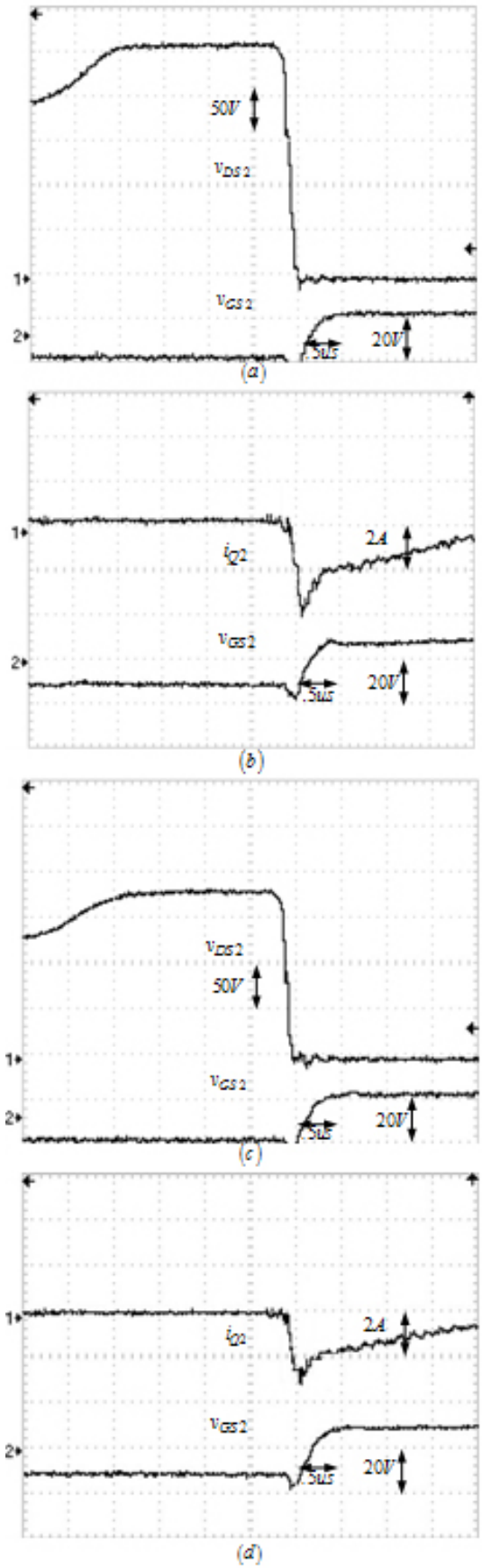

Fig. 7. ZVS operation for Q2, a, b at full load and c, d at half load.

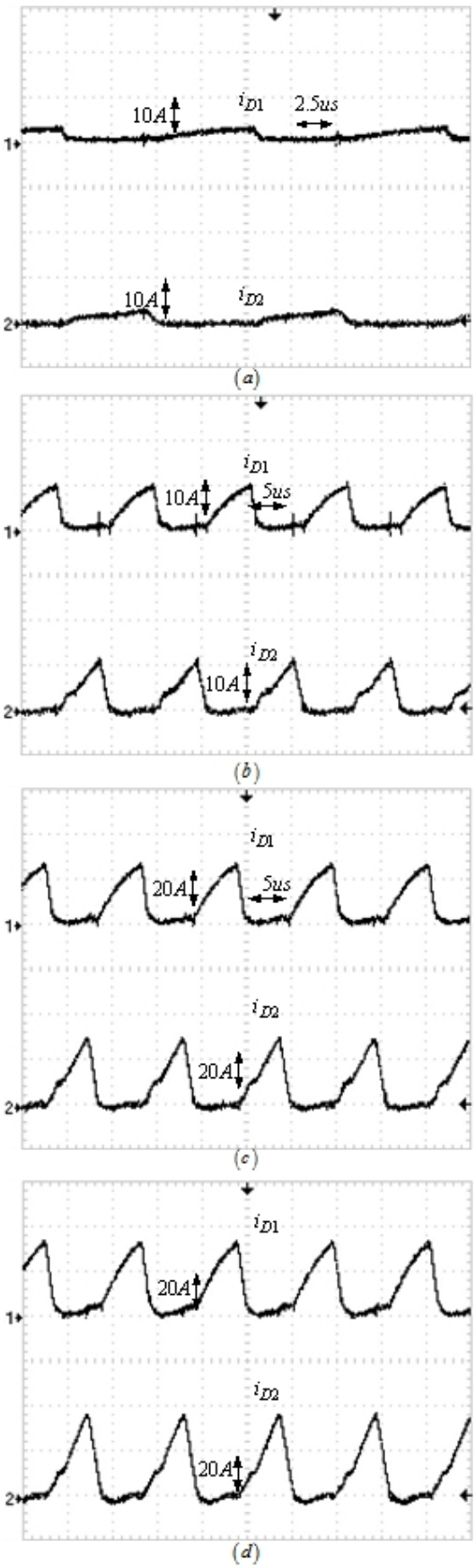

Fig. 8. Waveforms of iD1 and iD2 at a load current of (a) 2A, (b) 5A, (c) 10A, (d) 16A.

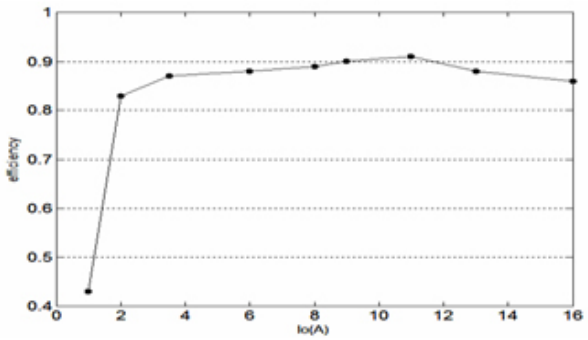

Fig. 9. Efficiencies of the proposed converter at different output current.

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Meghdad Taheri was born in Choram, Iran, in 1984. He received his B.S. in Electrical Engineering from Shiraz University, Shiraz, Iran, in 2006, and his M.S. from the Amirkabir University of Technology (Tehran Polytechnic University), Tehran, Iran in 2010. He is currently working toward his Ph.D. at the Amirkabir University of Technology. His research interests include switching power supplies, power electronics, electrical machines and drives.

Jafar Milimonfared received his B.S. in Electrical Engineering from the Amirkabir University of Technology, and both his M.S. and Ph.D. from Paris VI University, Paris, France in 1981 and 1984, respectively. He joined the Amirkabir University of Technology as an Assistant Professor in 1984, where he is now a Professor of Electrical Engineering. From 1990 to 1993 and from 1997 to 2005, he was the Deputy of Ministry of Science, Research and Technology in Iran. He is now the Head of the Iran Mechatronics Society and the Head of Iran's Society for Morality in Science and Technology. His research interests include the design and analysis of electrical machines, power electronic and variable speed drives.

Alireza Namadmalan was born in Ahvaz, Iran, in 1987. He received his B.S. and M.S. in Electrical Engineering from the Isfahan University of Technology (IUT), in 2009, and the Amirkabir University of Technology, Tehran, Iran, in 2011, respectively, where he is currently pursuing his Ph.D. His research interests include induction heating, resonant converters, switching power supplies, electrical machines and drives, magnetic and high frequency transformers.

Hasan Bayat was born in Zanjan, Iran, in 1985. He received his B.S. and M.S. in Electrical Engineering from Guilan University, Rasht, Iran, in 2008 and the Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran, in 2011, respectively. His research interests include power electronics, multilevel inverters and DC-DC power converters.

Mohammad Kazem Bakhshizadeh was born in Tehran, Iran, on April 30, 1986. He received his B.S. and M.S. in Electrical Engineering from the Amirkabir University of Technology, Tehran, Iran, in 2008 and 2011, respectively. His research interests include multilevel inverters, power electronics and power quality.