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Sliding Mode Control for Current Distribution Control in Paralleled Positive Output Elementary Super Lift Luo Converters

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Abstract

This paper presents a Current Distribution Control design for Paralleled Positive Output Elementary Super Lift Luo Converters (PPOESLLCs) operated in Continuous Conduction Mode using a Sliding Mode Controller (SMC). Manipulating the higher current requirement of the load through the paralleling of POESLLCs, results in a current inequality. This is mainly due to dissimilarities in the power semiconductor switches and circuit components used in POESLLCs, which may lead to converter failures. In order to balance the proper load current sharing and the load voltage regulation of PPOESLLCs, a SMC is developed. The SMC is designed for the inherently variable-structured of POESLLCs by using the state-space average based model. The static and dynamic performance of the developed controller with PPOESLLCs is validated for its robustness to perform over a wide range of operating conditions through both a laboratory prototype and MatLab/Simulink models, which are compared with a Proportional-Integral (PI) controller. Theoretical analysis, simulation and experimental results are presented to demonstrate the feasibility of the developed SMC along with the complete design procedure.

Key Words: DC-DC power conversion, Paralleled positive output elementary super lift luo converter, PI controller and sliding mode control, State-space average model

I. INTRODUCTION

The Positive Output Elementary Super Lift Luo Converter (POESLLC) is a new series of DC-DC converters possessing a high-voltage transfer gain, high power density, high efficiency and reduced output voltage/inductor current ripples [1]. In recent years, DC-DC converters with a steep voltage ratio have become a requirement in many applications. In particular in industrial, medical, telecom, distributed power supply, aerospace and military applications, many interesting solutions of DC-DC converters have been adopted [2], [3]. The super-lift technique considerably increases the voltage transfer gain stage by stage in a geometric progression at the cost of circuit complexity, while the POESLLC does the same thing with a simple structure. Intensive research in the area of DC-DC converters has resulted in novel circuit topologies [4], [5]. These converters in general have complex non-linear models with parameters variation. The state space averaging approach has been one of the most widely adopted modeling strategies for switching converters [6], [7].

Parallel operation of DC-DC converters provides advantages such as increased power processing capability, improved reliability due to a more even distribution of stresses, enhanced availability from fault tolerance made possible with converters, redundancy, expandability of the output power, ease of standardization, improved thermal management, etc. Generally, it is desirable to distribute a load current equally among paralleled converters. However, due to limited components' tolerances and the asymmetric layout of converters, their output currents can be significantly different To balance the load current among paralleled modules, a variety of approaches, with different complexities and current-sharing performances have been proposed and employed [8]–[11]. The simplest current-sharing technique is the open-loop (droop) method, which relies on the output resistance of paralleled modules to maintain a relatively even current distribution [8]–[10]. The average current mode control, the active current sharing control and the master slave current sharing control of multi-module parallel DC-DC PWM converters with improved dynamic response has been reported in [12]–[15].

Due to the fact that DC-DC converters are inherently variable structure systems (VSS) (i.e. their topology changes during operation), they are a very well-suited application for the sliding mode theory. Sliding-mode control (SMC) is an effective method of designing the control loops of parallel systems controlled by democratic or master-slave current-control schemes [16]–[18]. Essentially, SMC utilizes a high-speed switching control law to drive the nonlinear state trajectory

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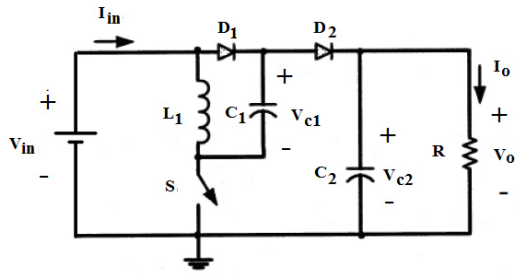


Fig. 1. The POESLLC circuit.

onto a specified surface in the state space, called the sliding or switching surface, and to maintain it on this surface for all subsequent time. The main advantages of SMC over conventional controllers are its improved stability, robustness, good dynamic response, and implementation simplicity. Various sliding mode strategies to control DC-DC power converters have been reported [19]–[26].

In this paper, the Current Distribution Control (CDC) design for Paralleled POESLLCs (PPOESLLCs) is proposed in Continuous Conduction Mode (CCM) using SMC. The state-space average model for a POESLLC is first derived and then the SMC is designed. A detailed discussion of the hitting, existence and stability conditions of the SMC for PPOESLLCs is also presented. The performance of the SMC versus a PI controller is evaluated in terms of robustness and current distribution capability. This initiative and attempt to implement SMC for VSS in an analog platform will be a useful contribution to researchers working in this field.

Section II presents the operation and a mathematical model of the POESLLC. The design of the SMC for PPOESLLCs is presented in section III. The design computation of the PPOESLLC's circuit components and the controller gains is well executed in section IV. Simulation results of the system using both the SMC and a PI controller in various regions are discussed in section V. The experimental results of the PPOESLLC using SMC in various regions are discussed in section VI. The conclusions are discussed in Section VII.

II. POESLLC AND MATHEMATICAL MODEL

A. Converter operation

A power circuit diagram of the POESLLC is shown in Fig. 1. It includes the DC input supply voltage V_{in}, the capacitors C_1 and C_2, the inductor L_1, the power switch (n-channel MOSFET) S, the freewheeling diodes D_1 and D_2, and the load resistance R. It is assumed that all of the components are ideal and also that the POESLLC operates in CCM. Fig. 2(a) and 2(b) show the modes of operation for the POESLLC [1].

In Fig. 2 (a), when the switch S is closed, the capacitor C_1 is charged to Vin and the current i_{L1} flows through the inductor L_1 which increases with the voltage V_{in}.

In Fig. 2 (b) when the switch S is open, the inductor voltage decreases with the voltage, $-(V_o - 2V_{in})$. Therefore, the ripple of the inductor current i_{L1} may be written as:

$$\Delta_{iL1} = \frac{V_{in}}{L_1} dT = \frac{V_o - 2V_{in}}{L_1} dT \tag{1}$$

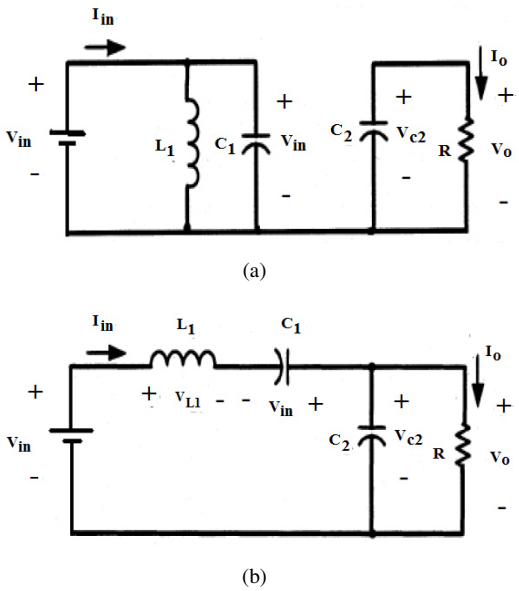


Fig. 2. Mode 2 operation of the POESLLC.

$$V_o = \frac{2-d}{1-d} V_{in}. \tag{2}$$

The voltage transfer gain is:

$$G = \frac{V_o}{V_{in}} = \frac{2-d}{1-d} \tag{3}$$

The input current i_{in} is equal to $(i_{L1} + i_{C1})$ during switching-ON and it is just equal to i_{L1} during OFF. The capacitor current i_{C1} is equal to i_{L1} during the switching-off. In the steady state, the average charges across the capacitor C_1 should not change.

$$\begin{aligned} i_{in-off} &= i_{L1-off} = i_{C1-off}, \\ i_{in-on} &= i_{L1-on} + i_{C1-on} \\ dT\, i_{C1-on} &= (1-d) T i_{C1-off}. \end{aligned} \tag{4}$$

If the inductance L_1 is large enough, i_{L1} is nearly equal to its average current i_{L1}. Therefore:

$$\begin{aligned} &i_{in-off} = i_{L1} = i_{C1-off}, i_{in-on} = i_{L1} + \frac{1-d}{d} \frac{i_{L1}}{d} \\ &i_{C1-on} = \frac{(1-d)}{d} i_{L1} \end{aligned} \tag{5}$$

and the average input current is:

$$I_{in} = d i_{in-on} + (1-d) i_{in-off} = i_{L1} + (1-d) i_{L1} = (2-d) i_{L1}. \tag{6}$$

Considering $T = \frac{1}{f}$ and:

$$\frac{V_{in}}{I_{in}} = \left(\frac{(1-d)}{(2-d)} \right)^2 \frac{V_o}{I_o} = \left(\frac{(1-d)}{(2-d)} \right)^2 R. \tag{7}$$

The variation ratio of the inductor currenti_{L1} is:

$$\xi = \frac{\Delta_{iL1/2}}{i_{L1}} = \frac{d(2-d) T V_{in}}{2 L_1 I_{in}} = \frac{d(1-d)^2}{2(2-d)} \frac{R}{f L_1}. \tag{8}$$

The ripple voltage of the output voltage V_o is:

$$\Delta_{vo} = \frac{\Delta Q}{C_2} = \frac{I_o (1-d) T}{C_2} = \frac{(1-d)}{f C_2} \frac{V_o}{R}. \tag{9}$$

Therefore, the variation ratio of the output voltage, V_o is:

$$\xi = \frac{\Delta_{vo}/2}{V_o} = \frac{(1-d)}{2 R f C_2}. \tag{10}$$

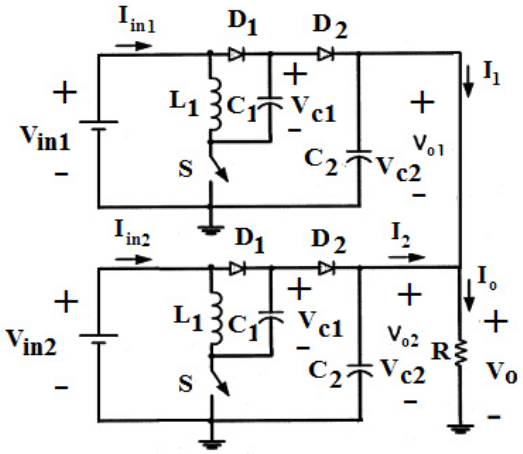


Fig. 3. The PPOESLLCs system.

B. Operation of PPOESLLCs

Connecting multi-module unit systems in parallel is a more efficient and reliable way of increasing the power ratings of the module units eradicating the limit of the low voltage and the current ceilings of power semi-conductor switches. For this reason, parallel-connected converters have been a viable alternative method of satisfying system power requirements beyond the capacity of the largest single module unit system.

Paralleled DC-DC converters require an explicit current sharing mechanism to ensure proper operation. There are a number of schemes available to achieve load current sharing viz. Average Current Sharing (ACS), the master slave scheme, the democratic current share scheme, the autonomous master-slave scheme, etc [8]–[16]. Proper load current sharing and the load voltage regulation of PPOESLLCs can also be achieved by using a control sucha as SMC. A well designed SMC can force the current and the voltage in paralleled modules to follow their references. The main benefits of SMC, when compared to convention controllers, are the robustness that the system acquires against disturbances in the load and in the input voltage. A PPOESLLC system with two modules connected in parallel is considered for study as shown in Fig. 3.

C. State space average mathematical model of POESLLC

The state variables of a POESLLC (x_1, x_2 and x_3) are chosen as the current i_{L1}, the voltage V_{C1} and voltage V_{C2}, respectively. When the switch is closed (Fig. 2(a)), the state space equation can be expressed as:

$$\begin{cases} \dot{x_1} = \dfrac{V_{in}}{L_1} \\ \dot{x_2} = \dfrac{V_{in}}{C_1 R_{in}} - \dfrac{x_1}{C_1} \\ \dot{x_3} = -\dfrac{x_3}{RC_2}. \end{cases} \tag{11}$$

Similarly, when the switch is open (Fig.2 (b)), the state space equation can be expressed as:

$$\begin{cases} \dot{x_1} = \dfrac{V_{in}}{L_1} - \dfrac{x_2}{L_1} - \dfrac{x_3}{L_1} \\ \dot{x_2} = \dfrac{x_1}{C_1} \\ \dot{x_3} = \dfrac{x_1}{C_2} - \dfrac{x_3}{RC_2} \end{cases}. \tag{12}$$

The state-space modeling of an equivalent circuit of a POESLLC with the state variables i_{L1}, V_{C1} and V_{C2} is given by [6], [7]:

$$\begin{bmatrix} \dfrac{di_{L1}}{dt} \\ \dfrac{dV_{C1}}{dt} \\ \dfrac{dV_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{L_1} & -\dfrac{1}{L_1} \\ \dfrac{1}{C_1} & 0 & 0 \\ \dfrac{1}{C_2} & 0 & -\dfrac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_{C1} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} \dfrac{V_{C1}+V_{C2}}{L_1} \\ -\dfrac{2i_{L1}}{C_1} - \dfrac{V_{C1}}{R_{in}C_1} + \dfrac{V_{in}}{R_{in}C_1} \\ -\dfrac{i_{L1}}{C_2} \end{bmatrix} \gamma + \begin{bmatrix} \dfrac{V_{in}}{L_1} \\ 0 \\ 0 \end{bmatrix} \tag{13}$$

$$\dot{x} = Ax + B\gamma + C \tag{14}$$

where, R_{in} is the internal resistance of the source and this small value is not shown in the circuit. γ is the status of the switches, while x and $\dot{x}$ are the vectors of the state variables (i_{L1}, V_{C1} , V_{C2}) and their derivatives, respectively.

$$\gamma = \begin{cases} 1 \to S \to ON \\ 0 \to S \to OFF. \end{cases} \tag{15}$$

III. Design of the SMC

Sensing of all of the state variables and the generation of suitable references for each of them are the basic requirements of a SMC. According to the principles of a SMC, the capacitor voltages V_{c1} and V_{c2} are made to follow their references as faithfully as possible. However, the inductor current reference is difficult to evaluate since it generally depends on the load power demand supply voltage and the load voltage. To overcome this problem in implementation, the state variable error for the inductor current (i_{L1}-i_{L1ref}) can be obtained from the feedback variable i_{L1} by means of a high-pass filter under the assumption that their low-frequency component is automatically adapted to the actual converter operation. Thus, only the high-frequency component of this variable is needed for the control. This high pass filter increases the system order and can heavily alter the converter dynamics. In order to avoid this problem, the cutoff frequency of the high-pass filter must be suitably lower than the switching frequency to pass the ripple at the switching frequency, but high enough to allow a fast converter response [25].

In the design of the converter, the assumptions viz. ideal power switches, a power supply free of dc ripple and a

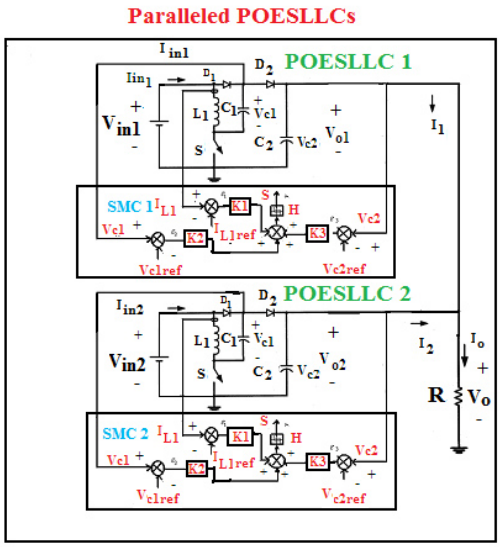


Fig. 4. Principle scheme of SMC applied to PPOESLLCs circuit.

converter operating at a high-switching frequency are considered. To have a good response in the output voltage and proper current sharing of the PPOESLLCs, a sliding surface equation in the state space, which is expressed by a linear combination of the state-variable errors ε (the respective differences of the feedback reference current/voltage and the feedback current/voltage), must be selected optimally.

$$S(i_{L1},V_{C1},V_{C2}) = K_1\varepsilon_1 + K_2\varepsilon_2 + K_3\varepsilon_3 \tag{16}$$

where the coefficients K_1, K_2 and K_3 are the proper gains, ε_1 is the feedback current error, ε_2 is the feedback voltage error and ε_3 is the feedback voltage error, or:

$$\begin{aligned} \varepsilon_1 &= i_{L1} - i_{L1ref} \\ \varepsilon_2 &= V_{C1} - V_{C1ref} \\ \varepsilon_3 &= V_{C2} - V_{C2ref}. \end{aligned} \tag{17}$$

By substituting (17) in (16), the following is obtained:

$$\begin{aligned} S(i_{L1},V_{C1},V_{C2}) = K_1(i_{L1} - i_{L1ref}) + K_2(V_{C1} - V_{C1ref}) \\ + K_3(V_{C2} - V_{C2ref}). \end{aligned} \tag{18}$$

The signal, S (i_{L1}, V_{C1}, V_{C2}), is generated using (16) while a conventional hysteresis modulator generates the gate pulses to the n-channel MOSFET switch. The complete control arrangement of a PPOESLLC is shown in Fig. 4. The status of the switch (γ) is controlled by hysteresis block H, which aims to minimize the error of the variables i_{L1}, V_{C1} and V_{C2}. The system response is determined by the circuit parameters and the coefficients K_1, K_2 and K_3. With a proper selection of these coefficients under any operating conditions, a high control robustness, stability, and a fast response can be achieved.

A. Selection of control parameters

Once the PPOESLLC's parameters are selected, the inductance L_1 is designed from specified input and output current ripples, the capacitors C_1 and C_2 are designed so as to limit the output voltage ripple in the case of fast and large load variations, and the maximum switching frequency is selected based on the proposed converter ratings and switch type. The system behavior is completely determined by the coefficients K_1, K_2 and K_3, which must be selected so as to satisfy the existence condition and ensure stability and a fast response, even under large supply and load variations.

According to the variable structure system theory, the converter equations must be written in the following form [25], [26]:

$$\dot{x} = Ax + B\gamma + D \tag{19}$$

where, x represents the vector of the state-variables errors, given by:

$$\dot{x} = x - X^* \tag{20}$$

where, $X^* = \left[i_{Lref}, V_{C1ref}, V_{C2ref}\right]^T$ is the vector of the references. The substitution of (20) into (13) results in:

$$D = AX^* + C \tag{21}$$

$$D = \begin{bmatrix} 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L1ref} \\ V_{C1ref} \\ V_{C2ref} \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ 0 \end{bmatrix} \tag{22a}$$

$$D = \begin{bmatrix} -\frac{V_{C1ref}}{L_1} - \frac{V_{C2ref}}{L_1} + \frac{V_{in}}{L_1} \\ \frac{i_{L1ref}}{C_1} \\ \frac{i_{L1ref}}{C_2} - \frac{V_{C2ref}}{RC_2} \end{bmatrix} \tag{22b}$$

By substituting (20) into (18), the sliding function can be rewritten in the form:

$$S(x) = K_1x_1 + K_2x_2 + K_3x_3 = K^Tx \tag{23}$$

where, $K^T = [K_1, K_2, K_3]$ and $x = [x_1, x_2, x_3]^T$.

The existence condition of the sliding mode requires that all of the state trajectories near the surface be directed toward the sliding plane. The controller can enforce the system state to remain near the sliding plane by proper operation of the converter switch. To make the system state move toward the switching surface, it is necessary and sufficient that [24]–[26]:

$$\begin{cases} \dot{S}(x) < 0, & \text{if } S(x) > 0 \\ \dot{S}(x) > 0, & \text{if } S(x) < 0. \end{cases} \tag{24}$$

The SMC is obtained by means of the following feedback control strategy, which relates to the status of a switch with the value of $S(x)$:

$$\gamma = \begin{cases} 0, & \text{for } S(x) > 0 \\ 1, & \text{for } S(x) < 0. \end{cases} \tag{25}$$

The existence condition (24) can be expressed in the form:

$$\dot{S}(x) = K^TAx + K^TD < 0, \quad S(x) > 0 \tag{26}$$

$$\dot{S}(x) = K^TAx + K^TB + K^TD > 0, \quad S(x) < 0. \tag{27}$$

For the simulation, by assuming that the error variable x_i is suitably smaller than the references V^*, (26) and (27) can be rewritten as:

$$K^TD < 0, S(x) > 0 \tag{28}$$

$$K^TB + K^TD > 0, S(x) < 0. \tag{29}$$

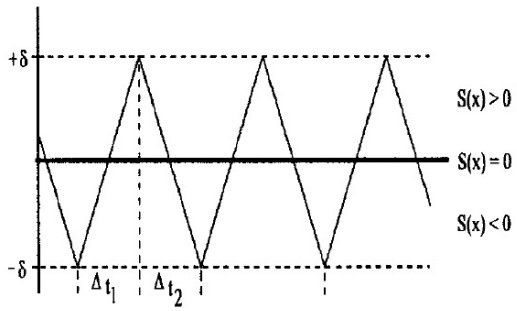


Fig. 5. Trajectory of $S(x)$.

By substituting the matrices B and D into (28) and (29), the following is obtained:

$$\frac{K_1}{L_1}\left[V_{C1ref}-V_{C2ref}+V_{in}\right]+\frac{K_2 i_{L1ref}}{C_1}+\frac{K_3}{C_2R}\left[Ri_{L1ref}-V_{C2ref}\right]<0 \tag{30}$$

$$\frac{K_1}{L_1}\left[V_{in}\right]-\frac{K_2}{C_1R_{in}}\left[V_{C1}-V_{in}\right]-K_2 i_{L1ref}-\frac{K_3V_{C2ref}}{RC_2}>0. \tag{31}$$

The existence condition is satisfied if the inequalities (30) and (31) are true.

Finally, it is necessary to guarantee that the designed sliding plane is reached for all of the initial states. If the sliding mode exists, in a system defined by (19), it is sufficient that the coefficients K_1, K_2 and K_3 be non-negative.

B. Switching frequency

In an ideal sliding mode at an infinite switching frequency, the state trajectories are directed toward the sliding surface and move exactly along it. A practical system cannot switch at an infinite frequency. The operating range of the average switching frequency of the hysteresis relay varies from 50 kHz to 450 kHz and its corresponding band varies from 0.1 to 1. From this operating range, the optimum value for the chosen average switching frequency is 100 kHz and its corresponding band is 0.5.

A practical relay always exhibits hysteresis modeled by:

$$\gamma(s)=\begin{cases}0, & \text{when } S>+\delta \text{ or}\\ & \text{when } \dot{S}<0 \text{ and } |S|<\delta\\ 1, & \text{when } S<-\delta \text{ or}\\ & \text{when } \dot{S}>0 \text{ and } |S|<\delta\end{cases} \tag{32}$$

where, δ is an arbitrarily small positive quantity and 2δ is the amount of hysteresis in $S(x)$. The hysteresis characteristic makes it impossible to switch the control on the surface S(x)=0. As a result, switching occurs on the lines $S=\pm\delta$, with a frequency depending on the slopes of i_{L1}. This hysteresis causes phase plane trajectory oscillations of width 2δ, near the surface $S(x)=0$, as shown in Fig. 5.

Note that Fig. 5 simply confirms that in Δt_1, the function $S(x)$ must increase from $-\delta$ to δ ($\dot{S}>0$), while in Δt_2, it must decrease from $+\delta$ to δ ($\dot{S}<0$). The switching frequency equation is obtained from Fig. 6 by considering that the state trajectory is invariable, near the sliding surface $S(x)=0$, and is given by:

$$f_s=\frac{1}{\Delta t_1+\Delta t_2} \tag{33}$$

where, Δt_1 is the conduction time of the switch S and Δt_2 is the off time of the switch S. The conduction time Δt_1 is derived from (31) and it is given by:

$$\Delta t_1=\frac{2\delta}{\frac{K_1}{L_1}\left[V_{in}\right]-\frac{K_2}{C_1R_{in}}\left[V_{C1}-V_{in}\right]-K_2 i_{L1ref}-\frac{K_3V_{C2ref}}{RC_2}}. \tag{34}$$

The off time Δt2 is derived from (30), and it is given by:

$$\Delta t_2=\frac{-2\delta}{\frac{K_1}{L_1}\left[V_{C1ref}-V_{C2ref}+V_{in}\right]+\frac{K_2 i_{L1ref}}{C_1}+\frac{K_3}{C_2R}\left[Ri_{L1ref}-V_{C2ref}\right]}. \tag{35}$$

The maximum value of the switching frequency is obtained by substituting (34) and (35) into (33) with the assumption that the converter is operating under no load ($i_{L1ref}=0$ and $1/R=0$) and the output voltage reference is crossing its maximum value ($V_{C2ref(max)}$). The maximum switching frequency is obtained as:

$$f_{s(\max)}=\frac{K_1V_{in}}{2\delta L_1}\left(1-\frac{V_{in}}{V_{C1ref(\max)}+V_{C2ref(\max)}}\right). \tag{36}$$

C. Duty cycle

The duty cycle $d(t)$ is defined by the ratio between the conduction time of the switch S and the switch period time, as represented by:

$$d(t)=\frac{\Delta t_1}{\Delta t_1+\Delta t_2}. \tag{37}$$

Considering the SMC, an instantaneous control, the ratio between the output and the input voltages must satisfy the fundamental relation under any working condition.

$$\frac{V_o}{V_{in}}=\frac{1}{1-d(t)}. \tag{38}$$

D. Inductor current

The high-frequency or maximum inductor current ripple is obtained from Fig.2 and is given by:

$$\Delta i_{L1}=\left(\frac{V_{in}-R_a i_{L1}(t)}{L_1}\right)\Delta t_1. \tag{39}$$

E. Voltage capacitor V_{C2}

The controller operates over the switch to make the voltage V_{C2} follow a low-frequency reference. Over $V_{C2}(t)$, a high-frequency ripple (switching) is imposed, which is given by:

$$\Delta V_{C1}(t)=\frac{V_{in}}{R_{in}C_1}-\frac{V_{C2}(t)}{RC_2}\Delta t_1$$
$$\Delta V_{C2}(t)=-\frac{V_{C2}(t)}{RC_2}\Delta t_1. \tag{40}$$

It is interesting to note that the switching frequency, the inductor current ripple, and the capacitor voltage ripple depend

on the control parameters, the circuit parameters, the reference voltage, the output capacitor voltage $V_{C2}(t)$, and the inductor current $i_{L1}(t)$.

It is important to determine circuit parameters and coefficients K_1, K_2 and K_3 that agree with the desirable values for a maximum inductor current ripple, a maximum capacitor voltage ripple, a maximum switching frequency, stability, and a fast response under any operating condition.

IV. Design Calculations of Circuit Components and Controller Parameters

The main purpose of this section is to use the previously deduced equations to calculate the PPOESLLC's components values and controller parameters.

A. Calculation of V_{C2}

From (37) and simulation simplicity, an output voltage is chosen to produce a duty cycle close to 0.56. The output voltage is taken as 36 V as mentioned in Table 1, and a variation of the duty cycle between $d_{min} = 0.3$ and $d_{max} = 0.9$ is expected. Finally, $V_{C2max} = 132$V.

B. Determination of ratio K_1/L_1

Substituting V_{in}, $V_{C1ref(max)} = V_{C1(max)}$ and $\delta = 0.3$ into (35) results in $K_1/L_1 = 6666.67$.

C. Determination of the ratios K_2/C_1 and K_3/C_2

From (30) and (31) and selecting $i_{L1ref} = i_{L1(max)} = 2.353$A, the conditions obtained are $1208 < K_2/C_1 < 248433$ and $1208 < K_3/C_2 < 248433$, respectively.

There are some degrees of freedom in choosing the ratios K_2/C_1 and K_3/C_2. In this controller, the ratios K_2/C_1 and K_3/C_2 are tuning parameters. It is recommended that the ratios K_2/C_1 and K_3/C_2 be chosen so that they agree with the required levels of stability and response speed. The ratios K_2/C_1 and K_3/C_2 are chosen by an iterative procedure (the ratio is modified until the transient response is satisfactory), and they are verified by simulation. Finally, the optimum tuned adopted value for the ratios K_2/C_1 and K_3/C_2 is 7248.

D. Calculation of L_1

The maximum inductor current ripple is chosen to be equal to 15 % of the maximum average inductor current and $L_1 = 100\mu$H, which is obtained from (36).

E. Calculation of C_1 and C_2

The maximum capacitor ripple voltages ΔV_{C1max} and ΔV_{C2max} are chosen to be equal to 0.5 % of the maximum capacitors voltage, and $C_1 = C_2 = 30\mu$F, which is obtained from (39).

F. Values of the coefficients K_1, K_2 and K_3

Having decided on the values of the ratio K_1/L_1 and inductor, the value of K_1 is unswervingly obtained ($K_1 = 0.667$). Similarly the $K_2 = K_3 = 0.217$ is computed using the ratio K_2/C_1 and K_3/C_2 and the C_1, C_2.

TABLE I
Parametrs of PPOESLLCs

Parameters name	Symbol	Value
Input Voltage	V_{in1} , V_{in2}	12V
Output Voltage	V_o	36V
Inductor	L_1	100μH
Capacitors	C_1, C_2	30 μF
Nominal switching frequency	F_s	100kHz
Load resistance	R	50Ω
Output power	P_o	25.92W
Input power	P_{in}	28.236W
Input current of module 1 and 2	I_{in1} , I_{in2}	1.1765 A
Efficiency	η	91.79%
Output current	I_o	0.72 A
Input current	I_{in}	2.353 A
Range of duty ratio	d	0.3 to 0.9

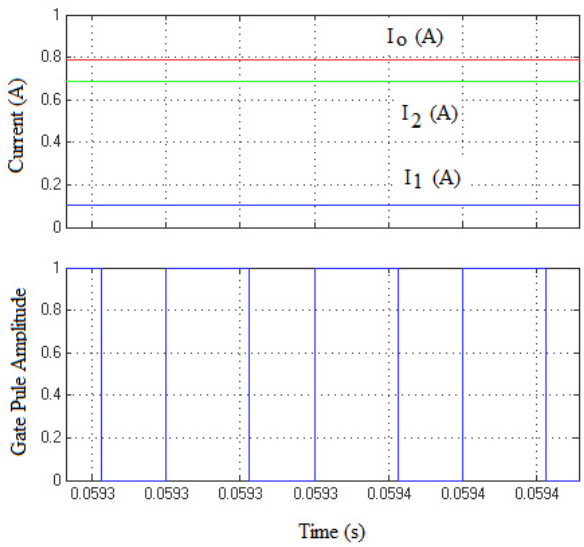


Fig. 6. Response of average output current of PPOESLLCs without current sharing controller for input voltage $V_{in1} = 12$ V & $V_{in2} = 15$ V, d = 0.56.

V. Simulation Results

The main purpose of this section is to discuss the simulation studies of the PPOESLLCs with SMC. A PI controller with the settings $K_p = 0.01205$ and $T_i = 0.0133$s obtained by the Ziegler-Nichols tuning technique [27], [28] is used for comparison with the designed SMC. The validation of the system performance is done for five different conditions viz. the start up transient, line variation, load variation, steady state and component variations.

Simulations are performed on the PPOESLLC's circuits with the parameters listed in Table I using MatLab/Simulink.

Table II presents the simulated results of the voltage and current profiles of PPOESLLCs without controllers for various input voltages and load resistances.

Fig. 6 shows the average output currents and the gate pulse of paralleled modules without a controller for different input voltages ($V_{in1} = 12$V & $V_{in2} = 15$V, d = 0.56). It can be seen that the current sharing of all of the modules and the PPOESLLCs are unequal.

Table II lists the simulated results of the average output current/voltage for each of the modules and the PPOESLLCs without controllers for various input voltages and load resistances. From this table, it can be clearly seen that the voltage regulation and the current distributions of each of the modules

TABLE II
PERFORMANC OF PPOESLLCS WITHOUT CONTROLLERS.

Change in V_{in1} & V_{in2} (V)	V_{o1} (V)	V_{o2} (V)	V_o (V)	I_1 (A)	I_2 (A)	I_o (A)
09	27.24	27.24	27.24	0.202	0.342	0.544
12	36.85	36.85	36.85	0.308	0.428	0.736
15	46.45	46.45	46.45	0.294	0.524	0.821
Change in R (Ω)	V_{o1} (V)	V_{o2} (V)	V_o (V)	I_1 (A)	I_2 (A)	I_o (A)
10	34.42	34.42	34.42	2.414	1.041	3.427
50	36.85	36.85	36.85	0.308	0.428	0.736
60	36.92	36.92	36.92	0.315	0.300	0.614

and the PPOESLLCs are in inequality.

A. Start-up transients

Fig. 7 (a) shows the dynamic behavior at startup for the output voltage of paralleled modules for different input voltages viz. 9V, 12V and 15V. It can be seen that the output voltage of the paralleled modules has a little overshoot and a settling time of 0.008 s for $V_{in} = 15$ V, whereas for 12 V and 09 V there are negligible overshoots and a settling time of 0.01 s and 0.012 s for the designed SMC, respectively.

Fig.7(b) shows the dynamic behavior at startup in terms of the average output current of module 1 for different input voltage values. It can be seen that the output current of module 1 has a little overshoot and a settling time of 0.022 s for $V_{in} = 15$ V, while for 12 V and 09 V there exist a negligible overshoot and the settling times are 0.025 s and 0.028 s, respectively.

Fig.7(c) shows the dynamic behavior at startup for the average output current of module 2. The settling times are 0.022 s, 0.025 s and 0.028 s, respectively for 15 V, 12V and 09V, while the overshoot imitates the conclusions of the previous cases. Fig. 7(d) shows the dynamic behavior at startup for the average output current of paralleled modules. Fig. 8 represents the dynamic behavior in the state plane of the total input current and output voltage designed for the SMC and PI controllers in the sliding surfaces.

As can be seen, in the SMC the total input current of the modules goes up to 2.353 A and the output voltage of the modules goes up to 36 V (without overshoot), where as in the PI controller, the total input current of the modules goes up to 3.33 A (the input current exceeds the adopted value in Table 1) and the output voltage of the modules goes up to 36.6 V (with overshoot).

Fig. 9(a) shows the dynamic behavior at startup of the output voltage of paralleled modules for different load resistances like 40 Ω, 50 Ω and 60 Ω. It can be seen that the output voltage of the paralleled modules has a slight overshoot and a settling time of 0.012 s for $R = 60\Omega$, whereas the output voltage of the paralleled modules for $R = 50\Omega$ and $R = 40\Omega$ has a negligible overshoot and settling times of 0.013 s and 0.014 s, with the designed SMC.

Fig. 9(b) shows the dynamic behavior at startup for the average output current of module 1 for different load resistances like 40 Ω, 50 Ω and 60 Ω. It can be seen that the output current of module 1 for $R = 40\Omega$, $R = 50\Omega$ and $R = 60\Omega$ has a negligible overshoot and settling times of 0.03 s, 0.025 s and 0.021 s, with the designed SMC.

TABLE III
VOLTAGE/CURRENT PROFILES OF PPOESLLCS FOR VARIOUS INPUT VOLTAGES AND LOAD RESISTANCES WITH NOMINAL INPUT VOLTAGE/LOAD IN START-UP REGION

Line Variation 9V- 15V (Start-up region)	Voltage Profiles					
	PI			SMC		
	V_{o1} (V)	V_{o2} (V)	V_o (V)	V_{o1} (V)	V_{o2} (V)	V_o (V)
	36.05	36.05	36.05	36	36	36
Load Variation 40Ω-60Ω (Start-up region)	Current Profiles					
	PI			SMC		
	I_1 (A)	I_2 (A)	I_o (A)	I_1 (A)	I_2 (A)	I_o (A)
40Ω	0.441	0.441	0.882	0.45	0.45	0.9
50Ω	0.358	0.358	0.716	0.36	0.36	0.72
60Ω	0.291	0.291	0.582	0.3	0.3	0.6

Fig. 9 (c) shows the dynamic behavior at startup for the average output current of module 2 for different load resistances like 40 Ω, 50 Ω and 60 Ω. It can be seen that the output current of module 2 for $R = 40\Omega$, $R = 50\Omega$ and $R = 60\Omega$ has a negligible overshoot and settling times of 0.03 s, 0.025 s and 0.021 s, with the designed SMC.

Fig. 9(d) shows the dynamic behavior at startup for the average output current of the modules for different load resistances like 40 Ω, 50 Ω and 60 Ω. It can be seen that the output current of the modules for $R = 40\Omega$, $R = 50\Omega$ and $R = 60\Omega$ has a negligible overshoot and settling times of 0.03 s, 0.025 s and 0.021 s, with the designed SMC. Table 3 lists the simulated results of the average output current and voltage of each of the modules and the PPOESLLCs with controllers for various input voltages and load resistances in the start-up region. From this table, it can be seen that the voltage regulation and the current distributions of each of the modules and the PPOESLLCs using the designed SMC show excellent performance in comparison with a conventional PI controller.

B. Line variations

In Fig. 10(a) shows the response of the average output voltage of paralleled modules using both a PI controller and the SMC for an input voltage step change from 12 V to 15 V (+30% line variations) at time = 0.1s. It can be seen that the output voltage of the paralleled modules using the SMC has a maximum overshoot of 3.8 V and a settling time of 0.01 s, while the output voltage of the paralleled modules using a PI controller has a severely affected overshoot of 12V and a long settling time of 0.02s, respectively.

Fig. 10(b) shows the response of the average output voltage of the SMC with paralleled modules using both a PI controller and the SMC for an input voltage step change from 12 V to 9 V (−30% line variations) at time = 0.1s. It can be seen that the output voltage of the paralleled modules using the SMC has a maximum overshoot of 4 V and a settling time of 0.01 s, while the output voltage of the paralleled modules using a PI controller has a maximum overshoot of 10V and a long settling time of 0.02s, respectively.

C. Load variations

Fig. 11(a) Response of output voltage of paralleled modules when load value takes a step changes from 50 Ω to 60Ω.

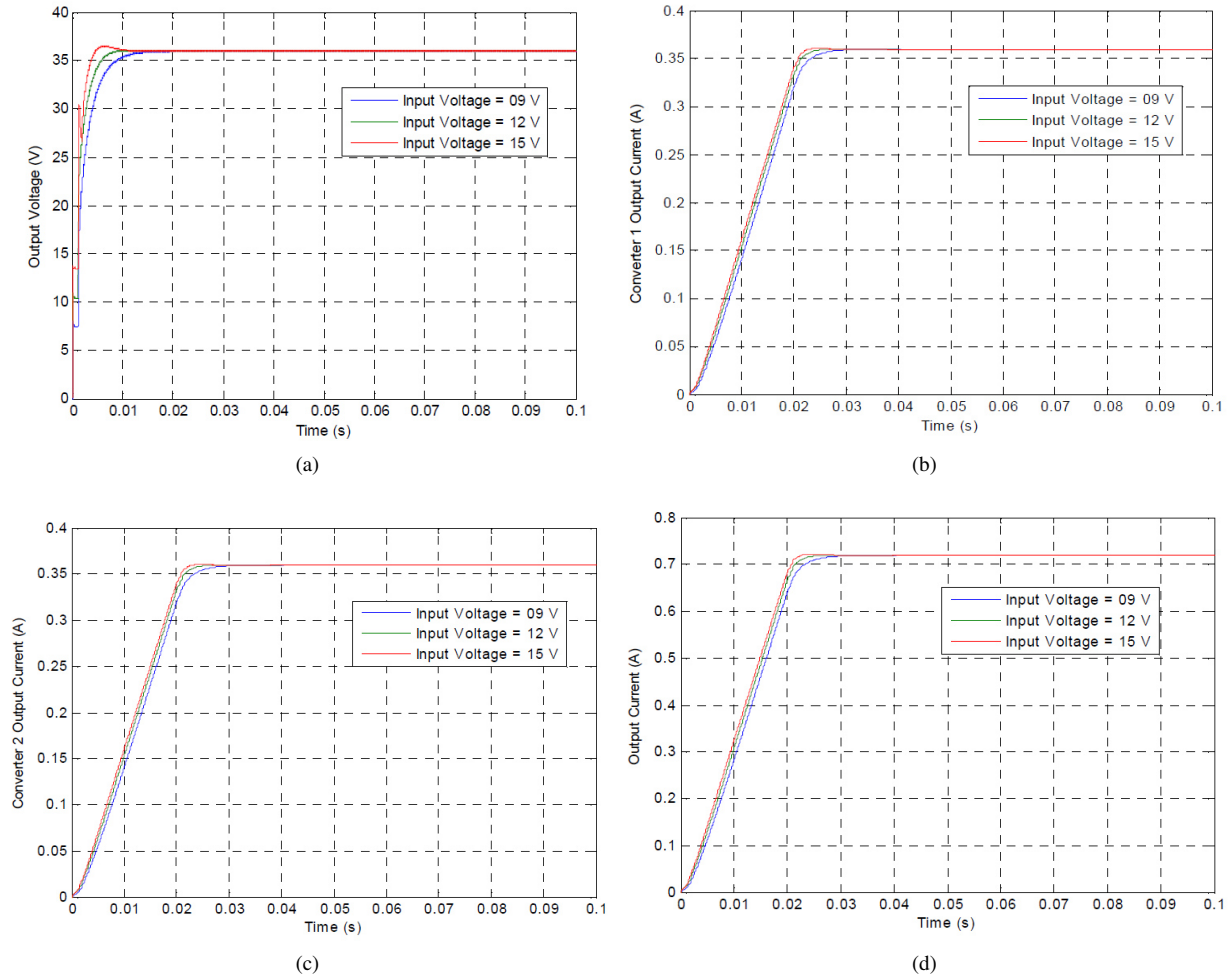


Fig. 7. (a) Response of average output voltage of PPOESLLCs in startup for various input voltage. (b) Response of average output voltage of PPOESLLC 1 in startup for various input voltage. (c) Response of average output current of PPOESLLC 2 in startup for various input voltages. (d) Response of average output current of PPOESLLCs in startup for various input voltages.

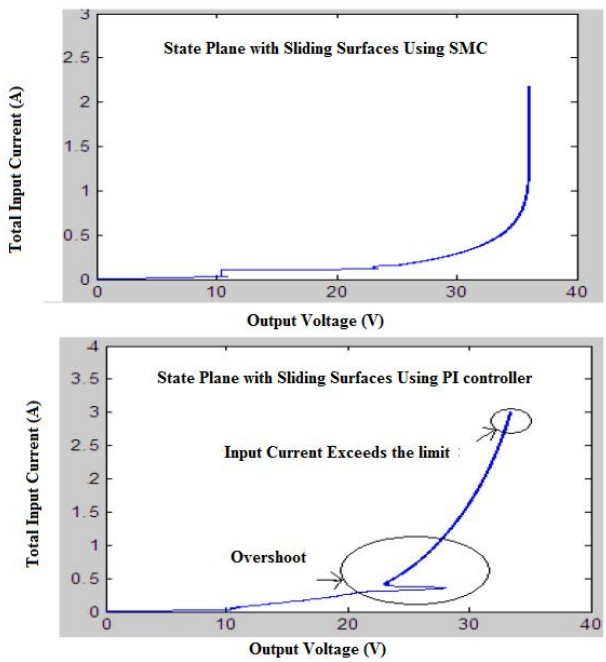


Fig. 8. System startup in the state plane with sliding surfaces.

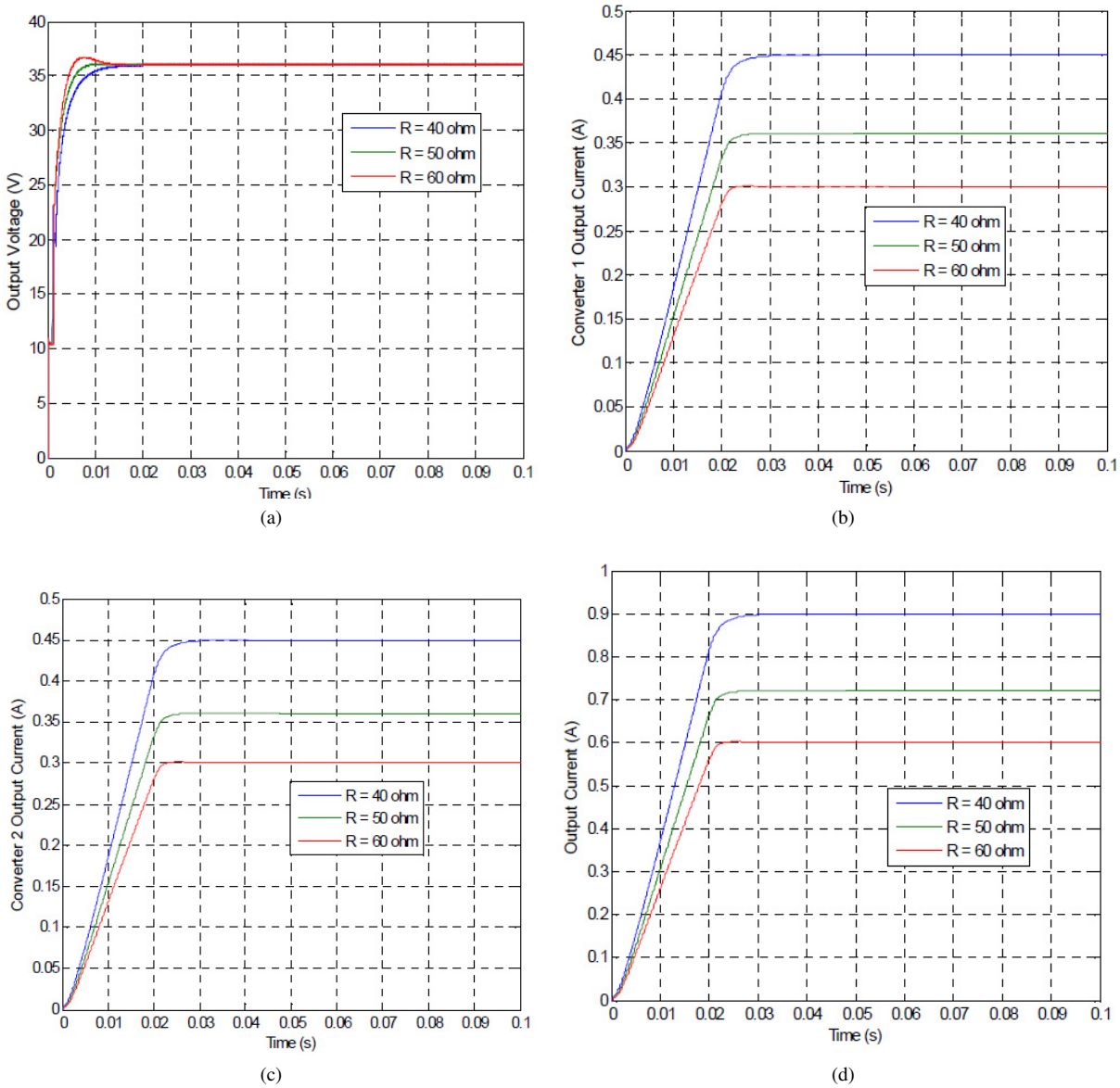


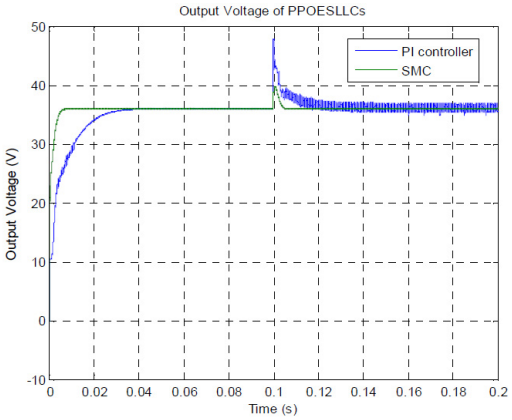
Fig. 9. (a) Response of output voltage of paralleled modules in startup for various load resistance. (b) Response of average output current of PPOESLLC 1 in startup for various load resistance. (c) Response of average output current of PPOESLLC 1 in startup for various load resistance. (d) Response of average output current of PPOESLLCs in startup for various load resistance.

(b) Response of output voltage of paralleled modules when load value takes a step changes from 50 Ω to 40Ω. (c) Time domain performance evaluation of PPOESLLCs using SMC versus PI controller under line disturbances in steady state operating region. (d) Time domain performance evaluation of PPOESLLCs using SMC versus PI controller under load disturbances in steady state operating region.

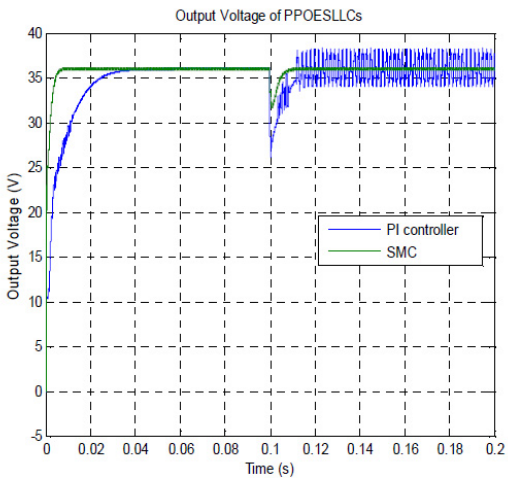
Fig. 11(a) shows the response of the output voltage of paralleled modules using both a PI controller and the SMC for a load step change from 50Ω to 60Ω (+20% load variations) at time = 0.1s. It can be seen that the output voltage of the paralleled modules using the SMC has a small overshoot of 1.8 V with a settling time of 0.01 s, while the output voltage of the paralleled modules using a PI controller has a maximum overshoot of 3V and a settling time of 0.02s, respectively.

Fig. 11(b) shows the response of the output voltage of paralleled modules using both a PI controller and the SMC for a load step change from 50 Ω to 40 Ω (−20% load variations) at time = 0.1s. It can be seen that the output voltage of the paralleled modules using the SMC has a maximum overshoot of 2.5 V with a settling time of 0.01 s, while the output voltage of the paralleled modules using a PI controller has a severely affected overshoot of 16V and a settling time of 0.02s, respectively.

Fig. 11(c) and 11(d) show the simulated time domain performance evaluation of the current/voltage profiles for PPOESLLCs using both the SMC and a PI controller. From these figures it can be clearly seen that the simulated results of the designed SMC exhibit better performance in comparison with a conventional PI controller under line and load disturbances



(a)



(b)

Fig. 10. (a) Response of output voltage of paralleled modules for input step change from 12V to 15 V. (b) Response of output voltage of paralleled modules for input step change from 12V to 9V.

under steady state operating conditions.

D. Steady state regions

Fig. 12(a) shows the instantaneous output voltage and the inductor current of paralleled modules in the steady state using the SMC. It is evident from this figure that the output voltage ripple is very small, about 0.08 V, and the peak to peak inductor ripple current is 0.9 A for an average switching frequency that is 100 kHz closer to the theoretical designed value listed in Table I.

Fig. 12(b) shows the instantaneous output voltage and the inductor current of paralleled modules in the steady state using a PI controller. It is evident from the figure that the output voltage ripple is little high, about 0.095 V, and the peak to peak inductor ripple current is 1 A.

E. Circuit components variations

Fig. 13(a) and 13(b) represent the response of the output voltage and current of paralleled modules using both the SMC and a PI controller for the variation of inductor L_1 from 100μH to 500μH. It can be seen that the change does not influence the paralleled converters behavior due to the proficient design of the SMC in comparison with a conventional PI controller.

An interesting result is illustrated in Fig. 13(c) and 13(d). It shows the response of the output voltage and the current of the paralleled modules with both a PI controller and the proposed control scheme for a variation in the capacitor's values from 30μF to 100μF. It can be seen that the SMC is very successful in suppressing the effect of the capacitance variation except that a negligible output voltage ripple with a quick settling time and a proper current distribution in comparison with a conventional PI controller. In summary, from the Fig. 13(a) to 13(d), it is clearly indicated that the designed SMC's simulated results show the excellent performance of the PPOESLLCs in comparison with a conventional PI controller during component variations.

VI. Experimental Results

The main purpose of this section is to discuss the experimental results of PPOESLLCs with the designed SMC. The validation of the system performance is done for different conditions viz. line variation, load variation, the steady state region and circuit components variations. The laboratory prototype model is performed on PPOESLLC circuits with the same specification as the simulations.

The laboratory prototype PPOESLLCs using the SMC circuits are shown in Fig. 14. The parameters of the power circuits are as follows:

S	IRFN 540 (MOSFET);
D1 - D2	FR306 (Diodes);
C1 - C2	30 μF/100V (Electrolytic and plain polyester type)
L1	100μH/5A (Ferrite Core)

The parameters of the controller are: $K_1 = 0.667$, $K_2 = K_3 = 0.217$ and $\delta = 0.3$ as calculated in the previous section. The designed SMC is implemented in an analog platform as shown in Fig. 14. and its operation is as follows; the inductor current and the capacitor voltages Vc1 and Vc2 of the PPOESLLCs are sensed by using an LA 25 – NP current sensor, resistances, capacitors and LM324 operational amplifiers, which are then compared with reference signals by using an LM324 operational amplifier that gives error signals. The inductor current error signal is further processed through a high pass filter (20 kHz) for the purpose of filtering out the low frequency component of the converter as the controller allows only high frequency signals. Then output of all of the SMC signals are summed, and then compared using an LM311 to generate the pulse width modulated (PWM) gate drive control signal. Afterwards, the generated gate signal is passed through the opt-isolator (MCT 2E) and the driver circuit (transistors SK100, 2N2222 and the resistances arrangement). In MOSFETs there is an internal capacitor in the gate terminal. Therefore, the transistors (2N2222 and SK100) are used as a quick charging and discharging capacitor and also for amplification. The output of the driver is directly connected to the gate of the MOSFET (IRFN 540) through the resistance as shown in Fig. 14. Using the SMC, the switching frequency of the gate pulse is varied to regulate the output current and

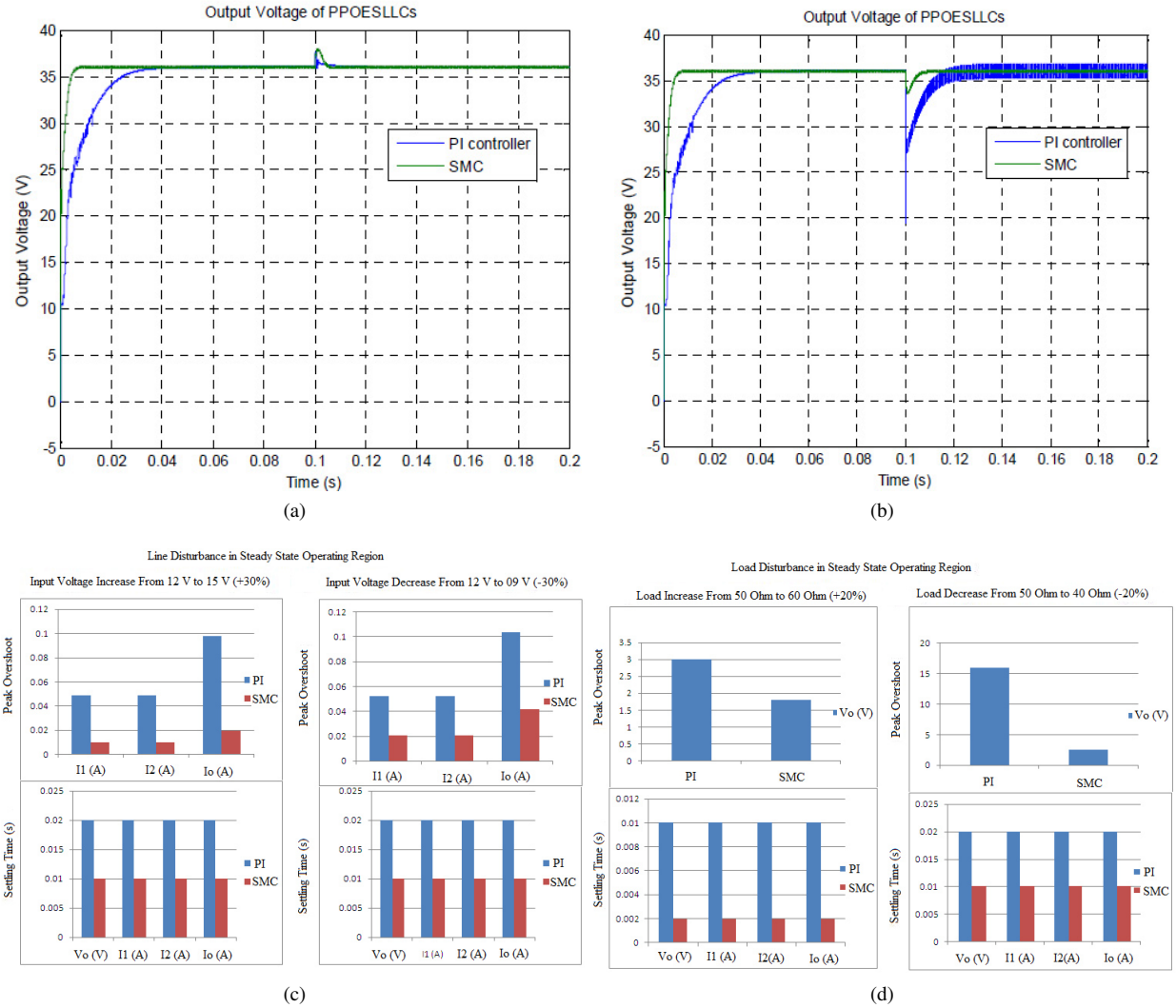


Fig. 11. (a) Response of output voltage of paralleled modules when load value takes a step changes from 50 Ω to 60Ω. (b) Response of output voltage of paralleled modules when load value takes a step changes from 50 Ω to 40Ω. (c) Time domain performance evaluation of PPOESLLCs using SMC versus PI controller under line disturbances in steady state operating region. (d) Time domain performance evaluation of PPOESLLCs using SMC versus PI controller under load disturbances in steady state operating region.

the voltage and also to improve the dynamic performance of the PPOESLLCs.

Fig. 15(a) and 15(b) show the dynamic behavior at startup for the average output currents of modules 1 and 2 for $V_{in1} =$ 12 V & $V_{in2} = 15$ V. It can be seen that the output current of modules 1 and 2 for $V_{in1} = 12$ V & $V_{in2} = 15$ V has an equal current distribution.

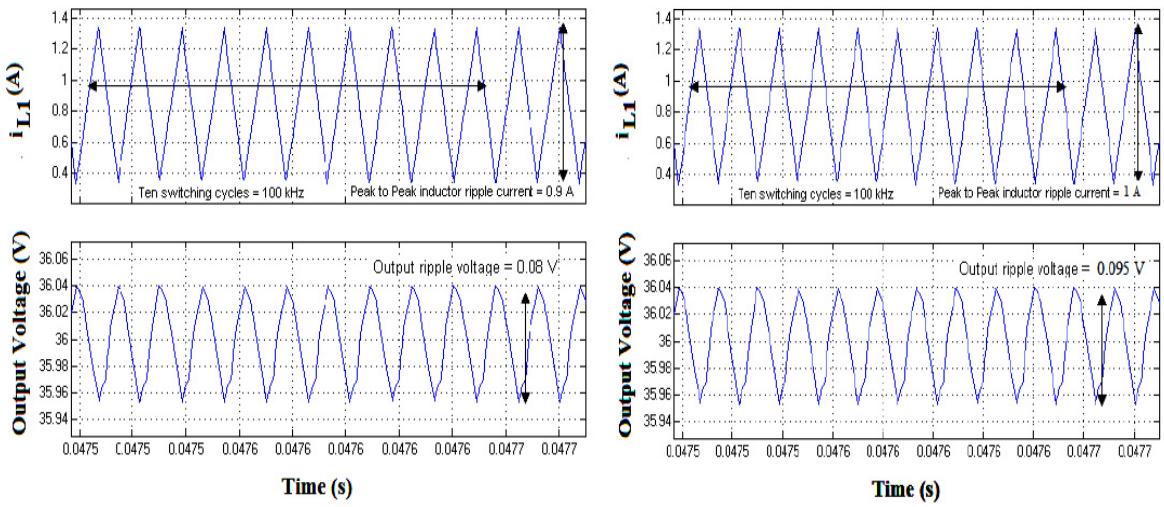
A. *Line variations*

Fig. 16(a) shows the experimental response of the average output voltage of the PPOESLLCs using the SMC for an input voltage step change from 12 V to 15 V (+30% line variations) at time = 0.05s. From these figures, it is clearly found from the experimental response that the output voltage of the PPOESLLCs using the SMC has a maximum overshoot of 2.6V and a settling time of 0.01 s.

Fig. 16(b) shows the experimental response of the average output voltage of the PPOESLLCs using the SMC for an input voltage step change from 12 V to 9 V (−30% line variations) at time = 0.05s. It can be seen from the experimental response that the output voltage of the PPOESLLCs using the SMC has a maximum overshoot of 3.2V and a settling time of 0.01s.

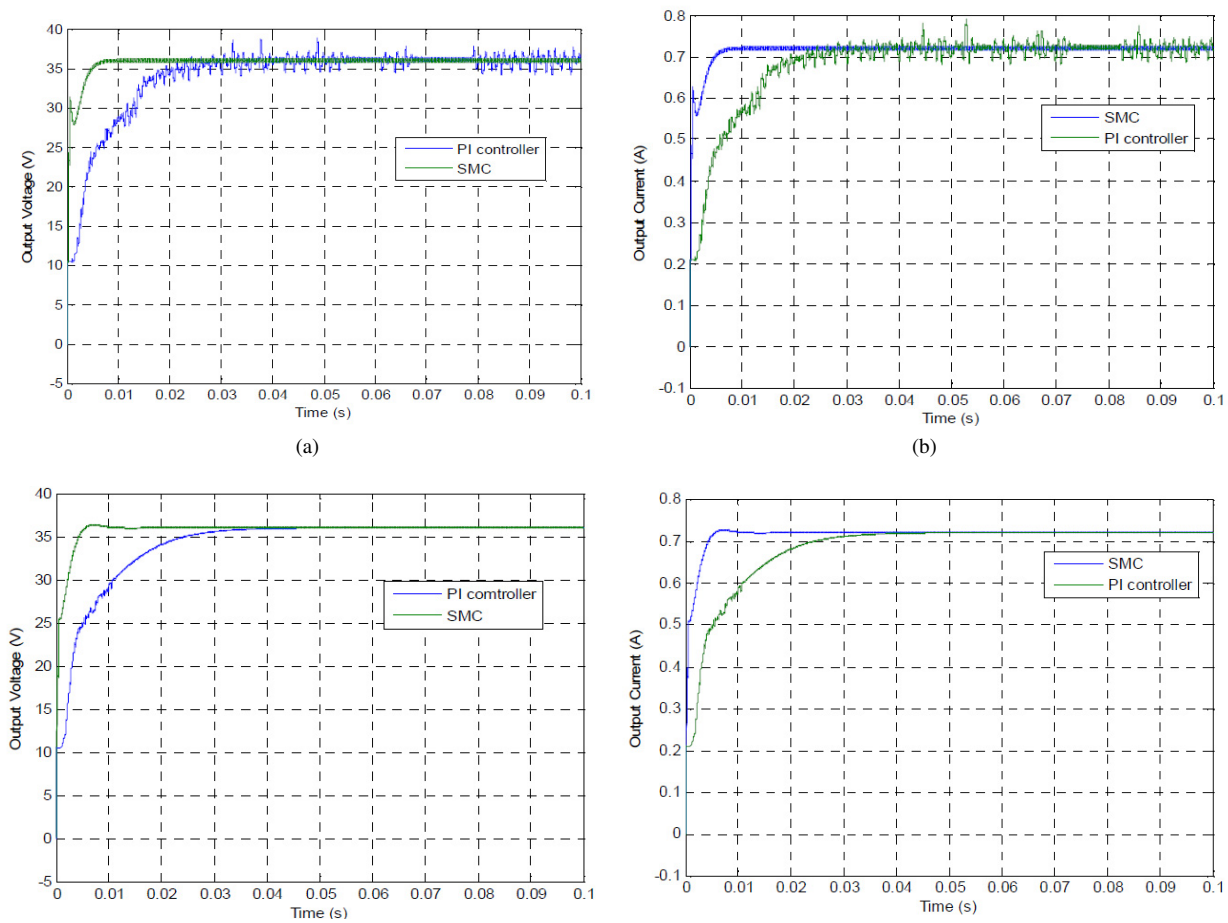
B. *Load variations*

Fig. 17(a) shows the experimental response of the output voltage of the PPOESLLCs using the SMC for a load step change from 50Ω to 60Ω (+20% load variations) at time = 0.05s. It can be seen from the experimental results that the output voltage of the PPOESLLCs using the SMC has a small overshoot of 2V with a quick settling time of 0.01s. Fig. 17(b) shows the experimental response of the output voltage of the PPOESLLCs using the SMC for a load step change from 50Ω to 40Ω (−20% load variations) at time = 0.05s. It can be seen from the experimental results that the output voltage of the PPOESLLCs using the SMC has a small overshoot of 2 V with a quick settling time of 0.01 s.



(a) (b)

Fig. 12. (a) Response of output voltage and inductor current i_{L1} in steady state condition using SMC. (b) Response of output voltage and inductor current i_{L1} in steady state condition using PI controller.



(a) (b)

(c) (d)

Fig. 13. (a) Output voltage of PPOESLLCs when inductor L_1 variation from 100 μH to 500 μH. (b) Output current of PPOESLLCs when inductor L_1 variation from 100 μH to 500 μH. (c) Output voltage of PPOESLLCs when capacitors variation from 30 μF to 100 μF. (d) Output current of PPOESLLCs when capacitors variation from 30 μF to 100 μF.

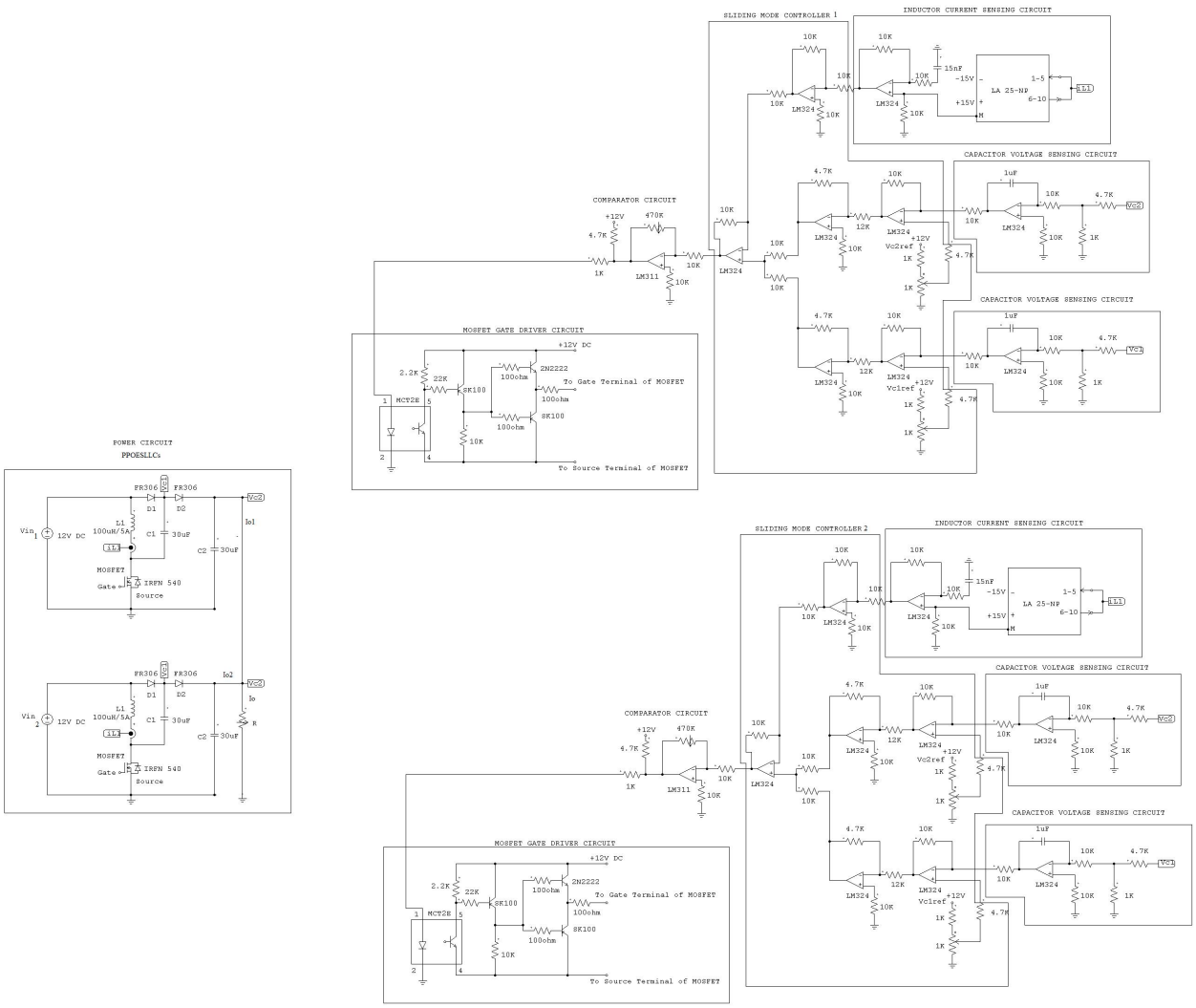


Fig. 14. Laboratory prototype model of PPOESLLCs using SMC in analog platform.

Table IV arranges the experimental and the simulated results of the average output current and voltage of each of the modules and the PPOESLLCs with the developed controllers for various input voltages and load resistances in the start-up region. From this table, it is clearly found that the voltage regulation and the current distributions of each of the modules and the PPOESLLCs using the designed SMC show excellent performance with a tolerance of $\pm 2\%$.

TABLE IV
EXPERIMENTAL AND SIMULATED VOLTAGE/CURRENT PROFILES OF PPOESLLCS FOR VARIOUS INPUT VOLTAGES AND LOAD RESISTANCES WITH NOMINAL INPUT VOLTAGE/LOAD IN START-UP REGION USING SMC

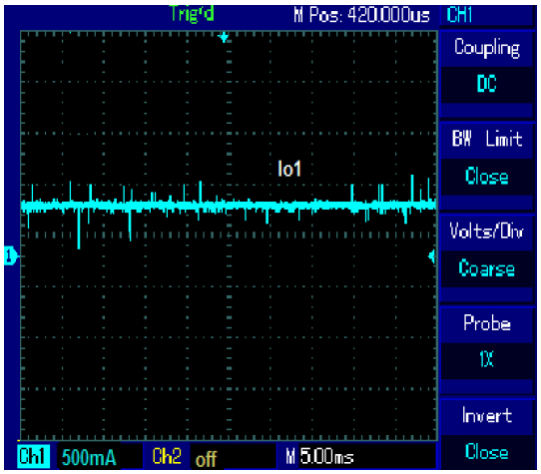
Line Variation 9V- 15V (Start-up region)	Voltage Profiles					
	Experimental (SMC)			Simulation (SMC)		
	V_{o1} (V)	V_{o2} (V)	V_o (V)	V_{o1} (V)	V_{o2} (V)	V_o (V)
	36.15	36.15	36.3	36	36	36
Load Variation 40Ω-60Ω (Start-up region)	Current Profiles					
	Experimental (SMC)			Simulation (SMC)		
	I_1 (A)	I_2 (A)	I_o (A)	I_1 (A)	I_2 (A)	I_o (A)
40Ω	0.461	0.461	0.922	0.45	.45	0.9
50Ω	0.368	0.368	0.736	0.36	.36	.72
60Ω	0.294	0.294	0.588	0.3	0.3	0.6

C. *Steady state region*

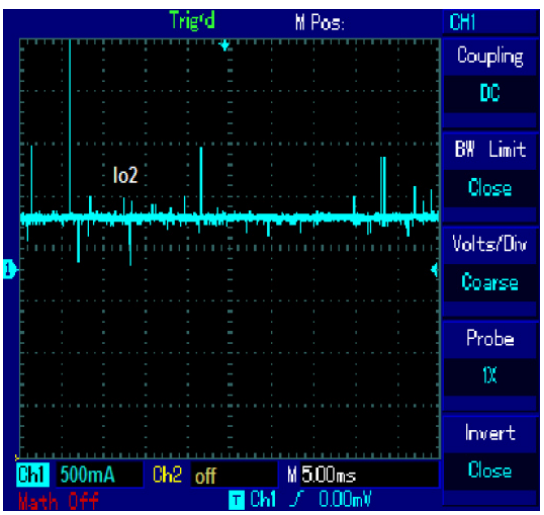
Fig. 18 shows the experimental instantaneous output voltage and the inductor current of the paralleled modules in the steady state region using the SMC. It is evident from the figure that the output voltage ripple is very small, about 0.45 V, and that the peak to peak inductor ripple current is 0.4 A for an average switching frequency 100 kHz closer to the theoretical designed value listed in Table I.

D. *Circuit components variation*

Fig. 19(a) represents the experimental response of the output voltage of the PPOESLLCs using the SMC for an inductor L1 variation from 100μH to 500μH. It can be seen that the change does not influence the PPOESLLC's behavior due

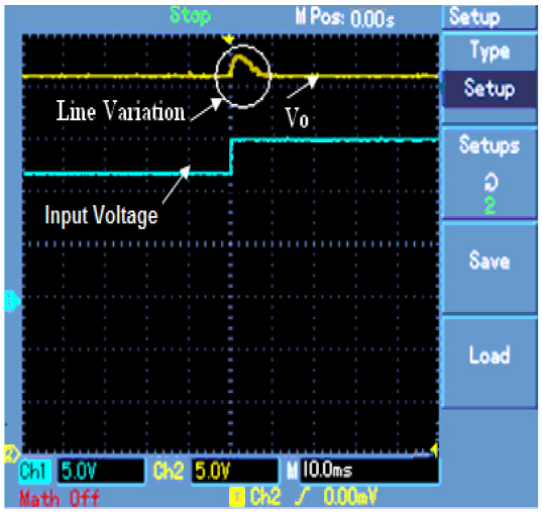


(a)

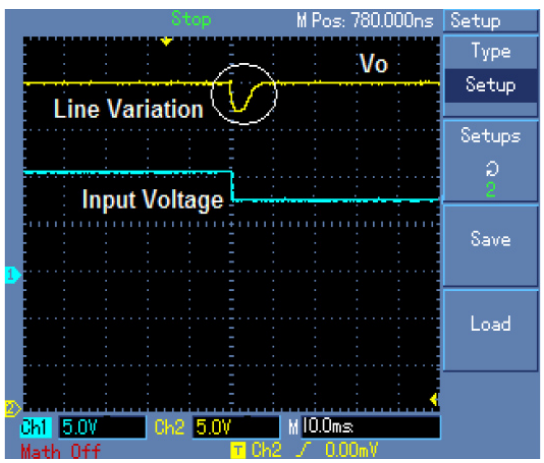


(b)

Fig. 15. (a) Response of average output current of PPOESLLC 1 in startup for $V_{in1} = 12$ V & $V_{in2} = 15$ V [Ch1: 500mA/Div-load current]. (b) Response of average output current of PPOESLLC 2 in startup for $V_{in1} = 12$ V & $V_{in2} = 15$ V [Ch1: 500mA/Div-load current].



(a)



(b)

Fig. 16. (a) Response of output voltage of PPOESSLCs for input step change from 12V to 15 V at time 0.05s with R = 50Ω [Ch1:5V/Div-output voltage and Ch2:5V/Div-input voltage]. (b) Response of output voltage of PPOESSLCs for input step change from 12V to 09 V at time 0.05s with R = 50Ω [Ch1:5V/Div-output voltage and Ch2:5V/Div-input voltage].

to the proficient SMC. An interesting result is illustrated in Fig. 19(b). It shows the experimental response of the output voltage of the PPOESLLCs with the SMC for a variation in the capacitors values from 30μF to 100μF. It can be seen that the proposed SMC is very successful in suppressing the effect of the capacitance variation except for a negligible output voltage ripple and a quick settling time.

In summary, from the Fig. 7(a) to 19(b), it is clearly indicated that the experimental results of the PPOESLLCs using the designed SMC match the simulated results with a tolerance of $\pm 2\%$. Finally, the proposed SMC performed well in all of the working conditions of the PPOESLLCs.

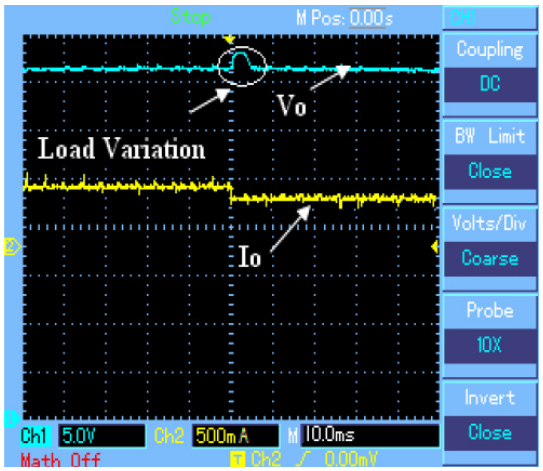
VII. Conclusions

The control loop of a parallel connection of two non-identical POESLLCs is designed successfully using the SMC theory for CDC in CCM. The proposed controller function has been implemented in an analog platform. A major advantage over a linear PI controller lies in the fact that the sliding mode controller is robust to large variations in line, load and parameter variations without modifying the sliding coefficients. Several simulation and experimental results are presented in order to prove the performance of the controller. The system presented is suitable for the real-world commercial applications, viz. an efficient power supply for mobile devices, distributed power supplies, computer power supplies, medical equipment, uninterruptible power supplies, etc.

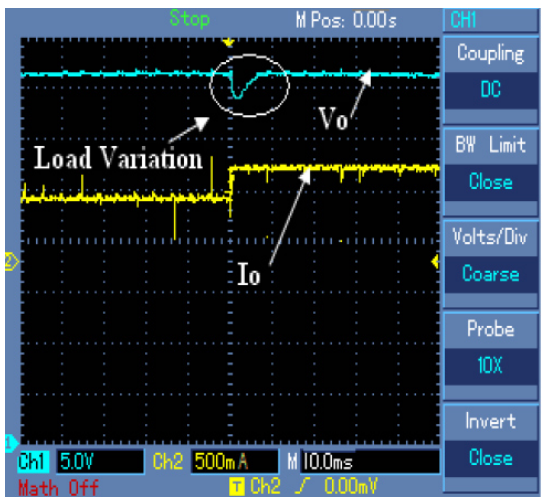
The influence of the controller parameters of the system is also studied. The simulation and experimental results show that the proposed SMC maintains a proper current distribution and a regulated output voltage of the PPOESLLCs in various regions.

Acknowledgment

We sincerely thank the Management, Chairman, Secretary and Principal of the Aalim Muhammed Salegh College of Engineering, Chennai, Tamilnadu, India for their complete support in carrying out this research work.



(a)



(b)

Fig. 17. (a) Response of output voltage of PPOESLLCs when load value takes a step changes from 50 Ω to 60Ω at time 0.05s with V_{in} = 12V [Ch1:5V/Div-output voltage and Ch2:500mA/Div-load current]. (b) Response of output voltage of PPOESLLCs when load value takes a step changes from 50 Ω to 40Ω at time 0.05s with V_{in} = 12 V [Ch1:5V/Div-output voltage and Ch2:500mA/Div-load current].

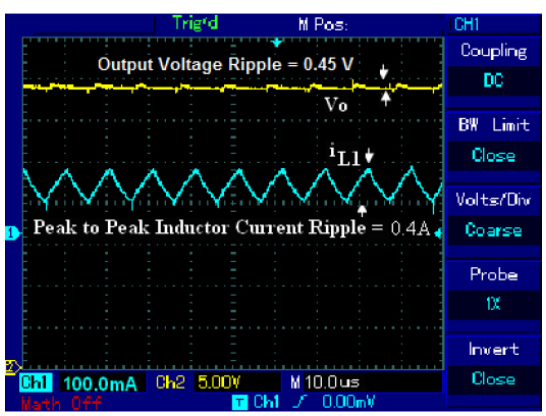
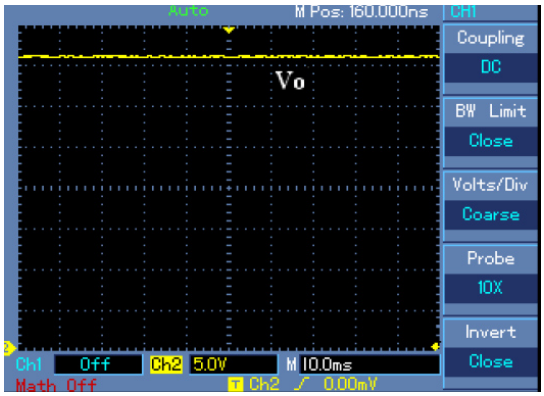
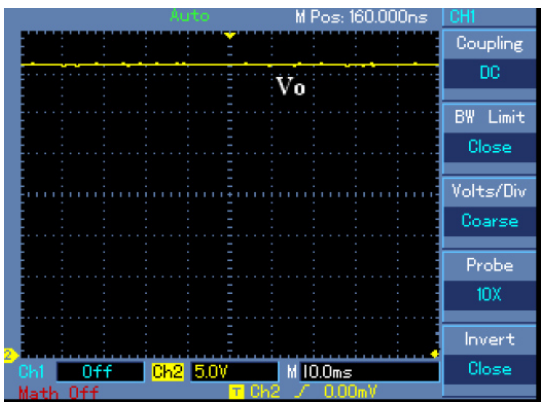


Fig. 18. Response of output voltage and inductor current iL1 in steady state condition using SMC [Ch2:5V/Div - output voltage and Ch1:500mA/Div - inductor current].



(a)



(b)

Fig. 19. (a) Response of output voltage of PPOESLLCs using SMC when inductor variation from 100 μH to 500 μH [Ch2:5V/Div denotes output voltage]. (b) Response of output voltage of PPOESLLCs using SMC when capacitor variation from 30 μF to 100 μF [Ch2:5V/Div denotes output voltage].

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