Design and Implementation of a Robust Predictive Control Scheme for Active Power Filters

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Abstract

This paper presents an effective robust predictive control scheme for the active power filter (APF) using a smith-predictor based current regulator, which show superior features when compared to proportional-integral (PI) controllers in terms of an enhanced closed-loop bandwidth and an improved current tracking accuracy. A moving average filter (MAF) is implemented using a field programmable gate array (FPGA) for signal pre-processing to eliminate the switching ripple contamination. An adaptive linear neural network (ADALINE) is used for individual harmonic estimation to achieve selective compensation purpose. The effectiveness and validity of the devised control algorithm are confirmed by extensive simulation and experimental results.

Key Words: Active power filter (APF), ADALINE, Harmonic contamination, Robust control, Smith-predictor

I. INTRODUCTION

Recently, electrical distribution systems have started to suffer from significant amounts of harmonic contamination due to the proliferation of power-electronic devices, which draw non-sinusoidal currents from distribution networks, causing interference to the sensitive loads connected at the point of common coupling (PCC) [1], [2]. Active power filters (APFs) are considered to be the most effective solution to these power quality problems, and they have been extensively studied in recent literatures [3], [4]. This paper aims to present a robust predictive control algorithm for APFs using a smith-predictor, which has better properties when compared to proportional-integral (PI) current regulators in terms of improvements in the closed-loop bandwidth and better steady-state precision. An adaptive linear neural network (ADALINE) is utilized for individual harmonic estimation, and selective compensation is achieved by using the devised algorithm [5], [6].

This paper is organized as follows. The system description and signal preprocessing technique are presented in Section II. The reference current generation (RCG) scheme using an ADALINE algorithm is presented in Section III. The current loop controller design and stability analysis are discussed in Section IV. The simulation and experimental results are presented in Section V and VI. Conclusions are given in Section VII.

II. DESCRIPTION OF THE ACTIVE POWER FILTER SYSTEM AND SIGNAL PREPROCESSING

Fig. 1 shows a circuit diagram of the shunt APF with LCL-type coupling impedance. To derive the mathematical model of the APF, the following assumptions are considered: (1). The equivalent resistance of the inductors L_g and L_c are neglected; (2). The grid is represented using a Thevenin's equivalent circuit, i.e., the ideal voltage source in series with the effective resistance R_s and inductance L_s; (3). The pulse-width modulation process is within its linear region [5], [6].

The power converter operates at a frequency of 10 kHz, generating remarkable switching ripples and high frequency noises, which degrade the current tracking and cause instability of the whole system. In this paper, a moving average filter (MAF) is implemented in a field programmable gate array (FPGA) for noise rejection and switching ripple elimination. The following discrete transfer function is used for the modeling of the moving average filter (MAF):

$$H_{MAF}(z) = \frac{1}{n} \cdot \frac{1 - z^{-n}}{1 - z^{-1}} \tag{1}$$

where n denotes the number of sampling data used for deriving the average quantities. Fig.2 shows the amplitude frequency property of the MAF under different values of n. It shows that the best attenuation for the switching components and their sideband harmonics can be achieved when $n=8$. Notably, the FPGA is sampling at a constant sampling rate of 80 kHz, the MAF is used to get the average quantity of eight consecutive data using the block by block manipulation scheme, hence the output of the MAF results in a sampling rate of 10kHz when $n=8$. Hence, the DSP board adopts the data with a sampling
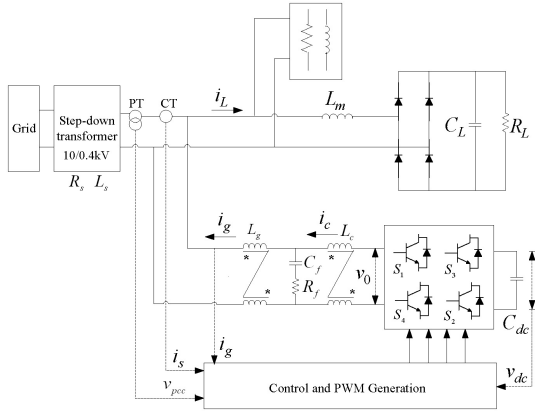
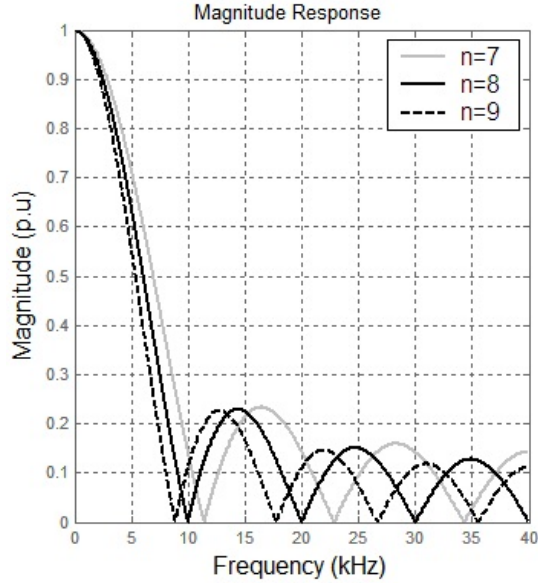Fig. 1. Circuit diagram of the shunt APF with LCL output filter.

Fig. 2. The amplitude-frequency characteristics of the moving average filter (MAF) with different number of samples 'n'.

rate of 10 kHz, which is the same as the PWM control cycle of the power converters.

III. REFERENCE CURRENT GENERATION USING AN ADAPTIVE LINEAR NEURAL NETWORK

This section presents the adaptive signal decomposition scheme using an adaptive linear neural network (ADALINE) [6]. An arbitrary nonlinear load current $Y(t_k)$ can be expressed by the Fourier series expansion as:

$$
\begin{aligned}
Y(t_k) &= \sum_{n=0,1,2,3,\cdots}^{N} A_n \sin(n\omega_0 t_k + \varphi_n) + n(t_k) \\
&= \sum_{n=0,1,2,3,\cdots}^{N} (a_n \sin 2\pi n f_0 t_k + b_n \cos 2\pi n f_0 t_k) + n(t_k)
\end{aligned}
\tag{2}
$$

where A_n and φ_n are correspondingly the amplitude and the phase angle of the nth order harmonic component, and $n(t_k)$ represents higher order components and random noise. Following the definition in [6], the pattern vector X_k and the weight vector W_k of ADALINE can be defined as:

$$
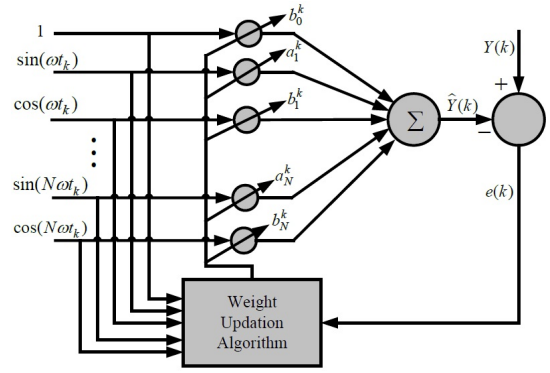\tilde{X}_k = [1, \sin\omega_0 t_k, \cos\omega_0 t_k, \cdots, \sin N\omega_0 t_k, \cos N\omega_0 t_k]^T \tag{3}
$$

Fig. 3. Principle of the adaptive linear neural network.

$$
\tilde{W}_k = [b_0^k, a_1^k, b_1^k, a_2^k, b_2^k, ..., a_N^k, b_N^k]^T. \tag{4}
$$

However, when the ADALINE algorithm is applied for nonlinear load current decomposition, it can be observed from equations (2)-(4) that the fundamental frequency active and reactive components cannot be directly estimated. In order to cope with this shortcoming of the conventional ADALINE [6], the fundamental frequency component of $Y(t_k)$ is rewritten as:

$$
\begin{aligned}
Y_1(t_k) &= A_1 \sin(\omega_0 t_k + \varphi_1) \\
&= A_1 \sin(\omega_0 t_k + \varphi_{PLL} + \varphi_1 - \varphi_{PLL}) \\
&= A_1 \sin(\omega_0 t_k + \varphi_{PLL})\cos(\varphi_1 - \varphi_{PLL}) \\
&\quad + A_1 \cos(\omega_0 t_k + \varphi_{PLL})\sin(\varphi_1 - \varphi_{PLL})
\end{aligned}
\tag{5}
$$

where φ_{PLL} represents the initial phase angle of the fundamental frequency grid voltage, and $\omega_0 t_k + \varphi_{PLL}$ represents the phase angle of the fundamental frequency grid voltage, which are obtained from the phase-locked-loop (PLL) [5], [6]. Referring to equation (5), the weight vector can be redefined for the fundamental component load current $Y_1(t_k)$, as follows:

$$
a_1^k = A_1 \cos(\varphi_1 - \varphi_{PLL}) \tag{6}
$$

$$
b_1^k = A_1 \sin(\varphi_1 - \varphi_{PLL}) \tag{7}
$$

Therefore, equations (3)-(4) can be rewritten as:

$$
\begin{aligned}
X_k = [1, \sin(\omega_0 t_k + \varphi_{PLL}), \cos(\omega_0 t_k + \varphi_{PLL}), \\
\cdots, \sin N\omega_0 t_k, \cos N\omega_0 t_k]^T
\end{aligned}
\tag{8}
$$

$$
W_k = [b_0^k, a_1^k, b_1^k, a_2^k, b_2^k, ..., a_N^k, b_N^k]^T. \tag{9}
$$

The fundamental grid voltage is denoted by $v_1 = V_1 \sin(\omega_0 t_k + \varphi_{PLL})$, and its phase angle is extracted by the PLL and utilized as the input vector for the ADALINE, as indicated by equation (8). The aforementioned ADALINE algorithm is utilized for reference current generation for the current-loop controller of the APF.

IV. CURRENT-LOOP CONTROLLER DESIGN AND STABILITY ANALYSIS

Fig. 4 shows a simplified circuit diagram of the LCL-type APF. The voltage source inverter (VSI) is denoted by the controlled voltage source U_0, the nonlinear load is connected at the point of common coupling, represented by the current disturbance. The grid inductance is denoted by L_s, and the
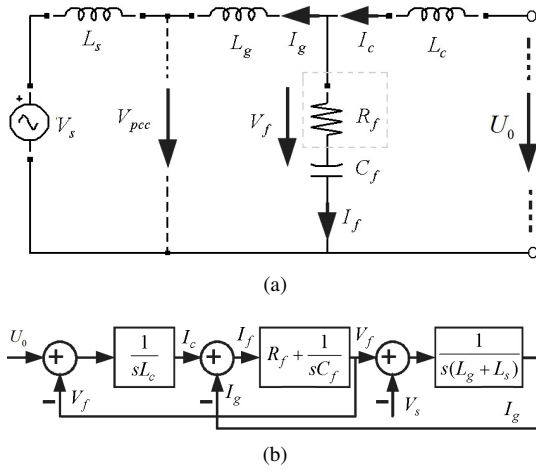
(a)

(b)

Fig. 4. The simplified circuit diagram of the APF. (a) Circuit diagram. (b) Block diagram.

transfer function from the inverter output U_0 to I_g is derived as:

$$\frac{I_g(s)}{U_0(s)} = \frac{sRC+1}{L_c(L_g+L_s)C_f \cdot s \cdot [s^2+2\xi_r\omega_r+\omega_r^2]} \quad (10)$$

where

$$\omega_r = \sqrt{\frac{L_c+L_g+L_s}{L_c(L_g+L_s)C_f}} \quad \xi_r = \frac{1}{2}R_f\sqrt{\frac{(L_c+L_g+L_s)C_f}{L_c(L_g+L_s)}}.$$

To analyze the performance of the current controller, a discrete domain model of the plant is derived, where the effect of the grid inductance L_s is neglected for the sake of brevity. From the circuit diagram, the transfer function from the inverter output to the output current can be derived as:

$$G_p(s) = \frac{Z_{RC}}{Z_{L_c}\left(Z_{L_g}+Z_{RC}\right)+Z_{L_g}Z_{RC}} \quad (11)$$

where the equivalent impedance of the RC brunch is denoted as:

$$Z_{RC} = R_f + \frac{1}{sC_f} \quad (12)$$

and the impedance of L_c and L_g are denoted by:

$$Z_{L_c} = sL_c \quad (13)$$

$$Z_{L_g} = sL_g \quad (14)$$

Substituting Eqs.(12)-(14) into Eq.(11), results in:

$$G_p(s) = \frac{1+R_fC_fs}{L_gL_cC_fs^3+(L_g+L_c)R_fC_fs^2+(L_g+L_c)s}. \quad (15)$$

Neglecting the effect of the damping resistance, yields:

$$G_p(s) = \frac{1}{L_gL_cC_fs^3+(L_g+L_c)s}. \quad (16)$$

Since the control algorithms are implemented using DSP and FPGA platforms, the plant model of the APF should be converted into a discrete form, as shown in Fig.5. It consists of three blocks: (1) the digital/analog converter, i.e., the holder, denoted as $H(s)$, (2) the plant model $G_p(s)$ and (3) the control delay T_d. Notably, the delay time T_d is associated with the hardware, which includes the sampling delay and the delay effect of the master/slave DSP communication. Generally,
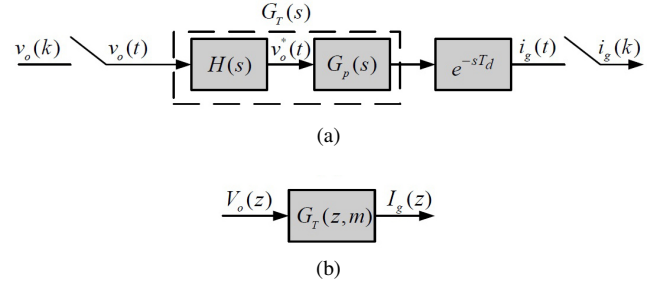

(a)

(b)

Fig. 5. The z-domain model of the continuous model G_p(s) with equivalent control delay T_d.

$T_d=(1\sim2)T_s$, to simplify the derivations, it is assumed that $T_d=mT_s$ $(1<m<2)$. Assuming that $g(t)$ is the impulse response of the plant $G_p(s)$, after a sampling $g(t)$ with an interval T_s, $Z\{G_p(s)\}$, i.e., $Z\{L^{-1}[G_p(s)](kT_s)\}$ is obtained, where L^{-1} denotes the inverse Laplace transformation. Hence, the discrete model of the continuous system in Fig.5(a) is denoted by:

$$Z\left\{\underbrace{H(s)G_p(s)e^{-smT_s}}_{G_T(s)}\right\} \quad (17)$$
$$= \sum_{k=0}^{\infty} z^{-k}g_T(kT_s-T_d) = Z_m\{G_T(s)\} = G_T(z,m)$$

where g_T represents the impulse response of $G_T(s)$, and $G_T(z, m)$ represents the discrete transfer function from the discrete input $V_0(z)$ to the discrete output $I_g(z)$ [see Fig.5(b)]. And $H(s)$ is assumed to be a zero-order-hold (ZOH) denoted as:

$$H(s) = \frac{1-e^{-sT_s}}{s} \quad (18)$$

Substituting Eq.(18) into Eq.(17), results in:

$$G_T(z,m) = Z\left\{\underbrace{\frac{1-e^{-sT_s}}{s}}_{H(s)}G_p(s)e^{-smT_s}\right\} \quad (19)$$
$$= \frac{z-1}{z}Z\left\{\frac{G_p(s)}{s}e^{-smT_s}\right\} = \frac{z-1}{z}Z_m\left\{\frac{G_p(s)}{s}\right\}$$

Moreover, if $H(s)$ is a first-order hold (FOH), then the output can be represented as a piece-wise function:

$$v_o^*(t) = \frac{v_o(k+1)-v_o(k)}{T_s}. \quad (20)$$

The output $v_o^*(t)$ is assumed to be constant during one sampling interval T_s. Therefore, $I_g(z)$ can be rewritten as:

$$I_g(z) = Z\left\{\underbrace{\frac{1-e^{-sT_s}}{s}}_{H(s)}\frac{G_p(s)}{s}e^{-smT_s}\right\}V_0^*(z) \quad (21)$$
$$= \underbrace{\frac{(z-1)^2}{zT_s}Z_m\left\{\frac{G_p(s)}{s^2}\right\}}_{Z_T(z,m)}V_o(z).$$

To simplify the analysis, a FOH is adopted herein, thus the discrete model can be derived as:

$$G_T(z,m) = \frac{1}{L_g+L_c}\left\{\frac{1}{z-1}-\frac{1}{\omega_r}\cdot\frac{(z-1)\sin(\omega_rT_s)}{z^2-2z\cos(\omega_rT_s)+1}\right\}z^{-m} \quad (22)$$
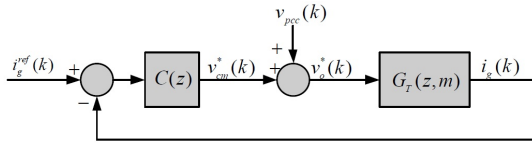
Fig. 6. The closed-loop block diagram of the current loop in the discrete domain.

Fig. 7. The closed-loop root locus of the current loop using PI controller.

where $\omega_r = \sqrt{(L_g + L_c)/(L_g L_c C_f)}$.

From this equation, the effects of the controller structure and the control delay on the closed-loop bandwidth and the dynamic property of the current loop can be analyzed in the forthcoming sections.

Fig. 6 shows a closed-loop block diagram of the current loop controller in the discrete domain, which is based on the kth control cycle. The input signal is the reference signal of the APF at the kth control cycle, which is derived from the ADALINE identification algorithm. $i_g(k)$ denotes the sampling current at the present control cycle, and $C(z)$ denotes the current controller. The output of the current controller is added to the grid voltage $v_{pcc}(k)$ to synthesize the inverter output voltage, which is applied to the plant model $G_T(z, m)$ to synthesize the inverter output current.

Next, the effects of a proportional-integral (PI) controller on the current loop performance is investigated. To enhance both the high frequency characteristics and the bandwidth of the current loop, a smith-predictor based predictive controller is proposed.

A. Proportional-Integral (PI) Controller

The discrete transfer function of the proportional-integral (PI) controller $C(z)$ is denoted as:

$$C(z) = k_p + \frac{k_i T_s}{z - 1} \tag{23}$$

where k_p and k_i denote the proportional and integral gains, respectively. The open loop transfer function of the current tracking controller is derived as:

$$H_{open}(z) = C(z)G_T(z,m)$$
$$= (k_p + \frac{k_i T_s}{z-1})\frac{1}{L_g + L_c}\left\{ \frac{1}{z-1} - \frac{1}{\omega_r} \cdot \frac{(z-1)\sin(\omega_r T_s)}{z^2 - 2z\cos(\omega_r T_s)+1} \right\}z^{-m}. \tag{24}$$

A tradeoff between the bandwidth and the tracking precision is achieved when selecting $k_p=1$ and $k_i=20$. Fig.7 shows the closed-loop root locus of the current controller using a proportional-integral (PI) regulator. A gain margin of 8.61 dB and a phase margin of 61.1 degrees are obtained, with a closed-loop bandwidth of 1.34 kHz. It shows that the P controller and the PI controller are similar in terms of performance.

B. Deadbeat Controller with Smith Prediction

From Eq.(22) and by neglecting the control delay, the closed-loop transfer function can be derived as:

$$H(z) = \frac{C(z)G_T(z,0)}{1 + C(z)G_T(z,0)}. \tag{25}$$

Let $G_T(z,0)=G(z)$ along with a control delay of m cycles. Then the plant model is derived as $G_T(z, m)=G(z)z^{-m}$. The
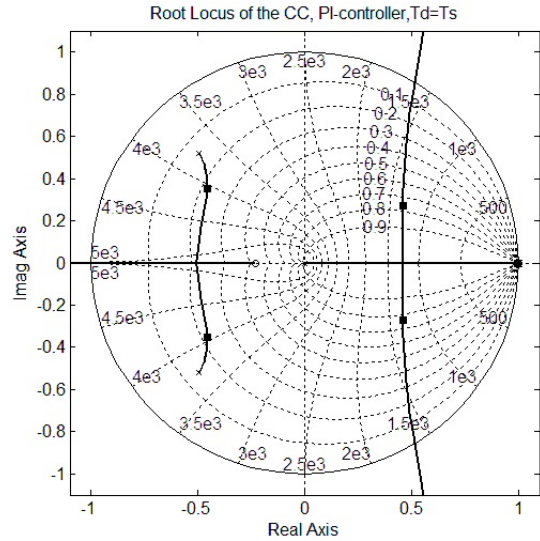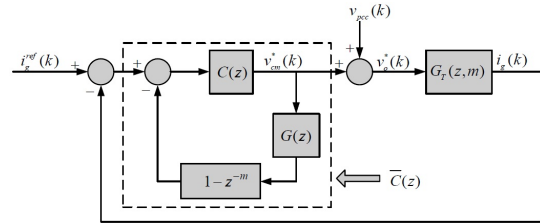

Fig. 8. The smith-predictor based current controller for the plant with control delay.

purpose of the smith predictor is to satisfy the following equation:

$$\overline{H}(z) = H(z)z^{-m} \tag{26}$$

where $\overline{H}(z)$ denotes the plant model with an m beat control delay. Assuming that the transfer function of the current controller with the smith predictor is denoted by $\overline{C}(z)$, the closed-loop transfer function $\overline{H}(z)$ can be derived as:

$$\overline{H}(z) = \frac{\overline{C}(z)G(z)z^{-m}}{1 + \overline{C}(z)G(z)z^{-m}} \tag{27}$$

From Eqs.(25)-(27), the following is obtained:

$$\frac{\overline{C}(z)G(z)z^{-m}}{1 + \overline{C}(z)G(z)z^{-m}} = \frac{C(z)G(z)}{1 + C(z)G(z)} \cdot z^{-m} \tag{28}$$

After the manipulation of Eq.(28), the following is obtained:

$$\overline{C}(z) = \frac{C(z)}{1 + G(z)C(z)(1 - z^{-m})}. \tag{29}$$

It can be seen from Eq.(29) that the new controller is composed of the previous controller $C(z)$ with a feedback loop $G(z)(1-z^{-m})$. Hence, the diagram of the current loop with the smith predictor is derived, as shown in Fig.8.

Since the order of the plant model $G(z)$ is high, the one-step-ahead prediction using $G(z)(1-z^{-m})$ results in a heavy computational load. Hence, the model $G(z)$ is replaced using a lower order equivalent model:

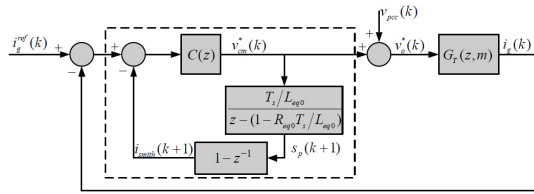$$\tilde{G}(s) = \frac{1}{L_{eq0}s + R_{eq0}}, L_{eq0} = L_{g0} + L_{c0} \tag{30}$$

Fig. 9. The smith-predictor based controller with one beat prediction for the plant.

where L_{g0} and L_{c0} denote the nominal parameters of the inductance, and the actual inductances are $L_g=L_{g0}+\Delta L_g$ and $L_c=L_{c0}+\Delta L_c$. Furthermore, ΔL_g and ΔL_c denote the parameter deviations and R_{eq0} denotes the equivalent series resistance. The discrete model is derived by using the zero-order-hold (ZOH):

$$\tilde{G}(z) = (1-z^{-1})Z\left[\frac{\tilde{G}(s)}{s}\right]$$
$$= \frac{1}{R_{eq0}}(1-z^{-1})\left(\frac{z}{z-1} - \frac{z}{z-e^{-R_{eq0}T_s/L_{eq0}}}\right) \quad (31)$$

The exponential term is approximated as:

$$e^{-R_{eq0}T_s/L_{eq0}} \approx 1 - R_{eq0}T_s/L_{eq0} \quad (32)$$

Substituting Eq.(32) into Eq.(31), yields:

$$\tilde{G}(z) = \frac{T_s/L_{eq0}}{z-(1-R_{eq0}T_s/L_{eq0})}. \quad (33)$$

From Eq.(29) and Eq.(33), the equivalent diagram can be derived, as shown in Fig.9. Only one step-ahead prediction is considered in the devised smith-predictor. The derived signal, after the approximated model, is denoted as $s_p(k+1)$ and the predicted current is denoted as $i_{smith}(k+1)$. From Fig.9, the predicted signal $s_p(k+1)$ can be derived as:

$$s_p(k+1) = v_{cm}^*(k)\frac{T_s/L_{eq0}}{z-(1-R_{eq0}T_s/L_{eq0})} \quad (34)$$

Hence, the relation between $s_p(k+1)$ and $s_p(k)$ is derived as:

$$s_p(k+1) = (1-\frac{R_{eq0}T_s}{L_{eq0}})s_p(k) + \frac{T_s}{L_{eq0}}v_{cm}^*(k-1) \quad (35)$$

Therefore, the output of the smith-predictor is derived as:

$$i_{smith}(k+1) = (1-z^{-1})s_p(k+1)$$
$$= -\frac{R_{eq0}T_s}{L_{eq0}}s_p(k) + \frac{T_s}{L_{eq0}}v_{cm}^*(k-1) \quad (36)$$

Thus, the transfer function of the current loop is derived as:

$$\overline{C}(z) = \frac{C(z)}{1+(1-z^{-1})\tilde{G}(z)C(z)} \quad (37)$$

where $C(z)$ denotes the deadbeat controller. Substituting Eq.(33) into Eq.(37), results in:

$$\overline{C}(z) = \frac{k_p}{1+k_p(1-z^{-1})\frac{T_s/L_{eq0}}{z-(1-R_{eq0}T_s/L_{eq0})}} \quad (38)$$

Hence, the open-loop transfer function can be derived as:

$$H_{open}(z) = \overline{C}(z)G_T(z,m)$$
$$= \frac{k_pz^2-k_p(1-R_{eq0}T_s/L_{eq0})z}{z^2+(k_pT_s/L_{eq0}+R_{eq0}T_s/L_{eq0}-1)z-k_pT_s/L_{eq0}} \quad (39)$$
$$\times\frac{1}{L_{eq}}\left\{\frac{1}{z-1} - \frac{1}{\omega_r}\cdot\frac{(z-1)\sin(\omega_rT_s)}{z^2-2z\cos(\omega_rT_s)+1}\right\}z^{-m}.$$
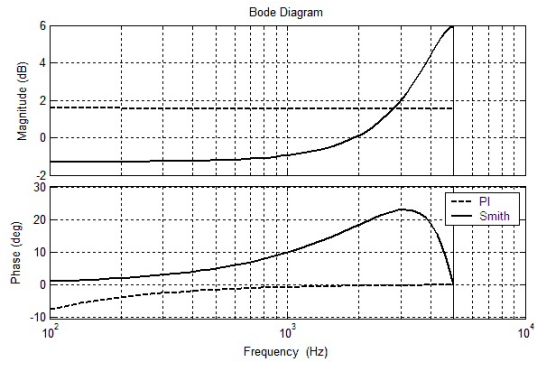

Fig. 10. The frequency-domain characteristic of the PI controller and the smith controller.

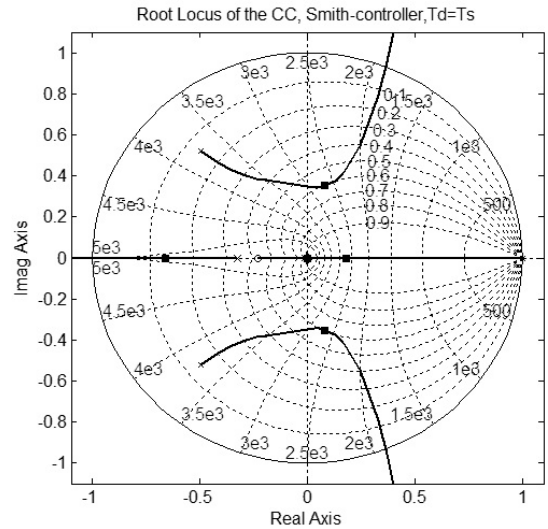Fig. 11. The closed-loop root locus of current loop using smith-predictor based controller.

Neglecting the resistance R_{eq}, and letting $\rho=T_s/L_{eq0}$, the open-loop transfer function with a one beat control delay can be derived as:

$$H_{open}(z) = \frac{k_p}{(z+\rho k_p)L_{eq}}\left\{\frac{1}{z-1} - \frac{1}{\omega_r}\cdot\frac{(z-1)\sin(\omega_rT_s)}{z^2-2z\cos(\omega_rT_s)+1}\right\} \quad (40)$$

Moreover, the closed-loop transfer function is derived as:

$$H_{close}(z) = \frac{\overline{C}(z)G_T(z,m)}{1+\overline{C}(z)G_T(z,m)}. \quad (41)$$

Fig. 10 shows the frequency-domain characteristic of the PI controller ($k_p=1.2$, $k_i=100$) and the smith controller. It shows that the PI controller reduces to a proportional controller at higher frequencies and that the smith controller shows a leading phase at higher frequencies. The leading phase of the smith controller is helpful for compensating the phase delay of the plant model at higher frequencies, thus enhancing the stability of the system.

Fig. 11 shows the closed-loop root locus of the current loop using the smith-predictor based controller. The dominant poles are shifted toward the center of the unit circle, thus the dynamic performance of the system is enhanced. A bandwidth of 2.6 kHz is obtained, with a gain margin of 6.57 dB and a phase margin of 60.4 degrees. The improved bandwidth is
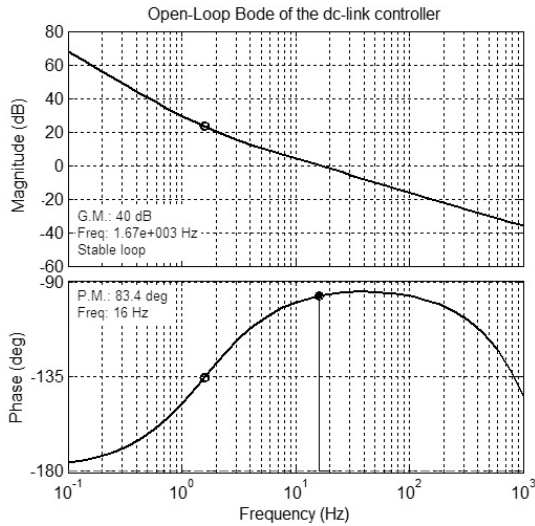
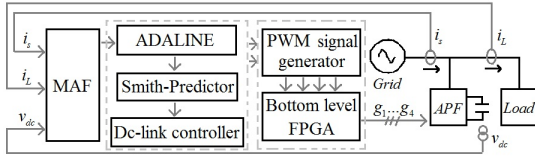Fig. 12. The open-loop bode diagram of the dc voltage loop.

Fig. 13. The complete control diagram of the whole system.

crucial to improving the compensation performance of the LCL-APF at higher harmonic frequencies.

V. DC-LINK CONTROLLER DESIGN

The dc voltage controller is used to regulate the active power balance between the APF and the grid. As discussed in [1], the open loop transfer function of the dc-link voltage controller is:

$$G_{open,dc}(z) = G_{c,dc}(z) \cdot G_{plant,dc}(z) \cdot G_{PWM,dc}(z) \qquad (42)$$

where $G_{c,dc}(z)$ denotes the controller, $G_{plant,dc}(z)$ denotes the discrete domain model of the inverter dc-link, and $G_{PWM,dc}(z)$ denotes the transfer function of the PWM process, normally approximated by a one cycle delay z^{-1}. The transfer functions $G_{c,dc}(z)$ and $G_{plant,dc}(z)$ are denoted as [1], [5], [6]:

$$G_{c,dc}(z) = k_{p,dc}(1 + \frac{1}{\tau_{dc}} \cdot \frac{T_s}{z-1}) \qquad (43)$$

$$G_{plant,dc}(z) = \frac{T_s}{C_{dc}} \cdot \frac{1}{z-1} \qquad (44)$$

Hence, the open-loop transfer function is derived as:

$$G_{open,dc}(z) = \frac{k_{p,dc} \cdot T_s}{C_{dc}} \cdot \frac{z - (1 - T_s/\tau_{dc})}{(z-1)^2 z}. \qquad (45)$$

To avoid interaction between the dc-link controller and the current loop controller, the bandwidth of the voltage loop must be much less than that of the current loop. The bandwidth is designed to be less than 50Hz and the overshoot less than 10%, as shown in Fig. 12. A gain margin of 40 dB and a phase margin of 83.4 degrees is obtained when $k_{p,dc}$=2 and τ_{dc}=1.

Fig. 13 shows a complete diagram of the whole system and the signal flow is also depicted. Notably, the sampling signals
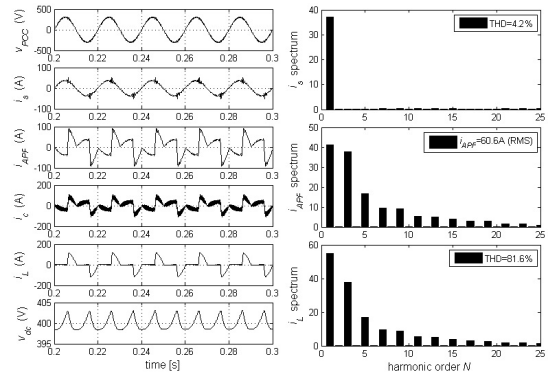

Fig. 14. Steady state performance of the LCL-APF based on the devised smith-predictor based control algorithm.

are preprocessed by the MAF using the FPGA to filter out both the sampling noise and the random noise. These signals are sent to the main DSP for the main routine, which includes the ADALINE algorithm for harmonic decomposition, the reference signal generation, the smith-predictor based current controller and the dc-link voltage controller. The obtained modulation signals are sent to the bottom FPGA controller to synthesize the IGBT gating signals for the power converter [see Fig. 13].

VI. SIMULATION RESULTS

To verify the effectiveness of the devised control algorithm, the single-phase APF is simulated using Matlab/Simulink. A thyristor rectifier load is used as harmonic source, the grid voltage is v_{PCC}=220V, the grid impedance R_s=50mΩ, the grid inductance L_s=20μH, and L_g=50μH, L_c=250μH, R_f=0.5Ω, and C_f=20μF. The firing angle of the thyristor is α=110°, and the dc-side resistance of the rectifier load is 2.2Ω, with a sudden increase of 2.2Ω to test the transient response of the system.

Fig. 14 shows the waveforms of the gird voltage v_{pcc}, the grid side current after compensation i_s, the APF compensating current i_{APF}, the converter side current i_C, the load current i_L and the dc-link voltage v_{dc}. The FFT spectrum of the grid current i_s, the APF compensating current i_{APF}, the load current i_L and their total harmonic distortion (THD) are also shown. Fig. 14 shows that the THD of load current is 81.6% and a sinusoidal waveform is obtained from the grid current, with a THD of 4.2%.

Fig. 15 shows the dynamic response of the APF using the devised control algorithm. The weights updating process of the ADALINE are also provided, where the parameters a_1, b_1 and a_3, b_3 denotes the coefficients of the fundamental component and the third harmonic component, and i_{error} denotes the estimation error of the ADALINE. It shows that the ADALINE algorithm is a tradeoff between the estimation accuracy and the dynamic response. The deficiency of the conventional low-pass-filter based approach is avoided. The transient APF current and the inverter dc-link voltage are also minimized by using the ADALINE algorithm [1], [6].

VII. EXPERIMENTAL RESULTS

To validate the devised control algorithm for the APF, a prototype system was built in the laboratory using three
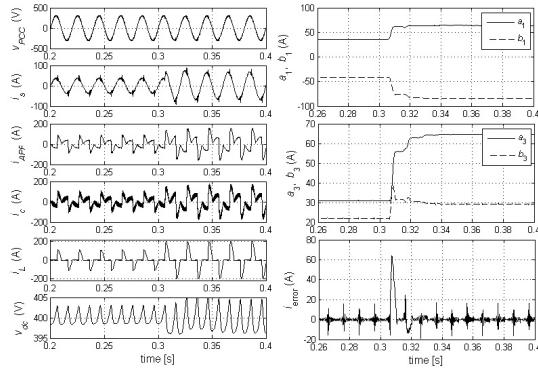
Fig. 15. Transient response of the LCL-APF based on the devised smith-predictor based control algorithm.

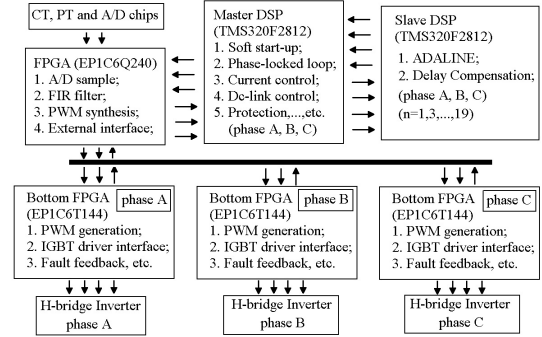Fig. 16. The photo of the LCL-APF experimental setup.

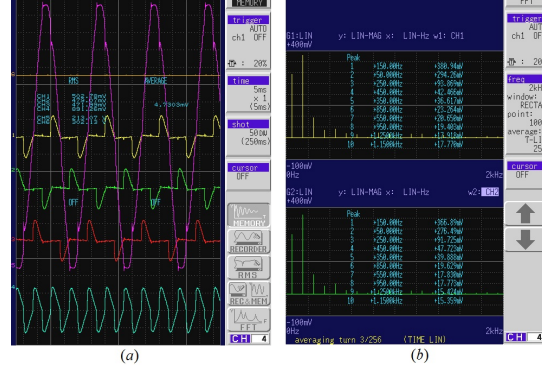Fig. 17. The architecture of the main controller platform.

Fig. 18. Experimental results of the load currents and the FFT spectrum. (a) The load currents i_{La}, i_{Lb}, i_{Lc}, i_{LN} (ch-1 to ch-4: 80A/div), and $v_{PCC,A}$ (ch-5: 40V/div). (b) FFT spectrum of i_{La}, i_{Lb}.

single-phase VSI topologies. Fig. 16 shows a photo of the experimental setup. Fig. 17 shows the architecture of the main controller platform. Three digital signal processors (DSPs) from Texas Instrument (TMS3202812) are used. The main controller is responsible for the main program, the soft-start routine, and the protection routine. The second DSP is used for the ADALINE based harmonic estimation algorithm. The third DSP is used for the man/machine interface, i.e., the parameter display and touch board. A field programmable gate array (FPGA) from Altera (EP1C6Q240C8) is used to receive the gating signals from the main controller and to generate PWM signals for the IGBTs.

The three single-phase thyristor rectifier loads are utilized as a harmonic source, and the parameters of the experimental set up are consistent with the simulation. Fig. 18(a) shows the test results of the load currents and the neutral wire current, the grid voltage and the dc-link voltage in phase 'a'. Fig. 18(b) shows the FFT spectrum of the load currents in phases 'a' and 'b'. The THD of the load current in phase 'a' is about 135% when the firing angle of the thyristor load is 110 degree, which is dominated by the odd order harmonics.

Fig. 19 shows the results of the grid currents, the grid voltage and the dc-link voltage in phase 'a'. The odd order harmonic components up to 19th order are estimated using the ADALINE algorithm, and the 3rd, 5th, 7th, 11th and 13th order components are selected to be compensated by the APF. The thyristor rectifier results in a high *di/dt* ratio at the conduction instant, which causes a significant voltage distortion due to the high grid impedance in the laboratory environment. It shows that sinusoidal waveforms are obtained from the grid side, with

a total harmonic distortion of about 4.8% and that the neural wire current is also minimized.

Fig. 20 shows the waveforms of the system dynamic response. In Fig. 20(a), the APF first works in the reactive compensation mode, and the thyristor load is abruptly turned on. Fig. 20(b) shows the case when the APF is suddenly turned off. It can be observed in Fig. 20 that the system is always stable during these dynamic disturbances, which verifies the effectiveness of the proposed control algorithms.

VIII. Conclusions

This paper proposes a robust control algorithm for active power filters using a smith-predictor based current regulator, which has a higher bandwidth when compared with proportional integral controllers. An adaptive linear neural network is used for individual harmonic estimation, and selective harmonic compensation is achieved. The simulation results are presented, and a perfect dynamic response is achieved owing to the ADALINE estimation algorithm. A laboratory prototype system is also built for verification. By selecting the four dominant harmonics to be compensated, the sinusoidal waveforms in the grid currents are achieved, which verifies the effectiveness of the devised control algorithm. By selecting the higher order harmonics to be compensated, the grid distortion can be further reduced, but as a tradeoff the computational load in the DSP controller is increased.
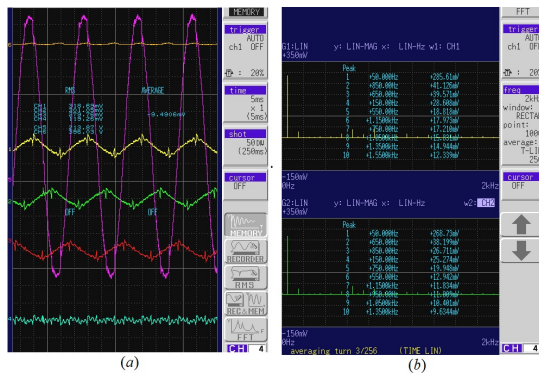
Fig. 19. Experimental results of the grid currents and the FFT spectrum. (a) The grid currents i_{sa}, i_{sb}, i_{sc}, i_{sN} (ch-1 to ch-4: 80A/div), and $v_{PCC,A}$ (ch-5: 40V/div). (b) FFT spectrum of i_{sa}, i_{sb}.
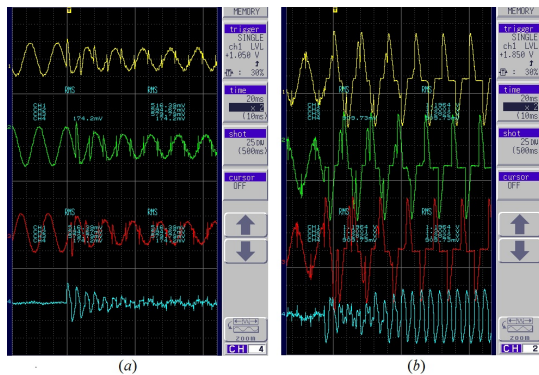

Fig. 20. The dynamic response of the APF.(a) The thyristor load is turned on abruptly. (b) The APF is suddenly turned off.

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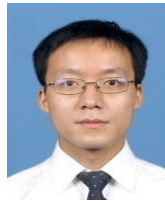
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