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Soft Switching Three Phase Inverter with Two Auxiliary Switches

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Abstract

In this paper, a new three phase soft switching inverter is presented. All of the semiconductor elements of this converter are soft switched. Employing only two auxiliary switches as DC-link switches and a simple control circuit are the advantages of the proposed inverter. The analytical equations and operating modes of the presented inverter are explained in details. The design considerations are presented and the experimental results verify the theoretical analysis.

Key Words: Quasi-resonant, Soft switching, Three phase inverter, Zero voltage switching (ZVS)

I. Introduction

Inverters have many applications in power electronics, such as AC motor drives, active power filters, and uninterruptible power supplies. To increase the efficiency of converters and to decrease electromagnetic interference, it is necessary to use soft switching techniques [1]–[3]. Among these techniques, quasi-resonant dc-link inverters have the advantages of zero voltage switching (ZVS) for the main switches, a low number of the auxiliary switches and low voltage stress on the main switches.

One of the main objectives of quasi-resonant dc-link inverters is achieving soft switching conditions with a minimum number of auxiliary circuit elements. The auxiliary circuit in [4] has three auxiliary switches and the auxiliary circuits in [5]–[9] have two auxiliary switches. Reducing the number of auxiliary switches simplifies the control circuit and decreases the inverter cost. Therefore, it is worth offering to provide soft switching inverters with one auxiliary switch [10], [11]. In [10], the number of auxiliary switches is reduced at the cost of employing extra elements including three diodes, coupled inductors and a resonant capacitor. The auxiliary circuit presented in [11] reduced the number of extra elements at the expense of adding a capacitive voltage divider at the inverter input and losing control over the zero voltage interval of the inverter DC-link. The control of the DC-link zero voltage interval, is used in some switching methods such as space vector modulation. The soft switching inverters presented in [12] and [13] have no auxiliary switch and the soft switching condition is achieved by a DC-link switch. The drawback of these inverters is that their DC-link switch is turned off under an almost zero voltage condition due to the existence of a leakage inductor in series with the DC-link switch, which causes a voltage spike across the switch at the turn off instant. To reduce this voltage spike, a passive turn off snubber must be used, which add extra losses to the circuit. Soft switching inverters usually do not have a passive snubber. The soft switching inverter presented in [14], in addition to having an auxiliary switch, requires such a snubber for the auxiliary switch.

A new soft switching inverter with two DC-link switches is proposed in this paper. These switches are turned on under the zero voltage zero current switching (ZVZCS) condition and off under the ZVS condition. Since the sources of the DC-link switches are connected together, and they are complimentary switched, their gate drive circuits become simple. The proposed inverter has a lower number of extra elements in comparison with previous converters while all of the switches are fully soft switched. Furthermore, the DC-link switches share the inverter current which considerably reduces the switches current stress.

The proposed inverter is introduced and its operating modes are discussed in section II. The design considerations of the proposed inverter are provided in section III and the experimental results of a 250W, 20kHz prototype inverter are presented in section IV. The presented experimental results confirm the theoretical analysis.

II. Proposed Inverter Description and Operation

The circuit configuration of the proposed soft switching inverter is illustrated in Fig. 1. The main inverter is composed of the switches S_1 to S_6. The auxiliary circuit consists of

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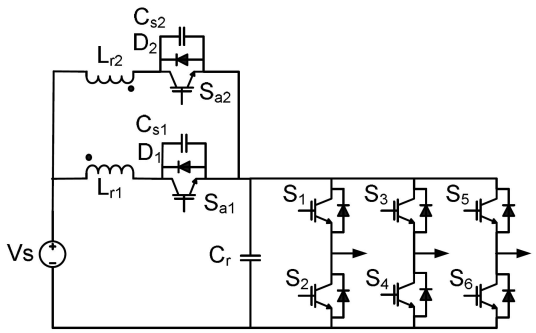

Fig. 1. Proposed Inverter.

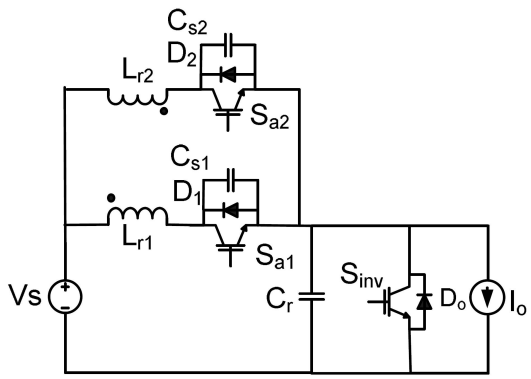

Fig. 2. Equivalent circuit of the proposed Inverter.

the DC-link switches S_{a1} and S_{a2}, the coupled inductors L_{r1} and L_{r2}, and the capacitors C_r, C_{s1} and C_{s2}. Due to circuit symmetry, L_{r1} is designed to be equal to L_{r2}, and C_{s1} is designed to be equal to C_{s2}. To simplify the inverter analysis, the main inverter switches and the load are replaced with S_{inv} and I_o as shown in Fig. 2. Also diode D_o stands for the anti-parallel diodes of the inverter switches. In order to simplify the inverter operating analysis, all of the circuit elements are assumed to be ideal.

The main theoretical waveforms of the proposed inverter are presented in Fig. 3. The proposed inverter has six distinct operating modes in a switching cycle, as shown in Fig. 4. Before the first operating mode, it is supposed that S_{a1} is on and that S_{a2} is off. Also, it is assumed that switch S_{inv} is on, I_o is flowing through D_o and the L_{r1} current is increasing.

Mode 1 ($t_0 \le t \le t_1$)**:** When the L_{r1} current reaches I_o, D_o turns off under the ZCS condition and then the additional current flows through S_{inv}. The L_{r1} current is:

$$I_{Lr1}(t) = \frac{V_s}{L_{r1}}(t - t_0). \tag{1}$$

The L_{r1} current increases linearly until it reaches I_i which is defined as the minimum required current of L_{r1} that guarantees the charging of C_r in mode 4. The design procedure of $I_i$is illustrated in section III. The duration of this mode is:

$$\Delta t_1 = t_1 - t_0 = \frac{L_{r1} I_i}{V_s}. \tag{2}$$

Mode 2 ($t_1 \le t \le t_2$)**:** At t_1, the states of the inverter main switches are changed. Due to C_r, the inverter main switches are turned off under the ZVS condition. This means that S_{inv} is turned off. Thus a resonance starts between C_r, C_{s2} and L_{r1} which increases the DC-link voltage. C_{s2} is designed to absorb the energy stored in the leakage inductance L_{r2} at the S_{a2} turn off instant. Therefore the discharging time of C_{s2} is negligible. The C_r voltage and the L_{r1} current equations are:

$$\begin{aligned} V_{Cr}(t) = {} & Z_r(I_i - I_o)\sin(\omega_r(t - t_1)) \\ & + V_s(1 - \cos(\omega_r(t - t_1))) \end{aligned} \tag{3}$$

$$\begin{aligned} I_{Lr1}(t) = {} & (I_i - I_o)\cos(\omega_r(t - t_1)) \\ & + \frac{V_s}{Z_r}\sin(\omega_r(t - t_1)) + I_o \end{aligned} \tag{4}$$

where

$$\omega_r = \frac{1}{\sqrt{L_{r1} C_r}} \quad , \quad Z_r = \sqrt{\frac{L_{r1}}{C_r}}. \tag{5}$$

This mode continues until the C_r voltage reaches V_s. Duration of this mode is:

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_r}\tan^{-1}\left(\frac{V_s}{Z_r(I_i - I_o)}\right). \tag{6}$$

Mode 3 ($t_2 \le t \le t_3$)**:** At t_2, the C_r voltage reaches V_s and the diode D_2 turns on under the ZVS condition. Thus, a fraction of the L_{r1} linkage flux moves to L_{r2} and the current of L_{r2} begins to freewheel through the switch S_{a1} and the inductor L_{r2}. At the beginning of this interval, the L_{r1} current is:

$$I_{Lr1}(t_2) = I_1 = \sqrt{\left(\frac{V_s}{Z_r}\right)^2 + (I_i - I_o)^2} + I_o. \tag{7}$$

The ampere-turns of the coupled inductors must be constant, so I_{Lr1} and I_{Lr2} are obtained as follows:

$$I_{Lr1} = \frac{I_1 + I_o}{2} \tag{8}$$

$$I_{Lr2} = \frac{I_1 - I_o}{2}. \tag{9}$$

In this mode the power flows from the source to the load. This mode continues until a change is required in the inverter switches.

Mode 4 ($t_3 \le t \le t_4$)**:** If the states of the inverter main switches need to be changed, S_{a1} must be turned off. Thus the ampere-turns of L_{r1} move to L_{r2} and the L_{r2} current increases. Therefore C_r begins to discharge.

Note that a part of the L_{r2} energy used to charge C_{s1} is negligible since C_{s1} is a smaller capacitance in comparison with C_r. In this mode L_{r1} resonates with C_r and the C_r voltage decreases to zero. S_{a1} is turned off under the ZVS condition at the beginning of this mode. Also, S_{a2} can be turned on under the ZVZCS condition due to the conduction of D_2. The L_{r2} current and the C_r voltage in this mode are:

$$V_{Cr}(t) = V_s - Z_r I_1 \sin(\omega_r(t - t_3)) \tag{10}$$

$$I_{Lr2}(t) = I_1 \cos(\omega_r(t - t_3)). \tag{11}$$

When the C_r voltage reaches zero, this interval ends. Thus, the duration of this mode is:

$$\Delta t_4 = t_4 - t_3 = \frac{1}{\omega_r}\sin^{-1}\left(\frac{V_s}{Z_r I_1}\right). \tag{12}$$

Mode 5 ($t_4 \le t \le t_5$)**:** In this interval, the diode D_o turns on under the ZVS condition and the L_{r2} current is discharged to the input source via D_o. Thus, the switch S_{inv} can be turned

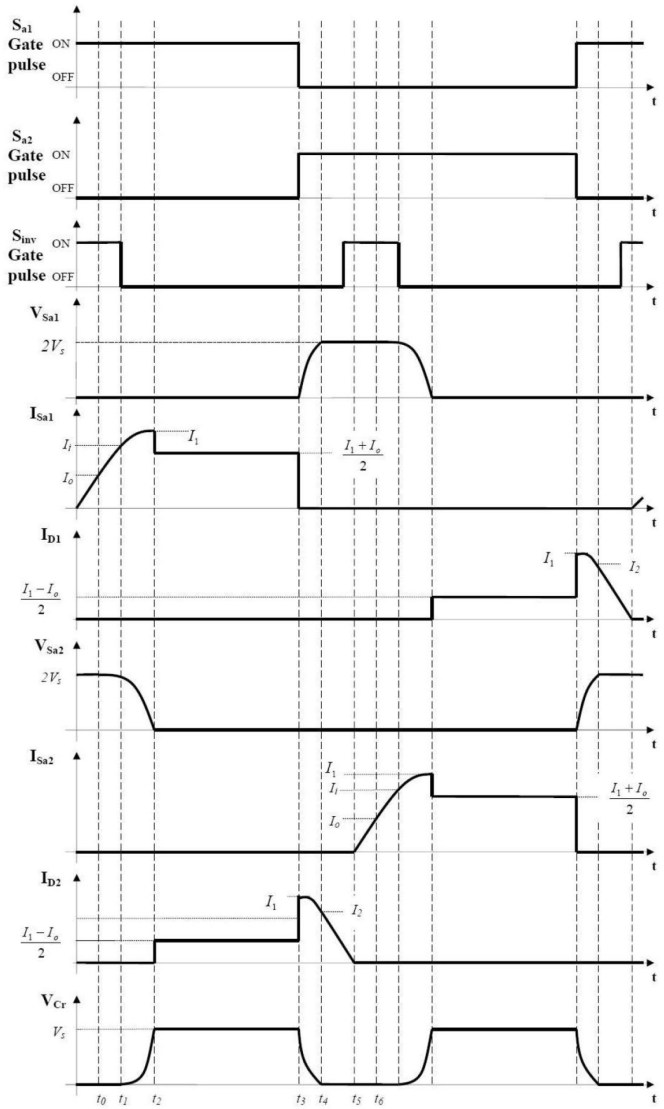

Fig. 3. Main theoretical waveforms of the proposed inverter.

on under the ZVZCS condition. The L_{r2} current decreases linearly from I_2 to zero. Thus the L_{r2} current is:

$$I_{Lr2}(t) = I_2 - \frac{V_s}{L_{r2}}(t - t_4) \tag{13}$$

where

$$I_2 = I_{Lr2}(t_4) = \sqrt{I_1^2 - (\frac{V_s}{Z_r})^2}. \tag{14}$$

Duration of this mode is:

$$\Delta t_5 = t_5 - t_4 = \frac{L_{r2} I_2}{V_s}. \tag{15}$$

Mode 6 ($t_5 \leq t \leq t_6$)**:** At t_5, the L_{r2} current reaches zero and the diode D_2 turns off under the ZCS condition. In this mode the L_{r2} current reverses and flows through S_{a2} and S_{inv}.

III. Design Consideration of the Proposed Soft Switching Inverter

Designing the proposed circuit involves the selection of L_{r1}, C_{s1}, C_r and I_i. The inductor L_{r1} provides the zero current switching condition for the DC-link switch at the turn on instant.

Therefore its value can be selected like that of a regular turn on snubber [15]. The capacitor C_{s1} provides the zero voltage switching condition at the switch turn off instant for the DC-link switch. Therefore its value can be selected like that of a regular turn off snubber [15].

C_r is designed to be much larger than C_{s1} and therefore the resonance time between C_{s1} and L_{r1} in mode 4 is negligible.

A practical design for the ratio of C_r/C_{s1} is between 10 and 20.

The initial current I_i must be large enough to guarantee the discharging of C_r in mode 4. Thus according to equation (10):

$$Z_r I_1 \geq V_s. \tag{16}$$

By substituting I_1 from equation (7) in equation (16), the following relation is obtained:

$$I_i \geq I_o + \sqrt{I_o^2 - 2 I_o \frac{V_s}{Z_r}}. \tag{17}$$

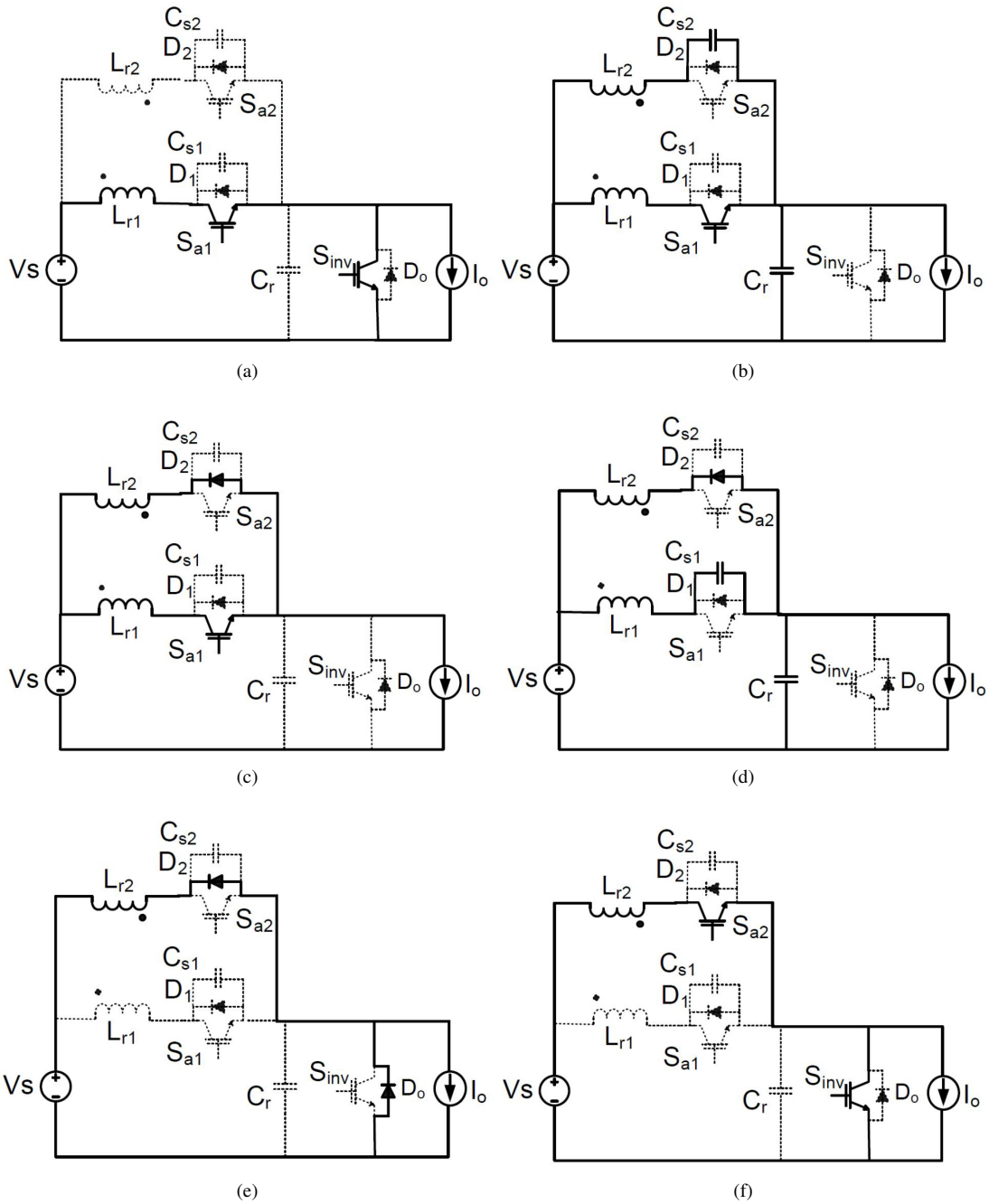

Fig. 4. Equivalent circuit of (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, (e) mode 5, and (f) mode 6.

t is necessary to design for the worst possible condition. The right side of relation (17) is at its maximum when I_o is maximized. In practice, to compensate for the effect of C_{s2} and C_{s1} in the second and fourth modes, I_i must be designed 20 percent larger than its calculated value. Thus the following equation is obtained:

$$I_i = 1.2(I_{om} + \sqrt{I_{om}^2 - 2I_{om}\frac{V_s}{Z_r}}) \quad (18)$$

where I_{om} is the maximum of I_o.

IV. Experimental Results

A prototype of the proposed soft switching inverter is implemented at a 20kHz switching frequency. The input voltage (V_s) is 100V and the output load power is 250W with a 0.9 power factor. The output frequency is 400Hz. According to the design procedure, the auxiliary circuit parameters are calculated as C_r =10nF, C_s=470pF, and L_r =18μH.

A photograph of the prototype inverter circuit is shown in figure 5. The switches in the inverter are IRFP460. A 470μF capacitor is placed at the rectifier output and the inverter input. The inverter input power is produced with a rectifying 50Hz voltage that was obtained from an autotransformer. The

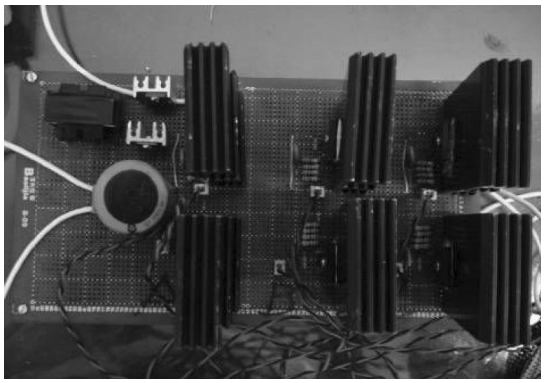

Fig. 5. Photograph of the prototype inverter circuit.

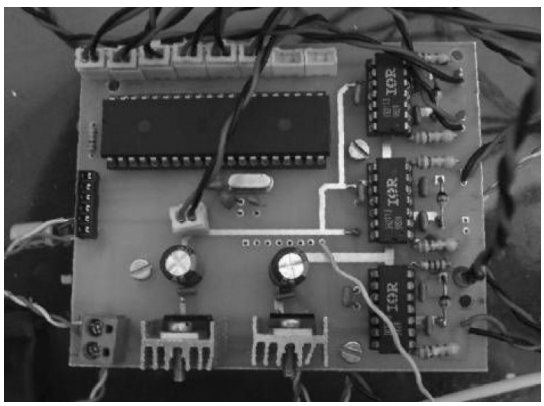

Fig. 6. Photograph of the prototype control circuit.

inverter load is a simple R-L load. A photograph of the prototype control circuit is shown in Fig. 6. The gate pulses are produced with an ATMEGA16 microcontroller and the gate drivers are IR2113.

The experimental results are illustrated in figures 7, 8 and 9. The voltages and currents of the auxiliary switches are illustrated in Fig. 7. The inherent anti-parallel diodes of the auxiliary switches are considered as D_1 and D_2. Thus, sum of the switches and the anti-parallel diodes are shown in this figure. It can be seen that the auxiliary switches are turned on under the ZVZCS condition and turned off under ZVS condition. The voltage and current waveforms of the inverter main switches along with the DC-link voltage are shown in Fig. 8. It can be seen from this figure that the inverter main switches are turned on and off under the ZVS conditions. Fig. 9 shows the inverter three phase output currents.

In Fig. 10 the proposed inverter efficiency is compared with a hard switching inverter at several output power levels. It can be seen that the efficiency of the proposed inverter is improved by about 2 percent at nominal power. This improvement is one of the several advantages of soft switching. Other advantages include a reduction in electromagnetic interference and an increase in the switching frequency of the inverter.

V. Conclusion

In this paper, a new soft switching three phase inverter is presented. To achieve soft switching for the main switches, the converter uses two DC-link switches. The inverter main switches are turned on and off under the zero voltage condition

Fig. 7. 1: S_{a1}+D_1current (5A/div), 2: S_{a1} voltage (50V/div), 3: S_{a2}+D_2 current (5A/div), 4: S_{a2} voltage (50V/div), (time: 5μs/div).

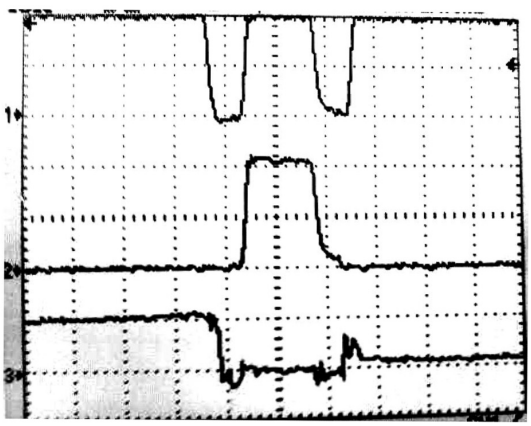

Fig. 8. Top: C_r voltage (50V/div), Center: S_1 voltage(50V/div), Bottom: S_1 current (2A/div), (time: 5μs/div).

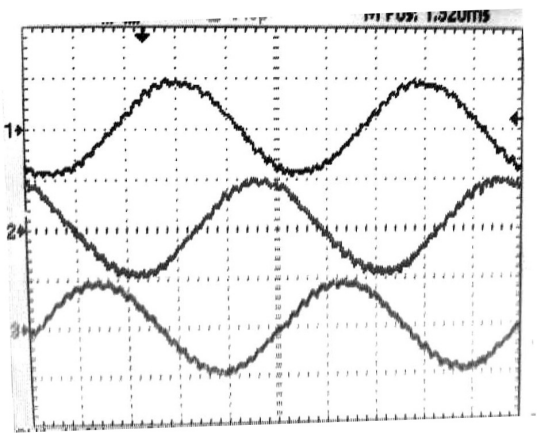

Fig. 9. Three phase output current (5A/div), (time: 500μs/div).

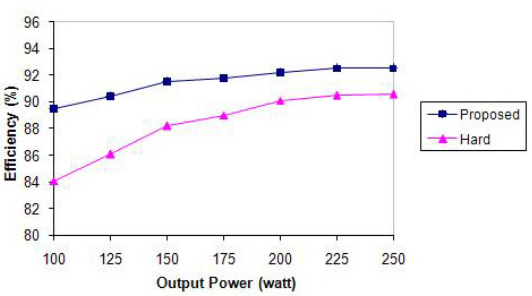

Fig. 10. Proposed inverter and hard switching efficiency curves.

as illustrated in the experimental results. The experimental results confirm the theoretical analysis of the proposed converter.

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