JPE 11-6-3

Investigating Buck DC-DC Converter Operation in Different Operational Modes and Obtaining the Minimum Output Voltage Ripple Considering Filter Size

Ebrahim Babaei[†], Mir Esmaeel Seyed Mahmoodieh[*], and Mehran Sabahi[*]

[†*] Department of Electrical Engineering, Ahar Branch, Islamic Azad University, Ahar, Iran

Abstract

This paper investigates the operational modes of buck dc-dc converters and their energy transmission methods. The operational modes of such converters are classified in two types, discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In this paper, the critical inductance relation of DCM and CCM is determined. The equations of the output voltage ripple (OVR) for each mode are obtained for a specific input voltage and load resistance range. The maximum output voltage ripple (MOVR) is also obtained for each mode. The filter size is decreased and the minimum required inductance value is calculated to guarantee the minimization of the MOVR. The experimental and simulation results in PSCAD/EMTDC prove the correctness of the presented theoretical concepts.

Key Words: Buck dc-dc converter, Critical inductance, Maximum output voltage ripple, Output voltage ripple

I. INTRODUCTION

DC-DC converters directly convert a specific dc voltage to another specific dc voltage. The most common types of dc-dc converters are buck, boost, buck-boost, and Cuk type converters. Nowadays, dc-dc converters play an important role in industry, electrical devices, electrical machines, air-space industry, portable systems, distributed generation, power factor correction, and voltage regulation [1]–[5]. In these applications, the output voltage quality is very important and it must have a minimum ripple value [6].

The majority of investigations done on buck dc-dc converters concentrate on new topologies [7], [8] and control methods [9], [10]. In these papers, the aim is either to improve a converter circuit topology and present a new structure or to present a new control strategy in order to improve the operation of a converter. In other words, they try to overcome major problems such as switching losses, converter size, and difficulties with electrical parameters. They generally improve converter functionality by creating a new topology and presenting a proper control method. It should be noted that the mentioned methods face disadvantages such as increases in the number of elements, circuit size increases, and losses increases. Applying some control methods leads to control system integration and sophistication.

Other applications considered for buck dc-dc converters are mines and refineries where flammable gasses are a major problem. In [11], a buck converter is investigated from an intrinsic security point of view. The optimized values for the inductances and capacitances are calculated in a way that the created spark is kept in its lowest value. This is accomplished by calculating the energy value stored in the inductors and capacitors. In [12], a buck dc-dc converter is investigated from an OVR point of view considering the intrinsic security level. This is accomplished by concentration on two aspects to maintain the intrinsic security level and to minimize the OVR by selecting proper inductance and capacitance values.

A buck dc-dc converter consists of energy storage elements (inductors and capacitors) whose values affect the magnitude of the OVR. Therefore, the values should be selected in a way that the magnitude of the OVR is minimized. In addition to these elements, the input voltage magnitude and the load resistance size affect the magnitude of the OVR. They must be kept under consideration in converter design.

This paper, investigates a buck dc-dc converter's OVR considering the filter size. The OVR is minimized and the required filter size is kept within an acceptable range by designing appropriate L and C parameters. In the proposed method, the OVR is controlled without adding any additional element or

Manuscript received Jan. 23, 2011; revised Oct. 1, 2011
Recommended for publication by Associate Editor Byung-Cho Choi.
[†] Corresponding Author: e-babaei@iau-ahar.ac.ir
Tel: +98-426-2235583, Fax: +98-426-2235432, Ahar Branch, Islamic Azad University
[*] Department of Electrical Engineering, Ahar Branch, Islamic Azad University, Iran

changing the classic structure of the converter. It is achieved through a proper design of the inductance and the capacitance. The OVR is minimized by determining appropriate values for the capacitors and the inductors in different ranges of input voltage and load resistance.

In [13] and [14], the output filter of a buck converter is designed for a special application considering the OVR. In the presented method, a buck dc-dc converter is investigated from two OVR and filter size points of view in a way that the converter shows desirable performance in both the DCM and CCM.

In this paper, the operation of a buck dc-dc converter is investigated in both DCM and CCM, and the critical inductance value between them is obtained. The relations of the OVRs are investigated in specific ranges of input voltage and load resistance. This is accomplished to achieve optimum inductance and capacitance values leading to the minimum value of the MOVR. Finally, the presented theoretical concepts and discussions are validated by experimental and simulation results in PSCAD/EMTDC.

II. Buck Dc-Dc Converter Operation Mode Analysis

Fig. 1(a) shows a circuit diagram of a buck dc-dc converter. The operation modes can be classified into CCM and DCM. This classification is carried out based on parameters such as duty cycle, input voltage, and load magnitude. In this paper, the operation modes are classified considering the converter inductance, where the border line of the CCM and DCM is commensurate with the critical inductance, L_C.

A. Converter Analysis in CCM

The CCM is the mode in which the inductor current (i_L) is always continuous and exists in all time intervals. The converter analysis in CCM is accomplished in the time intervals during which the switch S, is turned on (T_{on}) and is turned off (T_{off}) (as shown in Fig. 1). According to Fig. 1(a), as the switch is turned on, the diode D is reverse biased and the circuit shown in Fig. 1(a) is changed to the equivalent circuits shown in Figs. 1(b) and 1(c). As illustrated in Fig. 2(a), during this time interval (T_{on}), the inductor current increases linearly from its minimum value (I_{LV}) to its maximum value (I_{LP}). According to Fig. 1(a), the capacitor current is equal to $i_c = i_L - I_o$, where the load current is considered constant and assuming that the capacitor size is large enough. The T_{on} time interval is divided into two time intervals, $(0, t_0)$ and (t_0, t_1), comparing the inductor current with the load current. In $(0, t_0)$, since $i_c = i_L - I_o$ is valid, due to the fact that $i_L < I_o$, the capacitor current is negative and consequently the inductor and the capacitor provide the load current together. The equivalent circuit of Fig. 1(c) illustrates this fact well. In this time interval, as the capacitor discharges, its voltage decreases. At t_0, the capacitor voltage reaches its minimum value (V_{cv}) in which the current passing through it equals to zero. In (t_0, t_1), $i_L > I_o$ is valid and as a result the inductor charges the capacitor in addition to the load current provision. As the capacitor is charged, its voltage increases.

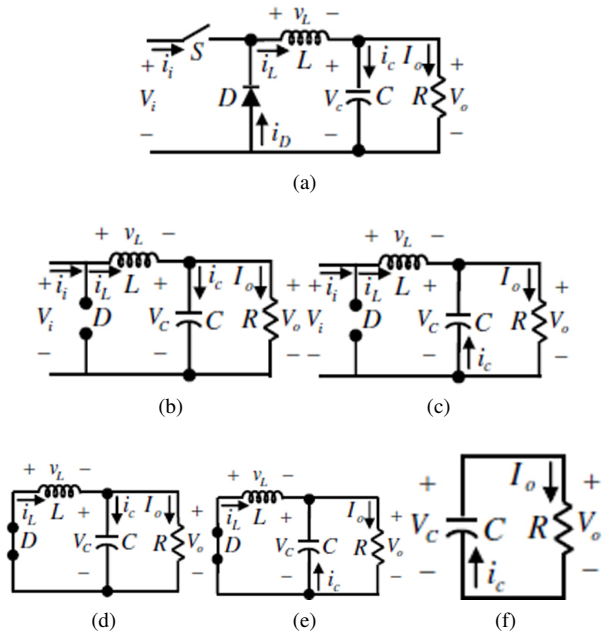

Fig. 1. (a) Buck dc-dc converter; (b) state in time interval T_{on}, $i_L > I_o$; (c) state in time interval T_{on}, $i_L < I_o$; (d) state in time interval T_{off}, $i_L > I_o$; (e) state in time interval T_{off}, $i_L < I_o$; (f) state in time interval T_{off}, $i_L = 0$.

As shown in Fig. 2(a), in the T_{off} time interval, the inductor current decreases linearly from its maximum value (I_{LP}) to its minimum value (I_{LV}). According to $i_c = i_L - I_o$ and comparing the inductor current with the load current, T_{off} is divided into two time intervals, (t_1, t_2) and (t_2, t_3). In (t_1, t_2), due to the fact that $i_L > I_o$, the capacitor current is positive and as a result the inductor charges capacitor in addition to the load current provision. The equivalent circuit of Fig. 1(d) illustrates this fact well. In this time interval, as the capacitor is charged, its voltage increases to reach its maximum value (V_{cp}) at t_2. In (t_2, t_3), since $i_L < I_o$, the capacitor current is negative and as a result the capacitor and the inductor the provide load current together. The equivalent circuit of Fig. 1(e) well illustrates this fact. During this time interval, the capacitor voltage decreases as it is discharged.

B. Converter Analysis in DCM

The DCM is the mode in which the inductor current is zero in one interval and is not zero in the following interval. The analysis of a converter in the DCM for the time interval T_{on} is such an analysis as accomplished in the CCM for the time interval T_{on}, but with differences in the initial conditions of the inductor and capacitor currents, and the output voltage.

As shown in Fig. 2(b), in the T_{off} time interval, the inductor current decreases linearly from its maximum value (I_{LP}) to zero. The T_{off} time interval is divided into three time intervals (t_1, t_2), (t_2, t_2'), and (t_2', t_3). In (t_1, t_2), due to the fact that $i_L > I_o$, the capacitor current is positive and as a result the inductor charges the capacitor in addition to the load current provision. The equivalent circuit of Fig. 1(d) illustrates this fact well. In this time interval, as the capacitor is charged, its voltage increases to reach its maximum value (V_{cp}) at t_2. In (t_2, t_2'), due to the fact that the inductor current is less than the load current, the capacitor current is negative since $i_c =$

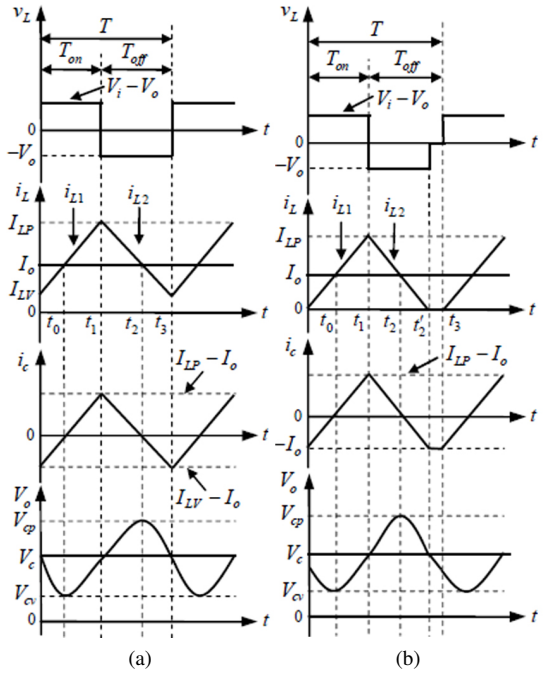

Fig. 2. Inductor voltage, inductor current, capacitor current, and output voltage. (a) CCM. (b) DCM.

$i_L - I_o$ is valid. Here, the capacitor and the inductor provide the load current together. This is well illustrated in the equivalent circuit of Fig. 1(e). In this time interval, the capacitor voltage decreases as its energy is discharged. In (t_2', t_3), the capacitor current equals to $-I_o$, since the inductor current is zero and as a result, the capacitor provides the load current by itself. The equivalent circuit of Fig. 1(f) illustrates this fact well. In this time interval, the capacitor voltage decreases linearly because the capacitor current is constant.

III. Calculating The Critical Inductance Between The Ccm And Dcm Modes

The borderlines between the different operational modes of a buck dc-dc converter can be determined by the critical inductance since these operational modes are indicated by the inductance depended inductor current. In order to achieve the critical inductance L_C, which exists between CCM and DCM, it can be in Figs. 2(a) and 2(b) that $I_{LV} = 0$ should be valid. In order to achieve this, it is necessary to calculate I_{LP} and I_{LV} initially. The energy survival law is applied as follows to calculate I_{LV} and I_{LP}.

$$\int_0^T i_c(t)dt = 0 \tag{1}$$

Considering Fig. 1(a), the current passing through the capacitor is as follows:

$$i_c(t) = i_L(t) - I_o \tag{2}$$

Considering Figs. 1(b) and 2(a), the inductor voltage in T_{on} (v_{L1}), can be expressed by:

$$v_{L1} = V_i - V_o \tag{3}$$

The following equation is always valid for the inductor current and voltage:

$$v_L = L\frac{di_L}{dt} \tag{4}$$

Using (3) and (4), it is clear that:

$$i_{L1}(t) = \frac{V_i - V_o}{L}t + I_{LV} \tag{5}$$

where $i_{L1}(t)$ is the inductor current in T_{on}.

Applying (5) in (2) the capacitor current in T_{on} (i_{c1}) is as follows:

$$i_{c1}(t) = \frac{V_i - V_o}{L}t + I_{LV} - I_o \tag{6}$$

Considering Fig. 1(d), the inductor voltage in T_{off} (v_{L2}) is equal to $-V_o$, so by allying the above value in (4) and assuming that $t_1 = 0$ is valid (new time era), the inductor current is obtained in T_{off} (i_{L2}):

$$i_{L2}(t) = -\frac{V_o}{L}t + I_{LP} - I_o \tag{7}$$

Considering (2) and (7), the capacitor current in T_{off} (i_{c2}) can be calculated as follows:

$$i_{c2}(t) = -\frac{V_o}{L}t + I_{LP} - I_o \tag{8}$$

The converter duty cycle (D) is defined as follows:

$$D = \frac{T_{on}}{T} \tag{9}$$

The following is valid if the buck dc-dc converter operates in CCM:

$$D = \frac{V_o}{V_i} \tag{10}$$

Applying the boundary provisions in (5) leads to the following:

$$I_{LP} - I_{LV} = \frac{V_i - V_o}{Lf}D \tag{11}$$

Applying (6) and (8) in (1), and considering (9)-(11) and $V_o = RI_o$, the value of I_{LP} can be expressed as:

$$I_{LP} = I_o\left[1 + \frac{R}{2Lf}(1-D)\right] \tag{12}$$

Using (11) and (12), I_{LV} is achieved as follows:

$$I_{LV} = I_o\left[1 - \frac{R}{2Lf}(1-D)\right] \tag{13}$$

It is obvious from Figs. 2(a) and 2(b) that the critical inductance (L_C) between CCM and DCM is obtained applying $I_{LV} = 0$ in (13). As a result:

$$L_C = \frac{R}{2f}(1-D) \tag{14}$$

According to (10), (14) can be expressed as follows:

$$L_C = \frac{R}{2f}\frac{(V_i - V_o)}{V_i} \tag{15}$$

If $L < L_C$, the converter operates in DCM and if $L > L_C$, it operates in CCM. According to (15), L_C is function of V_i and R. Due to Fig. 3, as the input voltage changes from $V_{i,\min}$ to $V_{i,\max}$ and the load resistance changes from $R_{\min}$ to $R_{\max}$, the operation region of the inverter would be a rectangul (ABCD)

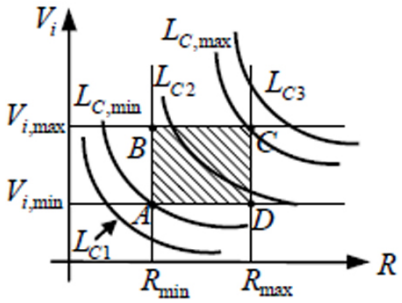

Fig. 3. Operational modes of the buck dc-dc converter in plate $R-V_i$.

in the $R-V_i$ plate. Note that Fig. 3 is drawn considering that $L_{C1} < L_{C,\min} < L_{C2} < L_{C,\max} < L_{C3}$ is valid.

Fig. 3 shows that the minimum and maximum critical inductances are commensurate by the A and C points, respectively. The magnitude of each can be expressed as follows:

$$L_{C,\min} = \frac{R_{\min}}{2f}\frac{(V_{i,\min}-V_o)}{V_{i,\min}} \tag{16}$$

$$L_{C,\max} = \frac{R_{\max}}{2f}\frac{(V_{i,\max}-V_o)}{V_{i,\max}} \tag{17}$$

Fig. 3 shows that the converter operates in the CCM if $L > L_{C,\max}$ is valid. This is denoted in Fig. 3 by L_{C3}. The converter operates in the DCM if $L < L_{C,\min}$ is valid. This is denoted in Fig. 3 by L_{C1}. Under the $L_{C,\min} < L < L_{C,\max}$ condition and for specific R and V_i values, and considering $V_{i,\min} < V_i < V_{i,\max}$ and $R_{\min} < R < R_{\max}$, if $L > L_C$ is valid, the converter operates in CCM and if $L < L_C$ is valid, the converter operates in DCM. This is denoted by L_{C2}.

IV. Output Voltage Ripple

The magnitude of the OVR is one of the most important parameters that should be taken under consideration in dc-dc converters design. In this kind of converter, the components should be designed in such a way that the output voltage possesses the minimum ripple magnitude. In this section, the magnitude of the OVR is calculated for each operational mode and the effect of each component and electrical parameter on the OVR magnitude is investigated.

A. Calculating the OVR in CCM

The magnitude of the OVR in CCM (V_{PP}^{CCM}) is obtained by integrating the capacitor current in the (t_0,t_2) time interval. According to Fig. 1(a), the output voltage of the converter is as follows:

$$V_o = V_c \tag{18}$$

Considering Fig. 2(a), the following is valid:

$$V_{cp} = V_{cv} + \frac{1}{C}\int_{t_0}^{t_2} i_c(t)dt \tag{19}$$

The OVR can be calculated as follows:

$$V_{PP}^{CCM} = V_{cp} - V_{cv} \tag{20}$$

Since the capacitor current is equal to (6) at (t_0,t_1), the value of t_0 can be expressed as follows, by applying zero for the capacitor current:

$$t_0 = \frac{L(I_o - I_{LV})}{V_i - V_o} \tag{21}$$

The value of t_2 can be obtained by applying zero for capacitor current in (8) as follows:

$$t_2 = \frac{L}{V_0}(I_{LP} - I_\circ) \tag{22}$$

Applying (6), (8), (10), (12), (20)-(22) in (19), the magnitude of the OVR in CCM can be expressed as follows:

$$V_{PP}^{CCM} = \frac{V_o(V_i - V_o)}{8LCf^2V_i} \tag{23}$$

It is obvious from (23) that the OVR magnitude in CCM does not depend on the load resistance. However, it is reversely related to the inductance value, and is directly related to the input voltage. In other words, the following is valid:

$$\frac{\partial V_{PP}^{CCM}}{\partial L} < 0 \tag{24}$$

$$\frac{\partial V_{PP}^{CCM}}{\partial V_i} > 0 \tag{25}$$

According to the mentioned explanations, for a specific V_i, the maximum OVR in CCM is obtained for $L = L_C$. By applying (15) in (23), the maximum OVR is obtained as follows:

$$V_{PP,\max}^{CCM} = \frac{V_o}{4fCR} \tag{26}$$

B. Calculating the OVR in DCM

The magnitude of the OVR in DCM (V_{PP}^{DCM}) is obtained by integrating the capacitor current in the (t_0,t_2) time interval. The following is always valid for the buck dc-dc converter in DCM [11]:

$$D^2 = \frac{2LfV_o^2}{RV_i(V_i - V_o)} \tag{27}$$

According to Fig. 2(b), I_{LP} can be calculated as follows:

$$I_{LP} = \frac{V_i - V_o}{Lf}D \tag{28}$$

The capacitor current in (t_0,t_1) is as follows:

$$i_{c1}(t) = \frac{V_i - V_o}{L}t - I_o \tag{29}$$

Due to the fact that the capacitor current is equal to zero at t_0, applying zero for the capacitor current in (29) results in:

$$t_0 = \frac{LI_o}{V_i - V_o} \tag{30}$$

Applying (8), (20), (22), (27)-(30) in (19), the magnitude of OVR is expressed as follows:

$$V_{PP}^{DCM} = \frac{V_o}{RfC} + \frac{LV_oV_i}{2R^2C(V_i - V_o)} - \frac{V_o\sqrt{2LV_i}}{RC\sqrt{Rf(V_i - V_o)}} \tag{31}$$

From (31), the following can be obtained:

$$\frac{\partial V_{PP}^{DCM}}{\partial L} < 0 \tag{32}$$

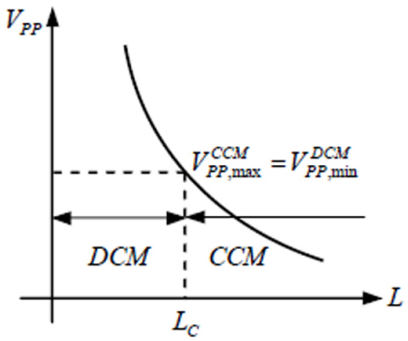

Fig. 4. The OVR variation curve in term of for constant V_i,C,f, and R_L.

$$\frac{\partial V_{PP}^{DCM}}{\partial V_i} > 0 \tag{33}$$

$$\frac{\partial V_{PP}^{DCM}}{\partial R_L} < 0 \tag{34}$$

It is obvious from (32), (33) and (34) that the OVR magnitude in DCM is reversely related to the inductance value and the load resistance, and it is directly related to the input voltage.

According to the mentioned explanations, for an specific V_i, the minimum OVR in DCM is obtained for $L = L_C$. Applying (15) in (31), the minimum OVR is obtained as follows:

$$V_{PP,\min}^{DCM} = \frac{V_o}{4fCR} = V_{PP,\max}^{CCM} \tag{35}$$

According to the explanations mentioned above, the OVR is basically determined by the inductance value. For different operational modes and for a constant switching frequency, capacitance, input voltage, and load resistance, the relation of the OVR and L is as shown in Fig. 4, due to the voltage ripple relations. As shown in Fig. 4, in a buck dc-dc converter with constant switching frequency, specific capacitance, input voltage, and load resistance values, the OVR magnitude is minimized in CCM and it is maximized in DCM. It depends on the inductance values in both modes.

V. Maximum Output Voltage Ripple

As previously mentioned, the OVR is directly related to V_i and is reversely related to the inductance value in the CCM operational mode. It does not depend on the load resistance value. The OVR magnitude in DCM is reversely related to the load resistance and inductance values and is directly related to the input voltage. Therefore, the worst operational condition (the MOVR condition) occurs for maximum value of $V_{i,\max}$ and the minimum value of $R_{\min}$. Under this condition and according to (15), the critical inductance for $V_{i,\max}$ and $R_{\min}$ are as follows:

$$L_{C,MOVR} = \frac{R_{\min}}{2f}\frac{(V_{i,\max} - V_o)}{V_{i,\max}} \tag{36}$$

The following can be concluded by comparing (36) with (16) and (17):

$$L_{C,\min} < L_{C,MOVR} < L_{C,\max} \tag{37}$$

According to (37), the operation region of the converter in the worst condition (MOVR) would be as Fig. 5.

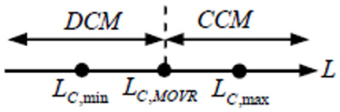

Fig. 5. The operation region of converter in the worst condition.

As the inductance value increases, the MOVR value decreases since the OVR magnitude is reversely related to the inductance value. Therefore, as illustrated in Fig. 5, the minimum value of the MOVR in DCM occurs for $L = L_{C,MOVR}$. Applying $L_{C,MOVR}$ in (31), the minimum value of MOVR is as follows:

$$\min\{V_{PP,\max}^{DCM}\} = \frac{V_o}{R_{\min}fC} + \frac{L_{C,MOVR}V_oV_{i,\max}}{2R_{\min}^2C(V_{i,\max} - V_o)} - \frac{V_o\sqrt{2L_{C,MOVR}V_{i,\max}}}{R_{\min}C\sqrt{R_{\min}f(V_{i,\max} - V_o)}} \tag{38}$$

Applying (36) in (38) leads to the minimum MOVR magnitude in DCM as follows:

$$\min\{V_{PP,\max}^{DCM}\} = \frac{V_o}{4fCR_{\min}} \tag{39}$$

As shown in Fig. 5, the maximum MOVR in CCM is obtained for $L = L_{C,MOVR}$. Applying $L_{C,MOVR}$ in (23), the maximum MOVR is as follows:

$$\max\{V_{PP,\max}^{CCM}\} = \frac{V_o(V_{i,\max} - V_o)}{8L_{C,MOVR}Cf^2V_{i,\max}} \tag{40}$$

Considering (36) and (40), the maximum magnitude of the MOVR in CCM can be expressed as follows:

$$\max\{V_{PP,\max}^{CCM}\} = \frac{V_o}{4fCR_{\min}} = \min\{V_{PP,\max}^{DCM}\} \tag{41}$$

VI. Design Considerations

The magnitude of the OVR is one of the most important electrical parameters in dc-dc converters. It is determined by L and C in the constant switching frequency. As is obvious from the OVR relations of CCM and DCM, the magnitude of the OVR is reversely related with the L, C, and f values. For OVR minimization, the values of the parameters L and C are important in the load resistance and the input voltage ranges. Due to the limitations that exist in high frequency power switch manufacturing and switching loss increases, the switching frequency cannot be increased very much. The method proposed in this section is an optimum method for achieving a low OVR with a minimum filter (L,C) size.

As previously mentioned, it is shown in Fig. 4 that the OVR in DCM possesses its maximum magnitude while it is lower in CCM. As can be seen in Fig. 5, for $L_{C,MOVR}$, the MOVR in DCM has its minimum magnitude which equals that of the converter in CCM. Equation (41) proves this fact. According to the discussions in previous sections, the magnitude of the OVR decreases as the inductance increases. In other words, the inductance value can be increased to minimize the magnitude of the OVR. The inductor value cannot be very large due to a saturation problem and a filter size increase. Therefore, it can be concluded that in the worst condition (MOVR), which occurs for $V_{i,\max}$ and $R_{\min}$, the OVR magnitude has

its minimum value of $L_{C,MOVR}$. In other words, the minimum magnitude of the proposed inductance is as follows:

$$L_{\min} = L_{C,MOVR} \tag{42}$$

Under this condition and due to (41), the maximum magnitude of the OVR in the worst condition (MOVR) is:

$$V_{PP,\max} = \frac{V_o}{4fCR_{\min}} \tag{43}$$

According to (43), the minimum value of the capacitor is considered as follows:

$$C_{\min} = \frac{V_o}{4fR_{\min}V_{PP,\max}} \tag{44}$$

In fact, the equivalent series resistance (ESR) and the equivalent series inductance (ESL) of the capacitor have a remarkable influence on the voltage ripple level. Therefore, an adequate multiple factor λ must be considered, i.e. [11], [16]:

$$C = \lambda C_{\min} \tag{45}$$

If the values of the inductance and the capacitor capacity are selected according to (42) and (44), the MOVR ripple is minimized and so the quality of the output voltage increases. Often dc/dc Buck converters are applied in places such as refineries and mines. There are explosive gases in such places, so by selecting the minimum values for the inductance and the capacitor, the value of the reserved energy will be less and so the intrinsic safety of the converter increases [11]. In addition to the maximum output voltage ripple and the intrinsic safety of the converter, for these values of the inductance and the capacitor, the size of the converter output filter will be small which is important in designing Buck dc/dc converters [13].

In the buck dc-dc converters and for heavy loads $(R_{\min})$, the current peak is higher in DCM when compared with CCM and it flows through the switches during the switching process. This current causes switching stress and as a result, DCM is not suggested. In CCM, due to (23) the OVR does not depend on R. Therefore, in this operational mode, there is no load magnitude limitation for converter operation.

VII. Theoretical Analysis

Fig. 6(a) shows the OVR variation curve in terms of the inductance for a specific V_i and R. As can be seen, the OVR magnitude decreases as the inductance increases. Fig. 6(a) shows that the OVR magnitude in DCM is more than the OVR magnitude in CCM. As can be seen, for equal voltages, a load resistance increase has no effect on the OVR magnitude in CCM.

For $R = 40\Omega$, $V_o = 8V$, and for inductance values of $0.4mH$, $1mH$, and $5mH$, the OVR variation curve in terms of the input voltage is illustrated in Fig. 6(b). It is obvious from Fig. 6(b) that for a constant input voltage, the OVR decreases as the inductance increases.

For $V_i = 12V$, $V_o = 8V$, and for inductance values of $0.4mH$, $1mH$, and $5mH$, the OVR variation curve in terms of load resistance is illustrated in Fig. 6(c). It is obvious from Fig. 6(c) that for a $5mH$ inductance value, the converter operates in CCM, where the OVR is independent of the load resistance and the OVR does not vary as the load resistance increases. For a $1mH$ inductance value and for low resistances, the converter operates in CCM, and because the OVR magnitude does not depend on the load resistance in CCM, according to Fig. 6(c), the OVR remains constant. For the same inductance value, as the load resistance increases, the converter operates in DCM and the OVR decreases as the load increases. For a $0.4mH$ inductance value, the converter operates in DCM and the OVR decreases as the load resistance increases. The curves shown in this section are drawn for the capacitance $C_{\min}$ calculated in section VI. This capacitance is obtained for the maximum magnitude of the OVR and the minimum value of the load resistance.

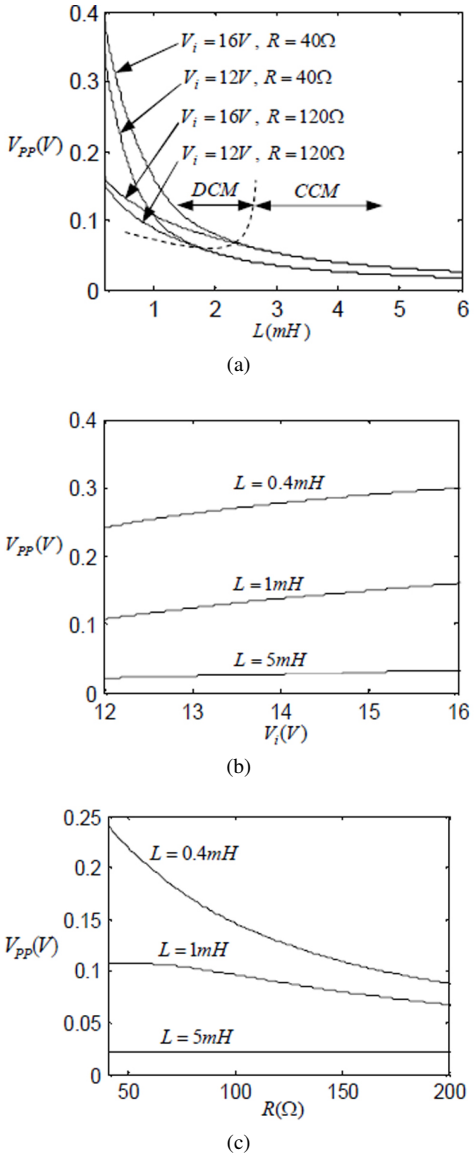

Fig. 6. Variations of OVR. (a) Versus inductance. (b) Versus V_i. (c) Versus R.

VIII. Experimental And Simulation Results

The buck dc-dc converter shown in Fig. 1(a) is simulated with PSCAD/EMTDC under different operational conditions to prove the correctness of the theories proposed in previous

sections. Experimental results are also presented to clarify the studies and to compare the theoretical and the practical results. The results are presented in the steady state. The main parameters are considered as follows [15]: $f = 10kHz$, $R = 40 - 200\Omega$, $V_i = 12 - 16V$, and $V_{PP,\max} = \%2V_o$.

The voltage levels, the switching frequency and the other electrical parameters of the converter have been selected in the experimental ranges. Another reason for selecting such numerical values for the electrical quantities of the converter is for considering the application of these kinds of converters (mines control systems, petrochemical plants, refineries) which was referred in [16].

The experimental and simulation results of the buck dc-dc converter are presented in both the CCM and DCM using the following values selected from the above ranges: $I_o = 0.08A$, $R = 100\Omega$, $V_i = 12V$, and $V_o = 8V$.

Considering (15)-(17), (36), and (44), the values of L_C, $L_{C,\min}$, $L_{C,\max}$, $L_{C,MOVR}$, and $C_{\min}$ are obtained as $1.67mH$, $0.67mH$, $5mH$, $1mH$, and $31.25\mu F$, respectively.

The inductor current and output voltage waveforms are shown in Fig. 7 considering different inductance values. A two-channel storage oscilloscope is used for making experimental measurements. The first channel is used to show the waveforms for the current passing through the inductor and the second channel is used to show the output voltage waveform. The dc coupling is used for the first channel, while the ac coupling is used for the second one. The zero level of the first channel (the current passing through the inductor) is depicted in the figures. Due to the coupling application for the second channel and proper $volt/div$ tuning, the zero level of the second channel is not visible on the oscilloscope screen.

According to Fig. 7(a), for $L = 2mH$, it is shown that the converter operates in CCM since this is more than $L_C = 1.67mH$. For $L = 0.5mH$, the converter operates in DCM since this is less than $L_C = 1.67mH$. In this mode, the inductor current equals zero. The result obtained in Fig. 7(b) illustrates this fact. According to Figs. 7(a) and 7(b), it can be seen that the experimental results are completely in accordance with the theoretical analysis presented in Figs. 2(a) and 2(b).

In the simulation results shown in Fig. 8(a), it is obvious that in DCM and for $R = 40\Omega$ (a heavy load), the inductor peak current increases when compared with similar the condition shown in Fig. 7(b). This confirms the correctness of the discussions mentioned in section VI.

In order to confirm the fact that the maximum OVR does not exceed $\%2V_o = 0.16V$ for $L_{\min} = L_{C,MOVR}$, the system is simulated for $V_{i,\max}$, $R_{\min}$ (the worst condition) and $L = L_{C,.MOVR} = 1mH$. Fig. 8(b) illustrates this fact well.

IX. Conclusions

The critical inductance existing between the CCM and the DCM of a buck converter is obtained by applying zero to the minimum inductor current. For inductances lower than this value, the converter operates in DCM and it operates in CCM for values more than the critical inductance value. The magnitude of the OVR in CCM and DCM decreases as the inductance increases. The analyses show that in CCM,

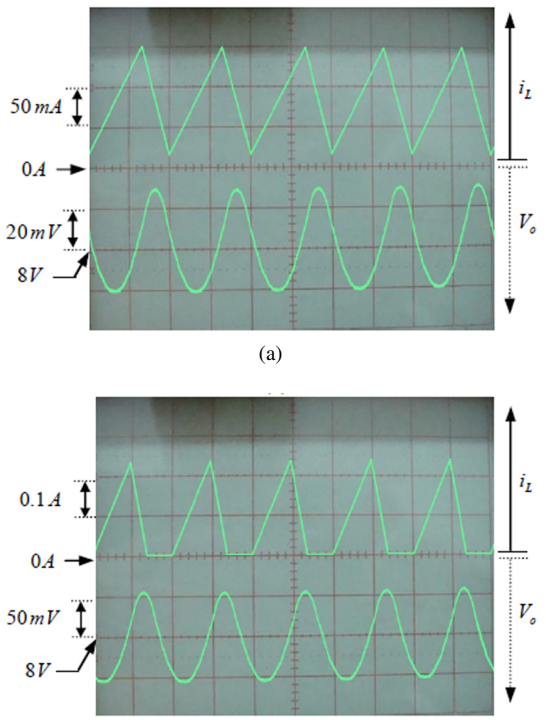

Fig. 7. Experimental results ($time/div = 50\mu s$) for different inductances; (a) CCM ($L = 2mH$); (b) DCM ($L = 0.5mH$).

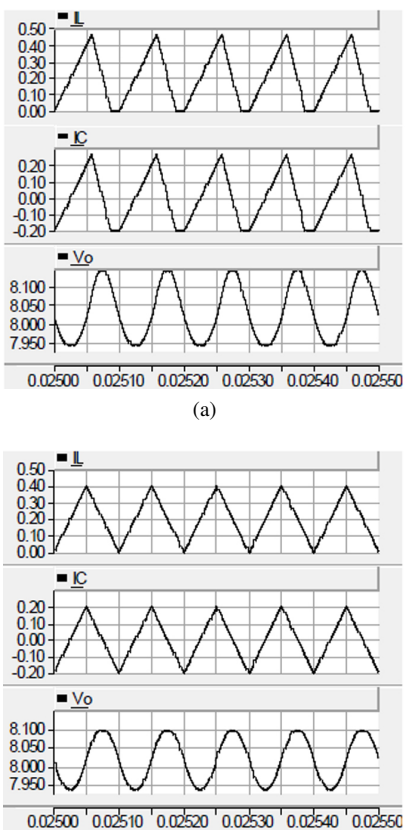

Fig. 8. (a) The DCM for heavy load ($R = 40\Omega$); (b) MOVR in the buck converter for $V_{i,\max}$ and $R_{\min}$(worst condition).

the OVR is directly related to the input voltage. However, this is independent from the load resistance value. In DCM, the OVR is directly related to the input voltage and it is reversely related to the load resistance. The results of this research also show that in DCM the MOVR is minimized for $L_{C,MOVR}$. This MOVR magnitude is equal to the maximum magnitude of the MOVR in CCM for $L_{C,MOVR}$. Selecting the minimum inductance value as $L_{C,MOVR}$ and using the minimum capacitance as (44), the converter filter size is minimized in addition to the MOVR reduction. The parameter $L_{C,MOVR}$ is the critical inductance value between the DCM and the CCM under the maximum input voltage and minimum load resistance condition.

REFERENCES

[1] A. Khaligh, A. M. rahimi, and A. Emadi, "Modified pulse-adjustment technique to control dc/dc converters driving variable constant-power loads," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 3, pp. 1133-1146, Mar. 2008.

[2] I.-D. Kim, J.-Y. Kim, E.-C. Nho, and H.-G. Kim, "Analysis and design of a soft-switched pwm sepic dc-dc converter," *Journal of Power Electronics*, Vol. 10, No. 5, pp.461-467, Sep. 2010.

[3] W. R. Liou, M. L. Yeh, and Y. L. Kuo, "A high efficiency dual-mode buck converter integrated circuit for portable applications," *IEEE Trans. Power Electron*., Vol. 23, No, 2, pp. 667-677, Mar. 2008.

[4] H. Cha, R. Ding, Q. Tang, and Z. Peng, "Design and development of high power dc-dc converter for metro vehicle system," *IEEE Trans. Ind. Appl.*, Vol. 44, No. 6, pp. 1795-1804, Nov./Dec. 2008.

[5] M. G. Villava and E. F. Ruppert, "Input-controlled buck converter for photovoltaic applications: modeling and design," in *Proc. PEMD,* pp. 505-509, 2008.

[6] N. D. Benavides and P. L. Chapman, "Modeling the effect of voltage ripple on the power output of photovoltaic modules," *IEEE Trans. Ind. Electron.,* Vol. 55, No. 7, pp. 2638-3643, Jul. 2008.

[7] T. Senanayake and T. Ninomiya, "An improved topology of inductor-switching dc-dc converter," *IEEE Trans. Ind. Electron.,* Vol. 52, No. 3, pp. 869-878, Jun. 2005.

[8] B. P. Divakar and D. Sutanto, "Optimum buck converter with a single switch," *IEEE Trans. Power Electron*., Vol. 14, No. 4, pp. 636-642, Jul. 1999.

[9] J. Xu and M. Qin, "Multi-pulse train control technique for buck converter in discontinuous conduction mode," *IET Power Electron.*, Vol. 3, No. 3, pp. 391-399, May 2010.

[10] K. M. Tsang and W. L. Chen, "Cascade controller for dc/dc buck converter," *IEE Proc. Electr. Power Appl.,* Vol. 152, No. 4, pp. 827-831, Jul. 2005.

[11] L. Shulin, L. Jian, Y. Yinling, and J. Zhong, "Design of intrinsically safe buck dc/dc converters," in *Proc. ICEMS*, Vol. 2, pp. 1327-1331, 2005.

[12] L. Shulin, L. Yan, and L. Li, "Analysis of output voltage ripple of buck dc-dc converter and its design," in *Proc. PEITS*, Vol. 2, pp. 112-115, 2009.

[13] A. De Nardo, N. Femia, G. Petrone, and G. Spagnuolo, "Optimal buck converter output filter design for point-of-load applications," *IEEE Trans. Ind. Electron.,* Vol. 57, No. 4, pp. 1330-1341, Apr. 2010.

[14] M. Jinno, P. Y Chen, Y. C. Lai, and K. Harada, "Investigation on the ripple voltage and the stability of synchronous rectifier buck converters with high output current and low output," voltage," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 3, pp. 1008-1016, Mar. 2010.

[15] E. Babaei, M. E. S. Mahmoodieh, and H. M. Mahery, "Operational modes and output voltage ripple analysis and design considerations of Buck-boost dc-dc converters," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 1, pp. 381-391, Jan. 2012.

[16] S.-L. Liu, J. Liu, H. Mao, and Y.-Q. Zhang, "Analysis of operating modes and output voltage ripple of boost dc-dc converters and its design considerations," *IEEE Trans. Power Electron.*, Vol. 23, No. 4, pp. 1813-1821, Jul. 2008.

Ebrahim Babaei was born in Ahar, Iran in 1970. He received his B.S. in Electronics Engineering and his M.S. in Electrical Engineering from the Department of Engineering, University of Tabriz, Tabriz, Iran in 1992 and 2001, respectively, graduating with First Class Honors. He received his Ph.D. in Electrical Engineering from the Department of Electrical and Computer Engineering, University of Tabriz, Iran, in 2007. He was an Assistant Professor from 2007 to 2011 and has been an Associate Professor since 2011. He is the author of more than 100 journal and conference papers. His current research interests include the analysis and control of power electronic converters, matrix converters and multilevel converters, as well as FACTS devices and power system dynamics.

Mir Esmaeel Seyed Mahmoodieh was born in Tabriz, Iran in 1984. He received his B.S. in Power Engineering from the Department of Engineering, Islamic Azad University of Ardabil, Iran, in 2008. He is currently pursuing his M.S. in Power Engineering at the Islamic Azad University of Ahar, Iran. His current research interests include the analysis, control and modelling of power electronic converters.

Mehran Sabahi was born in Tabriz, Iran, in 1968. He received his B.S. in Electronic Engineering from the University of Tabriz, his M.S. in Electrical Engineering from Tehran University, Tehran, Iran, and his Ph.D. in Electrical Engineering from the University of Tabriz, in 1991, 1994, and 2009, respectively. He has been an Assistant Professor since 2009. His current research interests include power electronic converters and renewable energy systems.