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Charge Balance Control Methods for a Class of Fundamental Frequency Modulated Asymmetric Cascaded Multilevel Inverters

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Abstract

Modulation strategies for multilevel inverters have typically focused on synthesizing a desired set of sinusoidal voltage waveforms using a fixed number of dc voltage sources. This makes the average power drawn from different dc voltage sources unequal and time varying. Therefore, the dc voltage sources are unregulated and require that corrective control action be incorporated. In this paper, first two new selections are proposed for determining the dc voltage sources values for asymmetric cascaded multilevel inverters. Then two modulation strategies are proposed for the dc power balancing of these types of multilevel inverters. Using the charge balance control methods, the power drawn from all of the dc sources are balanced except for the dc source used in the first H-bridge. The proposed control methods are validated by simulation and experimental results on a single-phase 21-level inverter.

Key Words: Asymmetric cascaded multilevel inverter, Charge balance control methods, Multilevel inverter, Symmetric cascaded multilevel inverter

I. INTRODUCTION

A multilevel inverter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltage as inputs [1]. Multilevel inverters have several advantages over conventional two-level inverters that use a high switching frequency pulse width modulation (PWM). The main advantages of the multilevel inverters include the high quality of the output quantities, the ability to operate at high power and high voltage with low power and low voltage switching devices, flexibility, etc. [2], [3].

Nowadays, there exist three commercial topologies for multilevel voltage source inverters: neutral point clamped (NPC) [4], cascaded H-bridge (CHB) [5] and flying capacitors (FC) [6]. Among these inverter topologies, the cascaded multilevel inverter reaches the highest output voltage and power levels (13.8 kV, 30 MVA), and the highest reliability due to its modular topology [7]. In addition to the conventional multilevel inverters, some other topologies have been presented for multilevel inverters [1], [8]–[10]. A new multilevel converter has also been presented in [11]. The topology consists of modular multilevel converter arms and it is used for ac/ac conversion at high voltage levels.

Unfortunately, multilevel inverters do have some disadvantages. One particular disadvantage is the larger number of power semiconductor switches that they require. Although lower voltage rated switches can be utilized in a multilevel inverter, each switch requires its own gate driver and protection circuits. This may cause the overall system to be more expensive and complex.

A CHB multilevel inverter is formed by connecting several single-phase H-bridge inverters in series. Each inverter generates a square-wave voltage waveform with a different duty cycle. Together, these form the output voltage waveform. There are two groups of cascaded multilevel inverters, the symmetric and the asymmetric multilevel inverters. In the symmetric multilevel inverters, there are an equal number of dc voltage sources in all-partial inverters. If one of the dc voltages is different from the other, it can be called an asymmetric multilevel inverter. This paper focuses on an asymmetric cascaded multilevel inverter.

The approaches for determining switching angles synthesize an output voltage waveform to eliminate particular harmonics. In these approaches, the dc power drawn from the dc voltage source of a single H-bridge over each cycle is different from one H-bridge to another [12]–[14]. As a result, the power drawn from different voltage sources varies as a function of the modulation level, the load level and the load power factor. This results in unsteady and unstable dc voltage levels. Thus, the stabilization of the voltage levels in the dc bus stack is an important concern that has been the focus of many research investigations [15]–[17].

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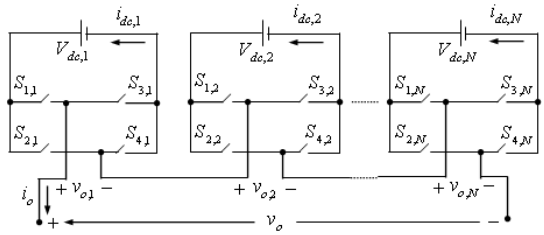

Fig. 1. Single-phase structure of a CHB multilevel inverter.

The dc power balancing in cascaded asymmetric multilevel inverters depends on the duty cycle of each level that is synthesizing the desired output waveforms. Generally, it is well understood that the power-balancing problem depends on the control strategy. To overcome the balancing problem of the dc power supplies in asymmetric multilevel inverters, special control methods are needed. It is important to note that different control methods for the voltage balancing of other types of multilevel inverters have been presented in [18]–[24]. A charge balance control method for symmetric cascaded multilevel inverters has been presented in [25]. This control strategy is based on the rotation of the duty cycles between different H-bridges in such a way that after some fundamental cycles, the average duty cycle of the H-bridges will be equal. This results in the charge balancing of the dc voltage sources. It is well understood that these charge balance control methods are not applicable to asymmetric multilevel inverters, since they do not have redundant switching combinations.

In this paper, firstly the basics of cascaded multilevel inverters are reviewed. Then, two new selections for the determination of the dc voltage source values of asymmetric multilevel inverters are proposed. In addition, two methods that are capable of balancing the dc power in the proposed cascaded asymmetric multilevel inverter are proposed. Finally, simulation and experimental results on a single-phase 21-level inverter are given to demonstrate the validity of the proposed selections and control methods.

II. Basics of the Cascaded Multilevel Inverters

Fig. 1 shows a CHB multilevel inverter. The switches in such an inverter must block a unidirectional voltage, but be able to conduct current in two directions, if a bidirectional power flow is desired. In this paper, an insulated gate bipolar transistor (IGBT) with an anti-parallel diode is used as a switch.

Considering Fig. 1, the output phase voltage is obtained by summing the output voltages of the H-bridges as follows:

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,N}(t) = \sum_{k=1}^{N} v_{o,k}(t) \quad (1)$$

where N is the number of CHBs.

Since the H-bridge cells can generate three output voltage levels ($+V_{dc,k}$, $-V_{dc,k}$ and zero), a switching function H_k (where $k = 1, 2, \cdots, N$) is defined for the H-bridge cells. The switching function for each H-bridge cell is defined to relate the dc bus quantities to the output quantities. The relation between the switching function H_k and the states of the switches $S_{1,k}$, $S_{2,k}$, $S_{3,k}$, and $S_{4,k}$ is as follows:

TABLE I
States Of The Switches And Switching Function For A Typical H-Bridge Cell

Switching function (H_k)	$S_{1,k}$	$S_{4,k}$	$v_{o,k}$	$i_{dc,k}$
1	1	1	$V_{dc,k}$	i_o
0	1	0	0	0
	0	1	0	0
−1	0	0	$-V_{dc,k}$	$-i_o$

$$H_k = S_{1,k} \cdot S_{4,k} - S_{2,k} \cdot S_{3,k} \quad (2)$$

where $S_{j,k}$ is the state of the switch S_j ($j = 1, 2, 3, 4$) for the k-th H-bridge. Each switch, $S_{j,k}$, can have the states 0 or 1 (1 means that the switch is turned on and 0 means it is turned off).

It is worth noting that the two switches of each leg are complementarily driven. Therefore, from (2), it can be seen that H_k can provide the states 1, 0 and -1. The states of the switches and the switching function for a typical H-bridge cell can be summarized as in Table I.

From Table I, it can be seen that the general relationships for the k-th H-bridge are as follows [17]:

$$v_{o,k} = H_k \cdot V_{dc,k} \quad (3)$$

$$i_{dc,k} = H_k \cdot i_o \quad (4)$$

The fundamental component of the output current can be written as:

$$i_o = I_{\max} \sin(\omega t + \phi) \quad (5)$$

where, ϕ is the angle between v_o and i_o.

Although each instance of the same harmonic of the voltage and the current contributes to the output power, the average power generated by the fundamental component of the voltage and the current is much more than that of the other higher order harmonics. Therefore, neglecting the power contribution of the higher order harmonics, only the fundamental component of the output current is considered [12].

III. Proposed Selection of the DC Voltage Source Values

The maximum number of output voltage levels (N_L) in a symmetric CHB multilevel inverter is related to the number of H-bridges (N) by the following equation:

$$N_L = 1 + 2N \quad (6)$$

Also, the maximum output voltage ($V_{o,Max}$) of N CHBs is:

$$V_{o,Max} = N \cdot V_{dc} \quad (7)$$

To provide a large number of output voltage levels without increasing the number of H-bridges, asymmetric multilevel inverters can be used. In [26] and [27], the magnitudes of the dc voltage sources have been chosen according to a geometric progression with a factor of two or three, which are called binary and trinary multilevel inverters, respectively. The number of output voltage levels for binary and trinary multilevel inverters are as follows, respectively:

$$N_L = 2^{N+1} - 1 \qquad if\ V_{dc,j} = 2^{j-1} V_{dc}; \quad j = 1, 2, \cdots, N \quad (8)$$

$$N_L = 3^N \qquad if\ V_{dc,j} = 3^{j-1}V_{dc}; \quad j = 1,\ 2, \cdots,\ N. \quad (9)$$

The maximum output voltage of a CHB multilevel inverter including N H-bridges is as follows:

$$V_{o,Max} = \sum_{j=1}^{N} V_{dc,j} \quad (10)$$

Equation (10) can be rewritten as (11) and (12) for binary and trinary multilevel inverters, respectively.

$$V_{o,Max} = (2^N - 1)V_{dc} \quad if\ V_{dc,j} = 2^{j-1}V_{dc}; \quad j = 1,\ 2, \cdots,\ N \quad (11)$$

$$V_{o,Max} = \left(\frac{3^N - 1}{2}\right)V_{dc} \quad if\ V_{dc,j} = 3^{j-1}V_{dc}; \quad j = 1, 2, \cdots,\ N. \quad (12)$$

By comparing (6)-(12), it can be seen that asymmetric multilevel inverters can generate more voltage levels and a higher maximum output voltage with the same number of H-bridges.

To provide a large number of output levels without increasing the number of H-bridges, two new asymmetric multilevel inverters are proposed in this paper. The proposed topologies combine the advantages of symmetric CHB multilevel inverters (i.e. modularity and cheaper design) and asymmetric multilevel inverters (i.e. high number of output voltage levels).

A. First Proposed Selection

In the first proposed selection for an asymmetric multilevel inverter, the values of the dc voltage sources are considered to be chosen according to the following equations:

$$V_{dc,1} = V_{dc} \quad (13)$$

$$V_{dc,j} = 2V_{dc} \qquad j = 2,\ 3,\ 4,\ \cdots,\ N. \quad (14)$$

For this selection, the maximum number of levels of output voltage and the maximum output voltage can be determined by the following equations, respectively:

$$N_L = 4N - 1 \quad (15)$$

$$V_{o,Max} = (2N - 1)V_{dc}. \quad (16)$$

B. Second Proposed Selection

In the second proposed selection for an asymmetric multilevel inverter, the values of the dc voltage sources are chosen according to the following equations:

$$V_{dc,1} = V_{dc} \quad (17)$$

$$V_{dc,j} = 3V_{dc} \qquad j = 2,\ 3,\ 4,\ \cdots,\ N. \quad (18)$$

For this selection, the maximum number of output voltage levels and the maximum output voltage can be obtained as follows:

$$N_L = 6N - 3 \quad (19)$$

$$V_{o,Max} = (3N - 2)V_{dc}. \quad (20)$$

When compared with the first proposed selection, the second proposed selection generates a lot more output voltage levels and the maximum output voltage increases considerably. It is worth noting that the proposed selections can produce any number of output voltage levels (even and odd).

As a result of the proposed selections for the values of the dc voltage sources, the charge balance control methods can be applied to asymmetric multilevel inverters. In other words, the proposed selections enable the charge balance control methods to be applied to asymmetric multilevel inverters. This is discussed further in Section V.

IV. Charge Balance Control Methods for Symmetric Cascaded Multilevel Inverters

The simplest way to control a multilevel inverter is the fundamental frequency switching control. In this control method, each switching device needs only to be switched one time per fundamental cycle, which results in low switching losses and low electromagnetic interference. With N CHB cells, a multilevel inverter under staircase modulation has N arbitrary switching angles for synthesizing the output voltage waveform [25], [28].

Fig. 2 shows three different switching patterns for a 7-level symmetric CHB multilevel inverter, where $v_{o,1}$, $v_{o,2}$ and $v_{o,3}$ represent the output voltages of the first, second and third H-bridges, as shown in Fig. 1. Considering the symmetry of the waveform, there are only three switching angles that need to be determined. These switching angles are θ_1, θ_2 and θ_3, as shown in Fig. 2. It can be seen that $\theta_1' = \pi - \theta_1$, $\theta_2' = \pi - \theta_2$ and $\theta_3' = \pi - \theta_3$. It is important to note that the calculation of the optimal switching angles for different goals, such as the elimination of selected harmonics and the minimization of total harmonic distortion (THD), is not the objective of this work.

Fig. 2(b) shows the waveforms and duty cycles of the different H-bridges that are used for providing a 7-level symmetric inverter. This inverter consists of three H-bridge cells. Each cell has a separated dc voltage source with a magnitudes of V_{dc}. Using this switching strategy, for example, on a motor drive continuously, the third H-bridge dc voltage source is cycled on for a much longer duration than the first H-bridge dc voltage source. This means that the third H-bridge dc voltage source will discharge much sooner than the first H-bridge dc voltage source. In other words, according to the control method shown in Fig. 2(b), the duty cycle for each of the dc voltage sources is different. As a result, the power drawn from different voltage sources vary as a function of the modulation level. This means that at different operation times, various powers are obtained from the dc voltage sources. Therefore, the power injected by the sources located in the bridges varies with time and consequently the dc voltage sources will have different charges. As a result, the lifetime of the different dc voltage sources will not be equal. It is necessary to mention that the discussions in this section can be developed for N bridges in a cascaded multilevel inverter.

In order to overcome the aforementioned problems, different methods are proposed. One such method is shown in Fig. 2(c). This method is called the full-wave charge balance control method. In this method, by rotating $\alpha_1 - \alpha_3$ pulses every cycle among the three H-bridges, all of the dc voltage sources are

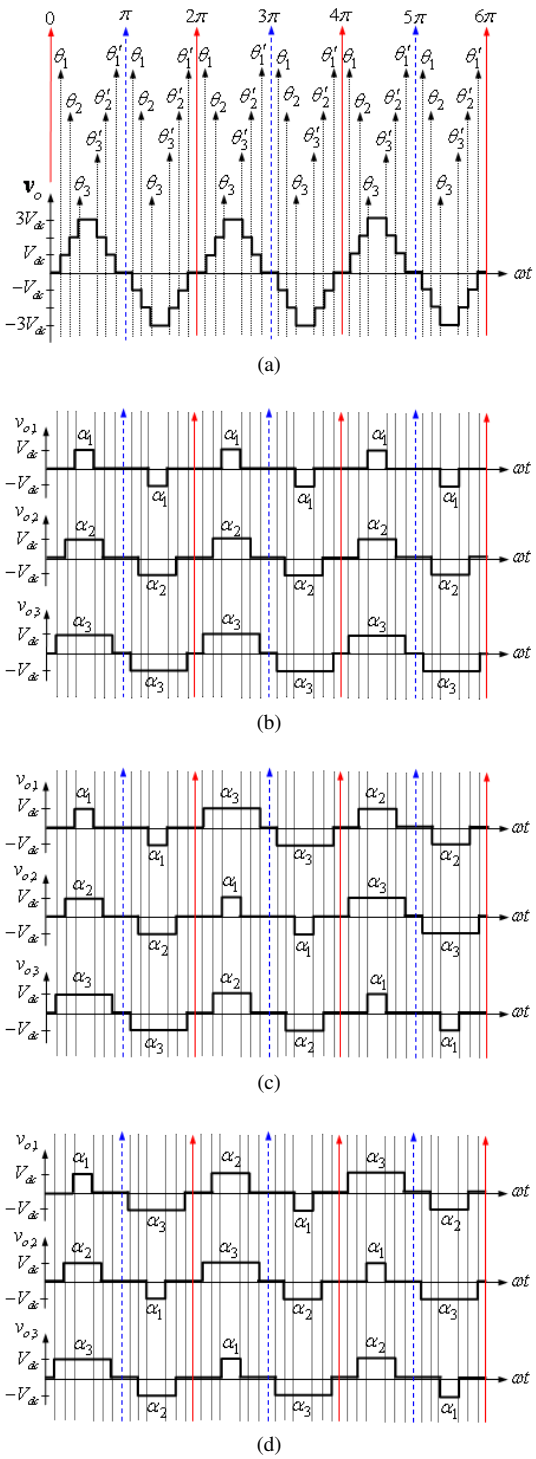

Fig. 2. Fundamental frequency switching controls for 7-level symmetric inverter. (a) Output voltage. (b) Conventional fundamental frequency control method. (c) Conventional full-wave charge balance control method. (d) Conventional half-wave charge balance control method.

equally discharged and balanced over three cycles. $\alpha_1 - \alpha_3$ are as follows:

$$\begin{aligned} \alpha_1 &= \theta_3' - \theta_3 \\ \alpha_2 &= \theta_2' - \theta_2 \\ \alpha_3 &= \theta_1' - \theta_1 \end{aligned} \tag{21}$$

The second control method for dc power balancing is shown in 2(d). This method is called the half-wave charge balance control method. According to this method, the rotation of $\alpha_1 - \alpha_3$ pulses is accomplished every half cycle instead of every full cycle.

By extending these methods to N_L-level inverters, the duty cycles of $(N_L-1)/2$ different H-bridges are equally discharged and balanced over all of the N_L cycles where it is necessary to have only $(N_L-1)/2$ H-bridges. These methods guarantee that the net powers drawn from different dc sources are equal and hence their voltages are constant. Therefore, the lifetime of the dc voltage sources that exist in different bridges is equalized. As a result, the charging or substitution time of the dc sources is reduced which leads to a reduction in the maintenance cost of the inverter. From (3) and (4), the average dc power supplied by the k-th H-bridge over a certain period can be calculated as:

$$P_{dc,k} = \frac{1}{T'} \int_o^{T'} v_{o,k} \cdot i_{dc,k} dt \tag{22}$$

where T' is the time duration necessary to accomplish the balancing methods.

Charge balance control methods, in general, are applicable to inverters with an even or an odd number of levels.

V. Development of the Charge Balance Control Methods for the Proposed Asymmetric Multilevel Inverters

It can be seen that the charge balance control methods cannot be applied to conventional asymmetric multilevel inverters. However, these methods are applicable to the proposed asymmetric multilevel inverters except for their first H-bridge.

Fig. 3 shows the two developed charge balance control methods for an asymmetric 15-level inverter according to the first proposed selection that was introduced in section III for determination of the dc voltage values. It is important to note that the proposed 15-level inverter consists of four H-bridge cells. The magnitudes of the dc voltage sources are V_{dc}, $2V_{dc}$, $2V_{dc}$ and $2V_{dc}$, respectively.

In the control methods shown in Figs. 3(b) and 3(c), the charge balancing is achieved by rotating $\alpha_2 - \alpha_4$ pulses every full (Fig. 3(b)) or half (Fig. 3(c)) cycle among the three H-bridges (H-bridges of 2, 3, and 4). As a result, all of the dc voltage sources, except for the dc voltage source used in the first H-bridge, become equally discharged and balanced over three cycles. The proposed strategies can be developed for multilevel inverters with N cascaded H-bridges. For the second proposed selection for an asymmetric multilevel inverter, the balancing method is similar to that of the first proposed selection. However, there is a difference in the switching function of the first H-bridge. Unlike the first proposed selection, in the second proposed selection, it is required that the first H-bridge produce a negative output voltage in the positive half cycle and a positive output voltage in the negative half cycle at specific intervals. This is necessary for the production of all of the possible output voltage levels. For example, when an output voltage level of $2V_{dc}$ is required, the first H-bridge should produce $-V_{dc}$ and one of the other H-bridges should generate $3V_{dc}$.

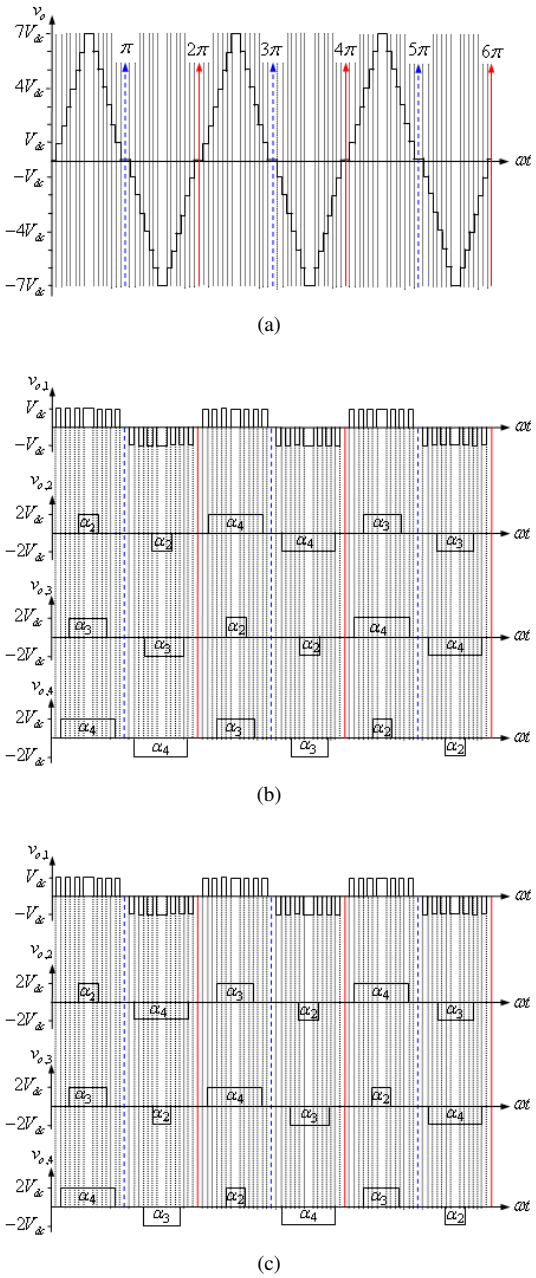

Fig. 3. Fundamental frequency switching controls for 15-level asymmetric inverter based on the first proposed selection. (a) Output voltage. (b) Proposed full-wave charge balance control method. (c) Proposed half-wave charge balance control method.

VI. Comparison of the Proposed Asymmetric Multilevel Inverters With The Conventional Topologies

Table II summarizes the number of levels, switches (N_S), and dc voltage sources as well as the maximum available output voltages for the conventional and proposed cascaded multilevel inverters when all of the inverters have an equal number of H-bridge cells. The number of output voltage levels in conventional CHB binary and trinary multilevel inverters is more than that of the proposed asymmetric multilevel inverters. However, in conventional binary and trinary CHB multilevel inverters the dc voltage sources have different values. This leads to a higher cost and a more complicated design. Moreover, it is not possible to apply charge balance control methods to them. The proposed asymmetric multilevel inverters use only two different values for whole the inverter and produce a lot more output levels than conventional symmetric inverters and the charge balance control methods are easily applied to them. In addition, the design cost of the proposed inverter decreases due to the similarity of H-bridges in all of the different H-bridge cells except the for first H-bridge cell.

TABLE II
Comparison Of Cascaded Multilevel Inverters

	Symmetric inverters	Asymmetric inverters			
		Binary	Trinary	Proposed	
				First proposed selection	Second proposed selection
N_L	$2N+1$	$2^{N+1}-1$	3^N	$4N-1$	$6N-3$
Number of dc sources	N	N	N	N	N
N_S	$4N$	$4N$	$4N$	$4N$	$4N$
$V_{o,Max}$	NV_{dc}	$(2^N-1)V_{dc}$	$\left(\frac{3^N-1}{2}\right)V_{dc}$	$(2N-1)V_{dc}$	$(3N-2)V_{dc}$
Charge balance possibility	Possible	Not possible	Not possible	Possible	Possible
Switches design cost	Low	High	High	Low	Low

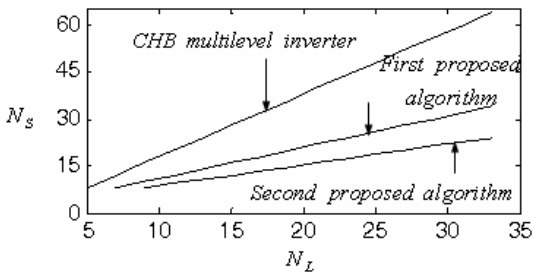

Fig. 4. Number of output voltage levels (N_L) versus number of switches (N_S) in the symmetric and the proposed asymmetric multilevel inverters.

Fig. 4 compares the number of switches required for a given number of output voltage levels for conventional symmetric and the proposed asymmetric multilevel inverters with the same number of H-bridges. The proposed asymmetric multilevel inverters combine the good modularity characteristic of symmetric multilevel inverters with the high number of output voltage levels of asymmetric multilevel inverters. Therefore, the proposed asymmetric multilevel inverters have a higher number of output voltage levels while having good modularity, which makes it possible to apply the charge balance control methods.

VII. Simulation and Experimental Results

In this section, the simulation and experimental results are presented to verify the validity and practicality of the proposed selections and the charge balance control methods. The simulations have been carried out using PSCAD/EMTDC software. In all of the simulations, the switches are considered to be ideal.

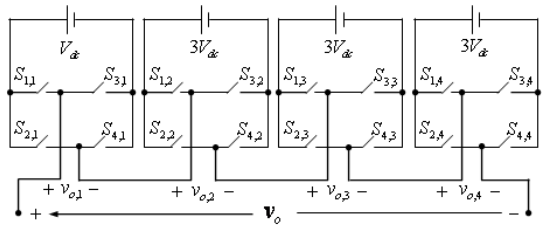

Fig. 5. Single-phase 21-level asymmetric multilevel inverter based on the second proposed selection.

A laboratory prototype based on the second proposed selection is implemented and tested. The laboratory setup is a single-phase 21-level inverter, as shown in Fig. 5. The inverter consists of four H-bridges. This multilevel inverter can produce maximum output voltage of $10V_{dc}$.

All of the IGBTs of the prototype are a BUP306D with internal anti-parallel diodes. A 89C52 microcontroller from the ATMEL Company has been used to generate the switching patterns according to the proposed switching strategies.

In the simulations and in the experimental prototype, the value of the first dc source is $V_{dc} = 10V$. The equation of the desired output voltage is considered to be $100\sin 100\pi t$. The load is an inductive load ($R = 20\Omega$ and $L = 55mH$). The conventional and the two proposed charge balance control methods (i.e. full-wave and half-wave, from Fig. 3) have been applied to the proposed asymmetric multilevel inverter.

Fig. 6 shows the simulation and experimental results for a 21-level inverter under the conventional control method (as shown in Fig. 2(b)). Fig. 6(a) shows the waveforms of the output voltage and the current. Comparing the current waveform with the voltage waveform shows that the current waveform is closer to a sinusoidal waveform. This is due to the application of a resistive-inductive load, which behaves as a low-pass filter. Considering the above comparison, it is obvious that there is a phase difference between the fundamental component of the output voltage and the current waveforms, which is due to the inductive characteristics of the load. The output voltages of the different bridges of the converter using the conventional control method are illustrated in Figs. 6(b) and 6(c). The output waveform of each bridge is in a pulse waveform in such a way that the sums of the output waveforms of the different bridges generate a semi-sinusoidal waveform at the load side. As shown in Figs. 6(b) and 6(c), the widths of the generated output voltage pulses are different form one bridge to another. Considering that the bridges are series connected, their current is equal. However, the time intervals during which the dc voltage sources in different bridges are delivering power are different. Therefore, the energy extracted from the dc voltage sources of the different bridges differs. Consequently, the dc voltage sources of the different bridges possess different charges and their lifetimes are not the same. For example, among the second, third and fourth H-bridges, the forth H-bridge gives the least energy in every cycle.

In the case of both charge balance control methods, the load voltage, the load current and the first H-bridge output voltage waveforms are the same as the waveforms of the conventional control method (Fig. 6(a)). Therefore, they are not repeated in the following results. However, the output voltage waveforms of the different bridges differ from each other. For the full-wave and half-wave charge balance control methods, the output voltage waveforms of the different bridges are illustrated in Figs. 7 and 8, respectively. It is important to mention that the charge balance control methods are not applicable to the first bridge. The charge balance control methods have been applied to balance the energy extracted from the second, third and fourth bridges. As shown in Figs. 7 and 8, the output voltages of the second, third and fourth bridges are substituted between these bridges in a way that their operation periods (the time that they are delivering power) are equalized after three fundamental cycles. The charge balance control methods can be imagined as replacing the dc voltage sources with each other so that each of them will experience the same conditions after three cycles. As a result, the dc voltage sources used in the three bridges are charged and discharged equally, and their lifetime will be similar if their initial charges are equal. It is necessary to mention that the operation period of the dc voltage source used in the first bridge differs from others in both of the charge balance control methods. Therefore, the charge balance control methods are not applicable to the first bridge. As the results show, the proposed selections and control methods can produce the desired number of output voltage levels and a balance between the dc sources is provided. The figures also show good agreement between the simulation and experimental results. It is important to note that there is a small difference between the amplitudes of the simulation and experimental results due to voltage drops on the switches of the prototype.

TABLE III
COMPARISON OF DC BUS POWER IN CONVENTIONAL AND CHARGE BALANCE CONTROL METHODS IN 21-LEVEL INVERTER

	dc bus power [W]			
	First H-bridge	Second H-bridge	Third H-bridge	Fourth H-bridge
Conventional method	11.8W	55.8W	49.7W	33.3W
Charge balance control methods	11.8W	46.3W	46.3W	46.3W

Table III shows a comparison of dc bus power in the conventional and the charge balance control methods based on the experimental results for the proposed asymmetric cascaded multilevel inverter. As can be seen in Table III, in the conventional control method, the supplied powers of the dc voltage sources are different from one another. However, in the charge balance control methods the supplied powers of the different dc voltage sources are equal except for the first H-bridge.

VIII. CONCLUSION

In this paper, two new selections for the determination of the values of the dc voltage sources for asymmetric cascaded multilevel inverters have been proposed. In addition, two modulation strategies have been proposed for dc power balance realization for the proposed asymmetric multilevel inverters. These modulation strategies will increase the lifetime of the dc sources. In addition, the number of charging and substitution times of the dc sources is decreased, which can lead to a reduction of the inverter maintenance costs. For multilevel

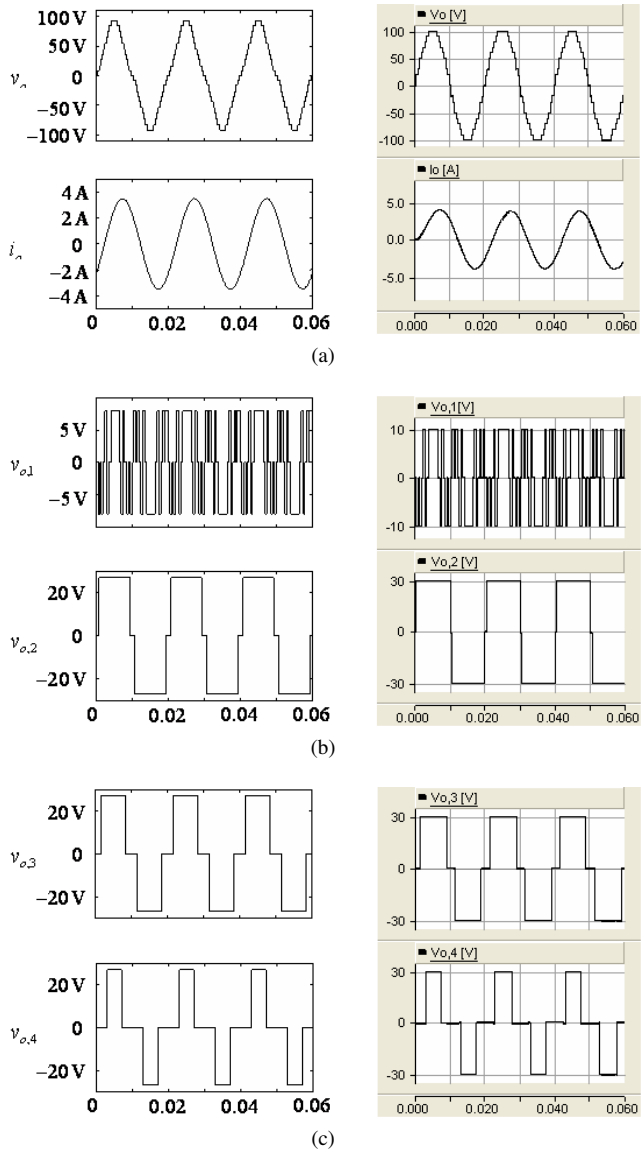

Fig. 6. Simulation and experimental results (horizontal axis is time [sec]) for conventional control method; right column: simulation results; left column: experimental results. (a) Output voltage and current. (b) First and second H-bridges output voltages. (c) Third and fourth H-bridge output voltages.

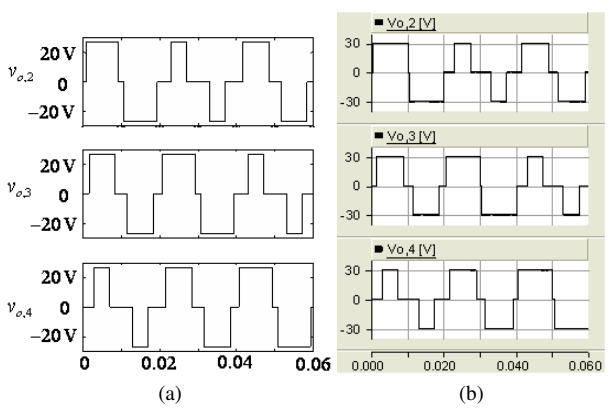

Fig. 7. Results for full-wave charge balance control method. (a) Experimental results. (b) Simulation results.

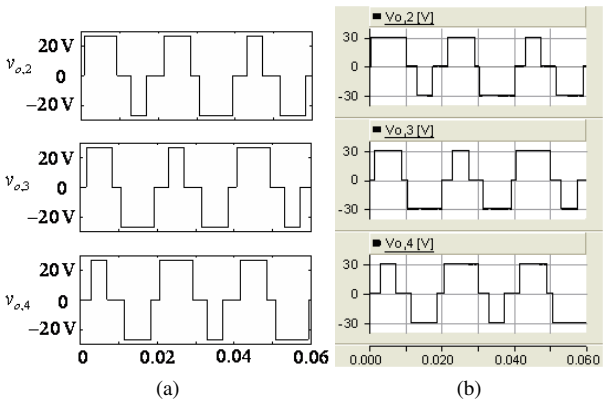

Fig. 8. Results for half-wave charge balance control method. (a) Experimental results. (b) Simulation results.

inverters with N H-bridge cells, all of the dc voltage sources except for the dc voltage source used in the first H-bridge become equally discharged and balanced over (N-1) cycles as a result of using the two charge balance control methods. Simulations and experimental results on a 21-level inverter prototype verify the theoretical analyses.

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