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Mathematical Analysis and Experiment Validation of Modular Multilevel Converters

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Abstract

This paper describes operating and capacitor voltage balancing of the modular multilevel converter. The paper focuses on sizing of the cell capacitor and establishes approximate expressions for the capacitor voltage. Simulations and experiments results obtained from three-level modular converter are used to demonstrate its viability in medium voltage applications. It is shown that the modular converter can operate over the full modulation index linear range independent of load power factor.

Key Words: Capacitor ripple and size, Modular Multilevel Converter, Sinusoidal Pulse width modulation

I. INTRODUCTION

The modular multilevel converter is proposed in [1]-[4]. It fulfills several requirements in medium voltage machine drives and HVDC applications. The topology overcomes the main disadvantages of the conventional multilevel converter and provides a set of attractive features [1], [5]-[10]:

- Modular construction.
- It is feasible to achieve capacitor balancing independent of the number of voltage levels generated and operating conditions.
- Low total harmonic distortion and switching devices experience low voltage stress.
- Failure management: protected all converter cells against mechanical destruction in case of a short circuit or insulation failure. Because of the realization of redundancy, a failed cell can be replaced by a redundant cell in the arm which gives more flexibility [11].
- Permits the use of a low cost interface transformer and harmonic filters can be eliminated, if the extendibility feature of the M2C is exploited.

This paper is organized as follows: Section II describes the operation principle and capacitor voltage balancing technique of the modular multilevel converter. Section III establishes approximate analytical expressions for the cell capacitor sizing and voltage. The simulation results in Section IV demonstrate the ability of the modular converter to operate independent of modulation index and load power factor. Section V uses experimental results to validation section IV. Section VI summarize the distinct features of the modular converter.

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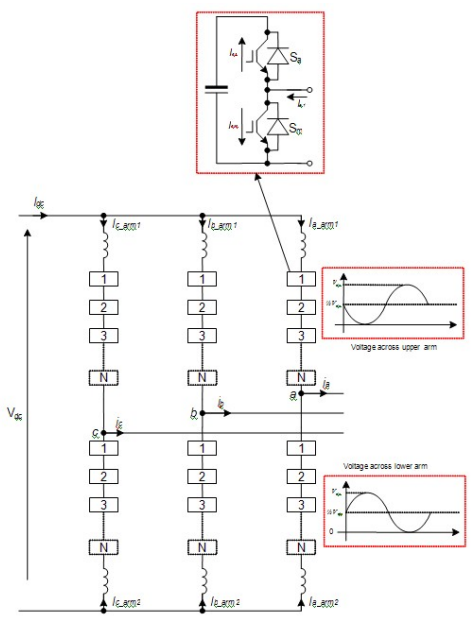


Fig. 1. Three phases of the N-level M2C.

II. THREE-LEVEL M2C

A. Operation Principle

Fig. 1 shows the three-phase modular converter with N cells per arm. Each converter phase generates N voltage levels at output phases a,b,c referred to the supply mid-point '0'.The voltage across each cell capacitor is $\frac{1}{N}V_{dc}$ and the voltage stress across each switching device is limited to one capacitor voltage. Arm inductance L limits the inrush and circulating currents between the phases that the converter switches may experience during the balancing process. Proper converter operation requires a robust capacitor voltage balancing strategy to ensure that the voltage across each switching device is controlled over the entire operating range [3, 6].

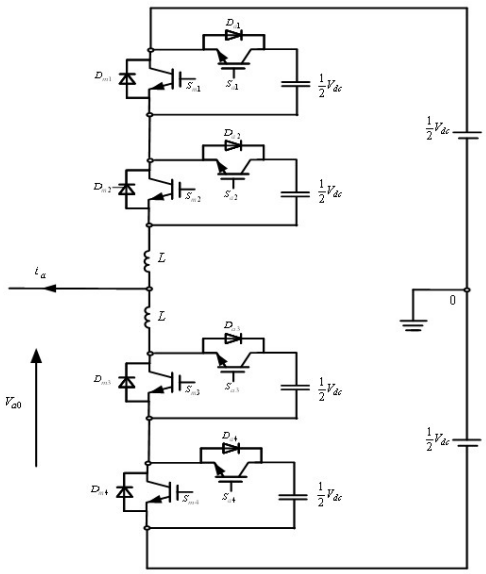


Fig. 2. Phase 'a' of a 3-level M2C.

Fig. 2 shows one phase of a three-level modular multilevel converter. Each cell consists of two switching devices. When the switch S_m is turned on and S_a is off, the output voltage is 0. When the switch S_a is turned on and S_m is off, the output voltage is V_{dc}. Two switches in each cell must be operated in a complementary manner. Each capacitor voltage in each cell must be maintained at $1/2V_{dc}$. The four main switches are $S_{m1}, S_{m2}, S_{m3}, S_{m4}$,and the four auxiliary switches are $S_{a1}, S_{a2}, S_{a3}, S_{a4}$ which make up four complementary switch pairs (S_{m1}, S_{a1}),(S_{m2}, S_{a2}),(S_{m3}, S_{a3}),(S_{m4}, S_{a4}). In the three-level converter, there are 3 output voltage states: 0, $\pm\frac{1}{2}V_{dc}$ Assuming the dc source midpoint as the output voltage reference, there are six switch combinations that synthesize three output voltage levels.

For voltage level $V_{a0} = \frac{1}{2}V_{dc}$, S_{m1}, S_{m2} from the upper arm and S_{a3}, S_{a4} from the lower arm, are on.

For voltage level $V_{a0} = 0$, the four switch combinations are:

S_{m1}, S_{m3} and S_{a2}, S_{a4} on
S_{m2}, S_{m3} and S_{a1}, S_{a4} on
S_{m2}, S_{m4} and S_{a1}, S_{a3} on
S_{m1}, S_{m4} and S_{a2}, S_{a3} on

For voltage level $V_{a0} = -\frac{1}{2}V_{dc}$, S_{a1}, S_{a2} from the upper arm and S_{m3}, S_{m4} from the lower arm, are on.

B. Sinusoidal Pulse Width Modulation

With regard to the modular and scalable topology, the applied modulation scheme should be expandable to any voltage level number. Therefore, a carrier-basis is used to control the switching states in this paper. By using phase disposition (PD) carrier strategy, *n*-level MMC needs (*n*-1) triangular carrier, and they are displayed with same frequency and same amplitude from 1 to -1. A sinusoidal reference wave (with triplens if desired) is then compared to these triangular waveforms and according to the results the gate signal to each IGBT is controlled [3], [4].

Fig. 3 shows 2 triangular carrier waveforms and one sinusoidal reference waveform, and when the reference signal is

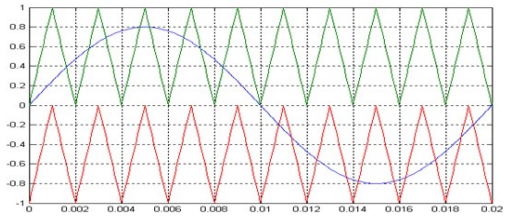


Fig. 3. Carrier and reference waveforms for 3-level M2C.

greater than the upper triangular signal the output voltage level equals $1/2V_{dc}$, when the reference signal is less than the lower triangular signal, the output voltage level equals $-1/2V_{dc}$. The last condition is voltage level 0 which can be generated by 4 different conditions.

C. Capacitor Balancing for 3-level MMC

To ensure cell capacitors and switching devices experience equal voltage stress the following capacitor voltage balancing algorithm is applied[3], [11]:

i. The capacitors voltages are measured periodically, and the upper group and lower group are sorted in ascending order.
ii. During positive load current, select a switch state that charges one upper capacitor with the minimum voltage and discharges one lower capacitor with the maximum voltage.
iii. During negative load current, select a switch state that charges one upper capacitor with the maximum voltage and discharges one lower capacitor with the minimum voltage.

By this method, the voltage balance of the cell capacitors is maintained.

III. Capactior Size, Ripple

A. Calculation of Capacitance

Modular multilevel converter upper and lower arm voltages of the same phase leg can be expressed as:

$$V_{arm1}(t) = \tfrac{1}{2}V_{dc}(1 - m\sin\omega t) \tag{1}$$

$$V_{arm2}(t) = \tfrac{1}{2}V_{dc}(1 + m\sin\omega t) \tag{2}$$

where V_{dc}, m, and ωrepresent total converter dc link voltage, modulation index and output voltage fundamental frequency in rad/s respectively. Assume the converter is lossless; the power balance equation can be expressed as:

$$P_{dc} = V_{dc}I_{dc} = 3 \times \tfrac{1}{2}V_m I_m \cos\varphi = P_{ac\_3\phi}. \tag{3}$$

Since for sinusoidal pulse with modulation, $V_m = 1/2mV_{dc}$, the dc component per arm is:

$$\tfrac{1}{3}I_{dc} = \tfrac{1}{4}mI_m\cos\varphi \tag{4}$$

where phase current $i_a = I_m\sin(\omega t - \varphi)$. Thus, the arm current of the phase 'a' can be expressed as:

$$I_{arm1} = \tfrac{1}{3}I_{dc} + \tfrac{1}{2}i_a. \tag{5}$$

Combining equations (4) and (5), the arm current can be expressed as:

$$I_{arm1} = \tfrac{1}{3} I_{dc} \left[1 + \frac{2}{m\cos\varphi} \sin(\omega t - \varphi) \right]. \quad (6)$$

Let $q = \frac{2}{m\cos\varphi}$, equation (6) can be rewritten as:

$$I_{arm1} = \tfrac{1}{3} I_{dc} \left[1 + q\sin(\omega t - \varphi) \right]. \quad (7)$$

For cell capacitance sizing, assume all the converter six arms contribute equal power. Therefore the instantaneous power the upper arm exchanges with the ac side is:

$$P_{arm1} = \tfrac{1}{2} V_{dc}(1 - m\sin\omega t) \times \tfrac{1}{3} I_{dc}(1 + q\sin(\omega t - \varphi)) \quad (8)$$

The average power the upper arm exchanges with the ac side over the full fundamental cycle is:

$$\bar{P}_{arm1} = \frac{1}{2\pi} \int_0^{2\pi} \tfrac{1}{2} V_{dc}(1 - m\sin\omega t) \times \tfrac{1}{3} I_{dc}(1 - q\sin(\omega t - \varphi)) d\omega t$$
$$= \tfrac{1}{6} P_{dc}(1 - \tfrac{1}{2} qm\cos\varphi). \quad (9)$$

By substituting $q = \frac{2}{m\cos\varphi}$ in equation (9), it reduces to zero. This demonstrates the natural balancing of the modular converter cell capacitors if they are rotated and modulated correctly. For cell capacitance sizing of the modular converter with N cells per arm, it can be assumed that each cell only operates for $2\pi/N$. Therefore, the energy each cell capacitor exchanges with the ac side can be expressed as:

$$W_c = \frac{1}{\omega} \int_0^{\frac{2\pi}{N}} \tfrac{1}{2} V_{dc}(1 - m\sin\omega t) \times \tfrac{1}{3} I_{dc}(1 - q\sin(\omega t - \varphi)) d\omega t$$
$$= \tfrac{1}{6} P_{dc} \left[\begin{array}{l} q\left\{\cos\varphi - \cos(\frac{2\pi}{N} - \varphi)\right\} + M\left\{\cos\frac{2\pi}{N} - 1\right\} + \\ \frac{1}{4} qm\left\{\sin\varphi + \sin(\frac{4\pi}{N} - \varphi)\right\} \end{array} \right]. \quad (10)$$

For three-level modular converter, N=2, therefore equation (10) reduces to (11).

$$W_c = \tfrac{1}{3} P_{dc} \frac{(2 - m^2)}{\omega m}. \quad (11)$$

Assume the cell capacitor maximum and minimum voltages are V_{cmax} and V_{cmin}, the pulsating energy each cell capacitor exchanges with ac side is:

$$W_c = \tfrac{1}{2} C \left(V_{c\max}^2 - V_{c\min}^2 \right) = C \left(V_{c\max} - V_{c\min} \right) \tfrac{1}{2} \left(V_{c\max} + V_{c\min} \right)$$
$$= C \Delta V_{\max} \bar{V}_c. \quad (12)$$

where C is cell capacitance, ΔV_{max} is the maximum allowable voltage ripple, and $\bar{V}_c$is average cell voltage. By equating equations (10) and (11), the cell capacitance is:

$$C = \frac{P_{dc}(2 - m^2)}{3\omega m \Delta V_{\max} \bar{V}_c} \quad (13)$$

Assuming $\bar{V}_c = \frac{1}{2} V_{dc}$ and $\xi = \frac{\Delta V_{c\max}}{\bar{V}_c}$(percentage voltage ripple), equation (13) can be rewritten as:

$$C = \frac{P_{dc}(2 - m^2)}{3\omega m \xi \bar{V}_c^2} = \frac{4P_{dc}(2 - m^2)}{3\omega m \xi V_{dc}^2}. \quad (14)$$

From equation (14), the converter is design to operate at high modulation indices requiring relatively small cell capacitance compared to those designed to operate at low modulation indices. Also, the lower the cell voltage the larger the cell capacitance. For example, a 20kV, 20MW converter, the cell capacitance required such that the voltage does not exceed 5% when operated at 0.9 modulation index is:

$$C = \frac{20 \times 10^6 \times (2 - 0.9)}{3 \times 2\pi \times 50 \times 0.9 \times 0.05 \times (10 \times 10^3)^2} \approx 5mF$$

B. Capacitor Ripple Analysis

The modular multilevel converter cell capacitors experience relatively high voltage due to the flow of the fundamental current component through the capacitors. Therefore, the capacitors are required to store more energy compared to that of two-level and neutral-point clamped converters in order to maintain the voltage ripple across the cell capacitors within acceptable limits. The cell capacitor voltage can be expressed using a switching function. If the phase current is assumed constant within each switching cycle, the switching function can be replaced by device duty cycle. For the three-level modular multilevel converter controlled using sinusoidal pulse modulation (SPWM) for instance, when $0 \leq \omega t \leq \pi$, the time at voltage level $+\frac{1}{2} V_{dc}$ is $T_c m \sin\omega t$and time at the 0 voltage level is $T_c(1 - m\sin\omega t)$ In the negative half cycle, the time at voltage level $-\frac{1}{2} V_{dc}$ is$-T_c m\sin\omega t$ and the time at the '0' voltage level is$T_c(1 + m\sin\omega t)$. Output voltage levels $+\frac{1}{2} V_{dc}$ and $-\frac{1}{2} V_{dc}$ do not affect the state of charge of the cell capacitors. Only switch combinations that connect the output phase to the '0' voltage level affect the state of charge of the cell capacitors. The time at the 0 voltage level is distributed equally between the cells capacitors, assuming the capacitor voltage balancing strategy that uses redundant switch states is ideal, and uses these capacitors for an equal period of time over the full fundamental cycle. So, an expression for capacitor voltage can be based on one capacitor. The average current flowing through the capacitor in each cell can be expressed by:

$$\bar{i}_{sa} = \tfrac{1}{2}(1 - m\sin\omega t) i_{a1} \quad (15)$$

$$\bar{i}_{sm} = \tfrac{1}{2}(1 + m\sin\omega t) i_{a1} \quad (16)$$

where i_{a1} is the converter upper arm current which is the same as I_{a_arm1}, $\bar{i}_{sa}$ is the average current of the auxiliary switch s_a (the same as the capacitor current), and $\bar{i}_{sm}$ is the main switch average current. Therefore, the voltage across each cell capacitor can be related to the local average current that flows through the cell capacitor:

$$C \frac{dv_c}{dt} = \bar{i}_{sa} \quad (17)$$

Therefore, the voltage cross the capacitor C is:

$$v_c(\omega t) = \frac{1}{\omega C} \int [\tfrac{1}{2}(1 - m\sin\omega t)(\tfrac{1}{3} I_{dc} + I_a \sin(\omega t + \varphi))] d\omega t$$
$$= \frac{1}{\omega C} [\tfrac{1}{6} I_{dc} m\cos\omega t - \tfrac{1}{4} I_a \cos(\omega t + \varphi) \quad (18)$$
$$+ \tfrac{1}{8} I_a \sin(2\omega t + \varphi)] + A.$$

If the capacitor initial voltage is $\frac{1}{2} V_{dc}$, the constant A is:

$$A = \tfrac{1}{2} V_{dc} - \frac{1}{\omega C} (\tfrac{1}{8} m^2 I_a \cos\varphi - \tfrac{1}{2} I_a \cos\varphi - \tfrac{1}{8} m I_a \sin\varphi). \quad (19)$$

Finally, the voltage across each cell capacitor $C$is:

$$v_c(\omega t) = \tfrac{1}{2}V_{dc} + \frac{I_a}{\omega C}[\tfrac{1}{8}m^2\cos\varphi\cos\omega t - \tfrac{1}{8}m^2\cos\varphi + \tfrac{1}{8}m\sin(2\omega t+\varphi) - \tfrac{1}{2}\cos(\omega t+\varphi) - \tfrac{1}{2}\cos\varphi + \tfrac{1}{8}m\sin\varphi]. \quad (20)$$

The first term of the equation (20) represents the desired settling point of the capacitor voltage, while the remaining terms represent the ripple voltage which depend on cell capacitance, load power factor, modulation index, and phase current magnitude.

IV. Simulation Results

To illustrate the ability of the modular multilevel converter to operate independent of load power factor and modulation index, the three-level modular converter in Fig. 2 is simulated under the operating conditions shown in table I, and the results obtained are shown in Figs. 4.

Fig. 4 shows the simulation results obtained when the converter is operated at 0.9 modulation index and 0.88 power factor lagging. From the output voltage waveforms in Figs. 4a and 4b, the spectrum of line voltage in Fig. 4(c) shows that the modular converter generates high quality output voltage with relatively low harmonic content and low *dv/dt* (principle of minimum switching losses, one voltage level per switching cycle is maintained). Fig. 4(d) shows that the modular converter produces high quality load current even at high power factors, utilizing it arm inductances as low pass filters.

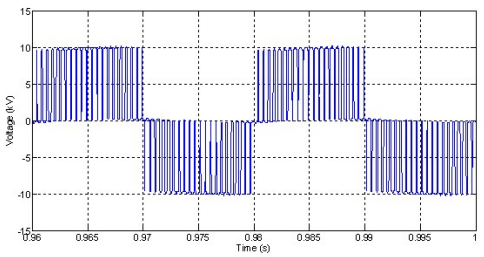
The initial value of cell capacitor of each arm are different, two upper arm capacitors are set to be 12kV, two lower arm capacitors are set to be 8kV.The results in Figs. 4(e), 4(f) and 4(g) show that the voltages across the cell capacitors of the three-level modular converter are maintained around the desire set-point after taking nearly 1 second to balance, viz. $\frac{1}{2}V_{dc}$. Fig. 4(h) shows phase current and its associated upper and lower arm currents. Despite the phase current being sinusoidal and dc offset free, the arm currents contain dc offset proportional to the peak phase current, load power factor and modulation index. This adds to the on-state losses of the modular converter compared to conventional multilevel converters such two-level and neutral-point clamped converters. Unlike the conventional voltage source converters with discontinuous arm current, the arm current of the modular converter is continuous as shown in Fig. 4(h). This may eliminate the need for dc side filters in applications such STATCOM or HVDC converters as the emitted audible noise is extremely low (but this is true only with a large number of cells per arm). Fig. 4(i) shows the current waveforms of two complementary switches of one M2C cell. The switching frequency per device under this operation condition is less than half the carrier frequency and the equivalent switching frequency on the output phase voltage is the same as carrier frequency. With an increased number of cells per arm, the switching frequency per device is expected to be reduced considerably.

V. Experiment Results

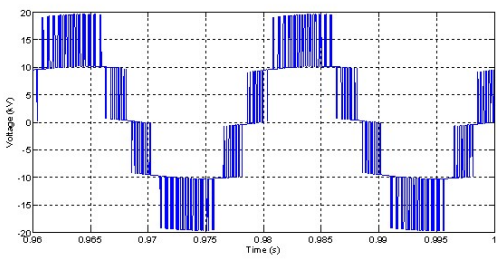
This section provides experimental validation of the analysis and simulation results presented in the paper. The practical

TABLE I
Simulation parameters

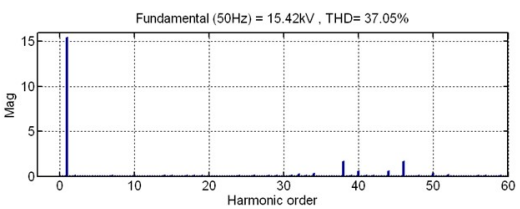
Converter rating	20MW
Modulation index	0.8
Load power factors	0.88 lagging
Capacitance	5mF
Switching frequency	2.1kHz
DC link voltage	20kV
Arm inductance	1mH



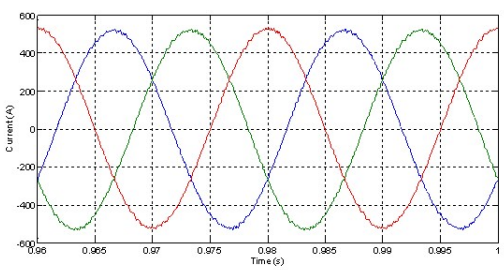
(a) Phase voltage referred to supply mid-point.



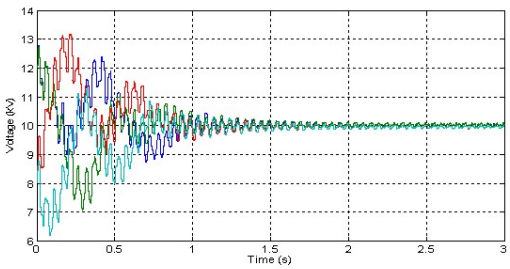
(b) Line-to-line voltage.



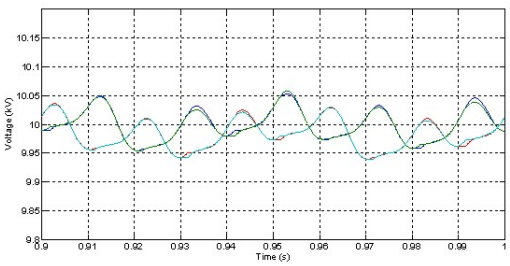
(c) Line voltage spectrum.



(d) Current waveforms.

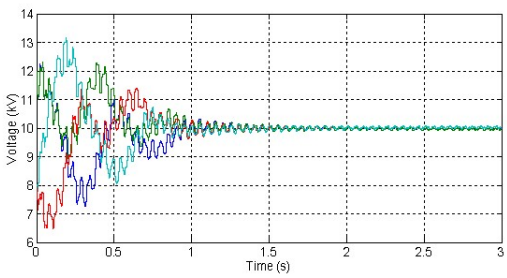


(i)

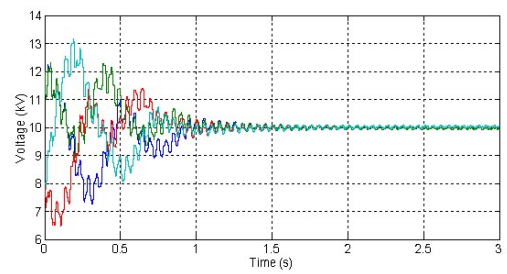


(ii)

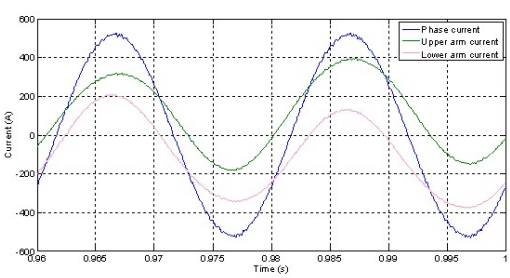
(e) Capacitor voltage of the phase a and (ii) expanded version of the capacitor voltage in. (i).



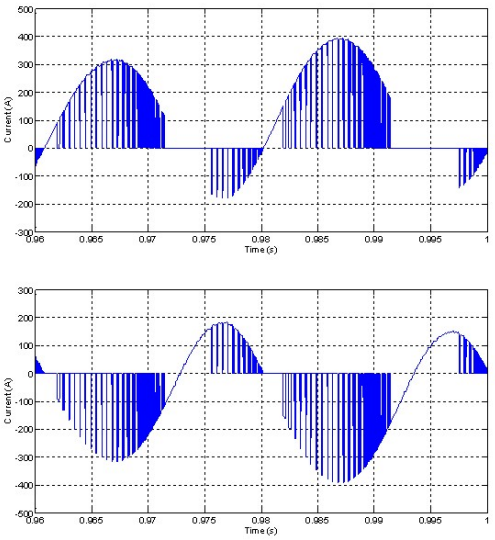
(f) Capacitor voltage of phase b.



(g) Capacitor voltage of phase c.



(h) Current in the upper and lower arm of phase a.



(i) Current waveforms in the main and complementary switches in one cell.

Fig. 4. Waveforms obtained when three-level modular converter is simulated when delivering 10MW the at 0.9 modulation index and 0.88 power factor lagging.

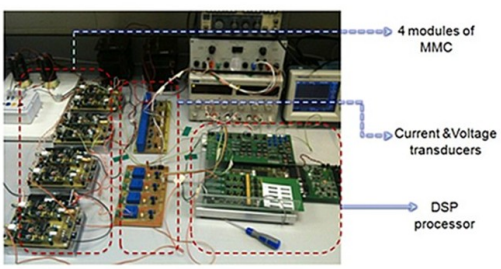
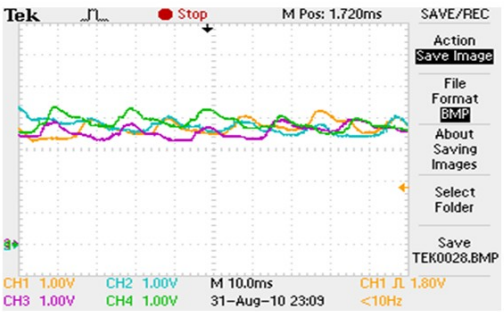


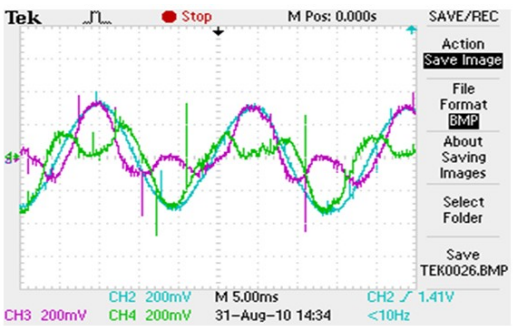
Fig. 5. Test rig for the 3-level modular converter.

results are obtained from one phase-leg of a prototype three-level modular converter with a 100V dc link voltage, 1mF cell capacitors, and arm inductance of 3mH (see Fig. 5). In this experiment, the converter is controlled using SPWM with a 2.1 kHz switching frequency. An Infineon Technology Tri-core microcontroller TC 1796 is used to program the modulation and capacitor voltage balancing strategy. Fig. 6 and Fig. 7 show the experimental results obtained at 0.72 power factor lagging and unity power factor. The converter is operated successfully in both cases and cell capacitor voltage balancing is maintained. From the phase voltage and current waveforms in Fig. 7(a) and 8(b), the modular converter with only two cells per arm produces high quality phase current, utilizing its upper and lower arm inductors as low-pass filters, as demonstrated in the simulations. From the current waveforms of devices S_a and S_m (Figs. 6(d) and 6(e)), these three-level modular switching devices operate at half the carrier frequency, as demonstrated in the simulation. This confirms the suitability of the modulation and capacitor voltage balancing method employed for high-voltage applications where the switching frequencies per device and semiconductor losses are restrictive factors. Even though the upper and lower arm currents include dc offset and distortion their sum remains sinusoidal and equal to the phase current.

(a) Load voltage and current (scale:5ms/div,100v/div, 1A/div).



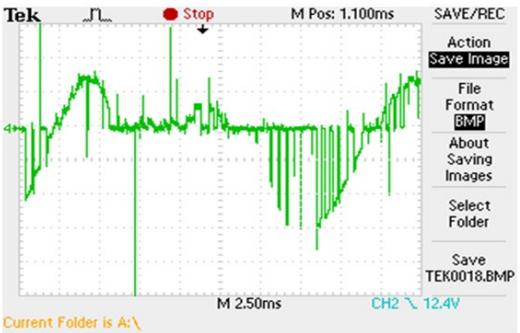
(b) Voltage across four cell capacitors of the phase-leg (scale: 10ms/div,10v/div).



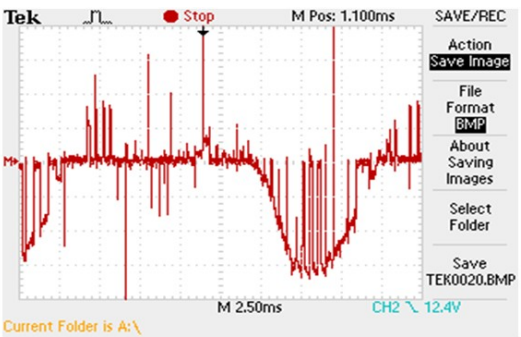
(c) Current in the upper and lower arms of the phase leg (scale: 5ms/div,1A/div).

VI. Conclusion

This paper analyzed the capacitor size and ripple of the modular multilevel converter when SPWM modulated, and also shows experimental validation of the analysis provided and demonstrates the advantages of the modulation and capacitor balancing strategy. As the M2C is the only multilevel converter able to exploit the full potential of multilevel modulation, it has been selected as representative of multilevel converters in this investigation. The results of this investigation show that the M2C is better in the following features: improved efficiency, lower voltage and current on the switching devices, extremely low *dv/dt* and audible noise resulted from small voltage steps and low switching frequency per device. These results confirm the suitability of the multilevel converter, such as the M2C, for medium and high-voltage applications, such as reactive power compensation, medium voltage drive systems, interface for renewable power plants using wind and solar energy, and high voltage dc transmission systems.

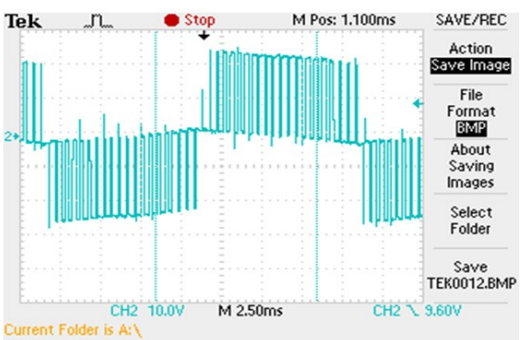


(d) Current in one device (IGBT and diode) of a cell. (scale: 2.5ms/div,1A/div).

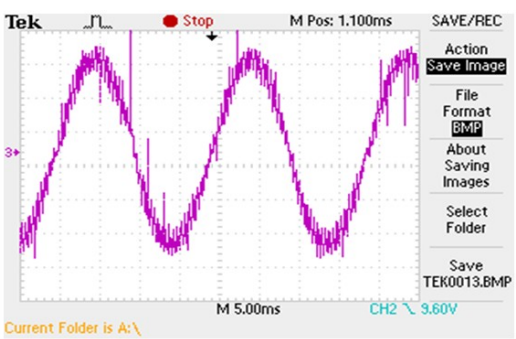


(e) Current in the other device (IGBT and diode) of a cell. (scale: 2.5ms/div,1A/div).

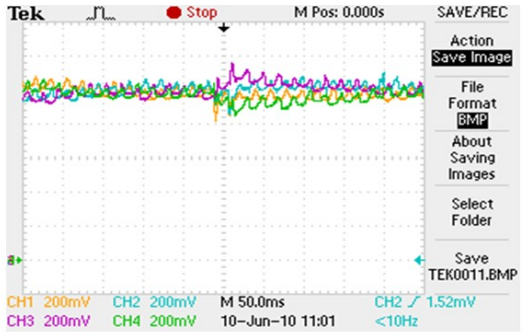
Fig. 6. Waveforms obtained from one-phase 3-level modular multilevel converter experiment at 0.9 modulation index and 0.72 power factor lagging.



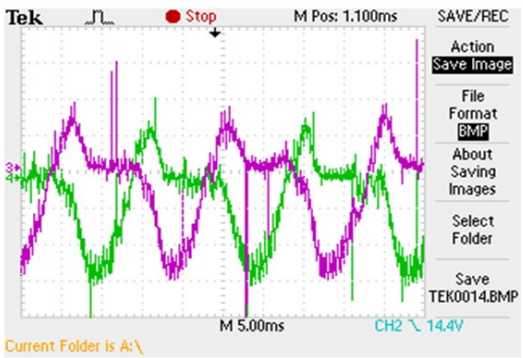
(a) Load voltage (scale:5ms/div,50v/div).



(b) Load current (scale:5ms/div,0.5Av/div).



(c) Voltage across four cell capacitors of the phase-leg (scale: 10ms/div,10v/div).



(d) Current in the upper and lower arms of the phase leg (scale: 5ms/div, 0.5A/div).

Fig. 7. Waveforms obtained from one-phase 3-level modular multilevel converter experiment at 0.8 modulation index and unity power factor.

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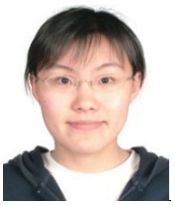

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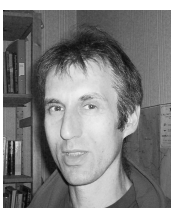

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