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Optimal Controller Design for Single-Phase PFC Rectifiers Using SPEA Multi-Objective Optimization

Ahmadreza Amirahmadi†, Ali Dastfan*, and Mohammadreza Rafiei**

†* Dept. of Electrical and Robotic Eng., Shahrood University of Technology, Shahrood, Iran
** Dept. of Electrical Eng., Islamic Azad University, Garmsar branch, Garmsar, Iran

Abstract

In this paper a new method for the design of a simple PI controller is presented and it has been applied in the control of a Boost based PFC rectifier. The Strength Pareto evolutionary algorithm, which is based on the Pareto Optimality concept, used in Game theory literature is implemented as a multi-objective optimization approach to gain a good transient response and a high quality input current. In the proposed method, the input current harmonics and the dynamic response have been assumed as objective functions, while the PI controller's gains of the PFC rectifier (Kpi, Tpi) are design variables. The proposed algorithm generates a set of optimal gains called a Pareto Set corresponding to a Pareto Front, which is a set of optimal results for the objective functions. All of the Pareto Front points are optimum, but according to the design priority objective function, each one can be selected. Simulation and experimental results are presented to prove the superiority of the proposed design methodology over other methods.

Key Words: Boost converter, Dynamic response, Game theory, Power-factor-correction rectifier, Strength Pareto Evolutionary Algorithm, Total Harmonic Distortion

I. INTRODUCTION

Power Factor Correction (PFC) Rectifiers based on Boost converters are one of the most popular topologies providing low input line harmonics in accordance with harmonic distortion standards. Control of this type of converter has received considerable attention in the past two decades. From the control point of view, the operation of a PFC rectifier can be regarded as a tracking problem, since the output voltage should follow the reference command with a good transient behavior and a low steady state error. Furthermore, the input current harmonics must remain low. Normally, a low input current distortion and a high input power factor are achieved by employing a high-bandwidth current control loop and a low bandwidth voltage control loop [1],[2]. The voltage loop is designed for low bandwidth to avoid the input current distortion caused by the output voltage ripple [3]. Such a rectifier system exhibits poor dynamic response with respect to input voltage and load disturbances [4]. In recent years, several techniques have been proposed to overcome this problem like the ripple compensation approach [5]-[12], which can be considered as two methods, compensation by use of a ripple estimator [5]-[7] or by use of a filter. The implementation of notch filters [8]-[10], dead zone ADC controllers [11] or comb filters [12] have been allowed with the help of digital controllers. The objective of these techniques is to increase the voltage loop crossover frequency by eliminating the second and higher harmonics ripples from the control signal. In another technique separate bandwidths for the steady state and transients has been considered [13]. The bandwidth of the voltage loop is kept low at the steady state to obtain a sinusoidal input current. During transients, it is increased to have a good dynamic response. The output voltage error is used to determine whether the rectifier is in the steady state or the transient condition. Although these methods improve the dynamic response of converters without an increase in the line current distortion, they significantly increase the complexity of the control circuit. Also, in digital implementation, the system requires large memory storage, and since the design of the new block is based on the converter model, these methods are sensitive to parameter variations.

Some control methods like feedforward control of the input voltage, load current, duty-ratio and reference current can improve the output dynamic response, but these methods require more sensors or quantity estimators [3],[4],[14]-[17].

Indirect current control of a PFC rectifier does not need to measure the input voltage and load current, so this is usually the basis for new control methods for PFC rectifiers.

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† Corresponding Author: amirahmadi@knights.ucf.edu
Tel: +1-407-683-6503, Shahrood University of Technology
* Dept. of Electrical and Robotic Eng., Shahrood University of Technology, Iran

In this method and in the resistance emulation method a proportional-integral (PI)-type voltage controller is used and all the modified methods take into consideration this part of the controller [4],[18]-[20]. In the indirect current control scheme, like the other control methods for a PFC rectifier, the input current quality and the dynamic response of the PFC rectifier are conflicting objectives. As a result, when one objective is imporoved, the other is degraded. In this case of simultaneous optimization, there is no single optimal solution, but a set of optimal solutions. These solutions are optimal in the wider sense that no other solutions in the search space are superior to them when all objectives are considered.

In this paper, the designing of a simple PI controller is proposed which is able to gain a good transient response as well as a high quality input current via a multi-objective optimization approach.

II. Multi-objective Optimization

The Game theory concept is applicable to a multi-objective optimization problem in its own original status without the need for modifying or combining the objectives, unlike other methodologies which combine the desired goals of the optimization problem, construct a scalar function and then use a common scalar optimization approach to resolve the problem [21]. The major problem with these methodologies, which are called plain aggregating approaches, is the unavailability of any straightforward method for combining the objectives or goals of the problem when they are not constant quantities. For experimental problems, the Game theory concept requires an evolutionary algorithm to solve MOPs because they process a set of solutions in parallel. One of the best EAs to reach globally optimum results is SPEA. This evolutionary algorithm covers all of the solutions which methods like Hajela's and Lin's Genetic Algorithm (HLGA) [22], Niched Pareto Genetic Algorithm (NPGA) [23], Vector Evaluated Genetic Algorithm (VEGA) [24], and Non-dominated Sorting Genetic Algorithm (NSGA) [25] offer and combines several of their features in a unique manner.

A simple mathematical definition of a multi-objective optimization problem can be considered as (1).

$$\begin{aligned} &Minimize \quad y = f(x) = (f_1(x), f_2(x), ..., f_k(x)) \\ &Subject \quad to \quad x = (x_1, x_2, ...x_n) \in X \\ &\& \quad y = (y_1, y_2, ...y_k) \in Y \end{aligned} \tag{1}$$

where x, X, y, and Y are the decision vector, parameter space, objective vector, and objective space, respectively.

Objective vectors that cannot be improved in one dimension without degradation in another are found, and their corresponding decision vectors are called solutions for a multi-objective optimization problem. To describe them mathematically, can be said that vector a dominate vector b if:

$$\begin{aligned} &\forall_i = \{1,2,...,k\} : f_i(a) \geq f_i(b) \\ &\exists_j \in \{1,2,...,k\} : f_j(a) > f_j(b) \end{aligned} \tag{2}$$

All decision vectors which are not dominated by any of the other decision vectors of a given set are called non-dominated. Every non-dominated solution is regarded as optimal in the sense of the Pareto Optimality concept or is called Pareto Optimal. Obviously, any Pareto Optimal solution is comparatively the most optimal one in terms of at least one of the objective functions.

The set of all non-dominated solutions is called the Pareto Optimal Set and the set of the corresponding values of the objective functions is called the Pareto Optimal Front [26].

A. Strength Pareto Evolutionary Algorithm (SPEA)

The SPEA because of its high diversity and fast convergence is one of the most popular evolutionary algorithms among similar approaches [26].

The flow of the algorithm can be summarized as following eight stages.

1– Randomize a prime population P within the allowed boundaries and consider an external non-dominated set P_{ND}.
2– Copy the non-dominated members of P into P_{ND}.
3– Delete the members of P_{ND} which are dominated.
4– If the number of P_{ND} members exceeds a given maximum N', prune P_{ND} by means of clustering.
5– Compute the fitness of all the individuals in P as well as in P_{ND}.
6– Choose the individuals from P+P_{ND}, until the mating pool is filled. Binary tournament selection with replacement can be used.
7– Apply crossover and mutation operators as usual.
8– If the maximum number of generations is done, end the algorithm, otherwise return to step 2

The Fitness assignment technique is done in two steps [26].

1– Every individual (i) of P_{ND} is considered a strength 0Si<1 which equals:

$$S_i = \frac{n}{N+1} \tag{3}$$

where N is the size of P and n is the number of individuals in P which are dominated by individual (i) of P_{ND}. The fitness of (i) equals Si.

2– For every individual (j) of P the fitness (fj) equals:

$$f_j = 1 + \sum_{i,i \geq j} S_j \quad where \quad f_j \quad \in [1,N) \tag{4}$$

The adding of 1 to the summing of the strengths of PND individuals which dominate j is done because small fitness values correspond to high reproduction probabilities. This guarantees that members of PND have better fitness than members of P.

Furthermore, a clustering approach called the average linkage method has been selected for SPEA. It includes the following steps [26]:

1– Initialize cluster set C. Each external non-dominated point i $\in$ P_{ND} forms a separate cluster:

$$C = \bigcup_i \{\{i\}\} \tag{5}$$

2– If the number of P_{ND} members does not exceed N', go to step 5, otherwise go to step 3.
3– Compute the distance for all possible pairs of clusters. The distance d between two clusters c_1 and $c_2 \in$ C is given as

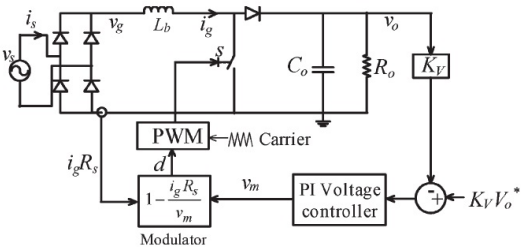


Fig. 1. Boost based PFC Rectifier under study with indirect current control [20].

the average distance between pairs of individuals across the two clusters.

$$d = \frac{1}{|C_1|.|C_2|}. \sum_{i1 \in C1, i2 \in C2} \|i_1 - i_2\| \tag{6}$$

Where the metric ||.||shows the distance between the two individuals i_1 and i_2.

4– Determine two clusters c_1 and c_2 with a minimal distance d. The selected clusters amalgamate into a large cluster:

$$C = C \setminus \{C_1, C_2\} \cup \{C_1 \cup C_2\} \tag{7}$$

Then return to step 2.

5– Compute the reduced P_{ND} by selecting one representative individual per cluster. SPEA considers a point with the minimal average distance to all other points in the cluster to be the representative solution.

III. Conventional PFC Rectifier System

The AC/DC converter under study is a Boost based PFC rectifier with a constant switching frequency that converts an AC input voltage to a desired DC voltage. This converter with the indirect current control system is shown in Fig. 1. Selection of the passive elements has been done according to the following equations [15].

$$L_b = \frac{M_g V_o^2}{8 P_o f_{sw} (\Delta I_{g(MAX)}/I_{gm})} \tag{8}$$

$$C_o = \frac{P_o}{2\pi f V_o^2 (\Delta V_{o(MAX)}/V_o)} \tag{9}$$

$$M_g = V_{gm}/V_o \tag{10}$$

where f, f_{sw}, P_O, V_O, and V_{gm} are the input supply frequency, switching frequency, output power, output voltage and peak input voltage of the PFC rectifier, respectively. In the conventional method, the PI gains of the voltage controller are designed based on the frequency domain model of the converter's voltage loop [20]. This model is shown in Fig. 2 where H(s) and G(s) are transfer functions for the PI controller and the plant, respectively. These transfer functions are according to (11) and (12).

$$H(s) = \frac{K_{PI}(1 + sT_{PI})}{sT_{PI}} \tag{11}$$

$$G(s) = \frac{G_V}{1 + sT_V} \tag{12}$$

TABLE I
Specifications of Boost based PFC rectifier

P_o	$300w$	R_s	0.2Ω
V_{gm}	$156v$	K_v	0.005
V_o	$230v$	R_e	40Ω
f_{sw}	$70kHz$	R_o	176Ω
L_b	$2mH$	C_o	$440\mu F$
$\frac{\Delta I_g(\max)}{I_{gm}}$	$< 10\%$	$\frac{\Delta V_o(\max)}{V_o}$	$< 4\%$

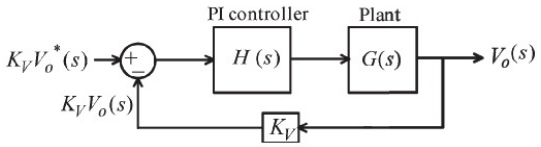


Fig. 2. Frequency domain model of the voltage control loop [20].

where G_v, T_v and K_{PI} can be calculated by use of (13), (14) and (15). Also, Re for the PFC rectifier can be estimated by using equation (16).

$$G_V = \frac{0.5 M_g^2 R_o/R_s}{1 + M_g^2 R_o/R_e} \tag{13}$$

$$T_V = \frac{R_o C_o}{1 + M_g^2 R_o/R_e} \tag{14}$$

$$K_{PI} = \frac{2\pi F_{BW} T_V}{G_V K_V} \tag{15}$$

$$R_e = \frac{V_{grms}^2}{P_o}. \tag{16}$$

The value of T_{PI} has been chosen to compensate the pole of the plant, so that it is almost equal to T_v. For the input current THD to be low, usually f_{BW} is considered to be less than the input supply frequency. It is set to around 10 Hz. The specifications of the PFC rectifier are displayed in Table I. Figure 3 shows the steady state input current with PI gains (K_{PI}=4.8, T_{PI}=26ms) which is obtained from the frequency domain model of the PFC Rectifier. Fig. 5 shows the dynamic response to a step change in the load, according to Fig. 4, with these gains. In this situation the input current THD is 7.26% while the dynamic response time to a step change in the load is 82 ms, which is not fast enough. With multi-objective optimization, a faster dynamic response with a lower input current THD can be obtained.

IV. Proposed Compensator Gains for a Fast Dynamic Response and a Low Input Current Distortion

For obtaining the optimized gains of the PI controller in the indirect current controller of a PFC rectifier, the flowchart which, is shown in Fig. 6, has been used. Also, the values of the parameters in this algorithm are displayed in Table II. There are two variables (Kpi, Tpi), which should be designed according to the control objectives. The initial position of each member of the first population can be represented by a two dimensional vector, and then the initial values are randomly generated based on the extreme values. The program is conducted by the m-file in MATLAB, while the objective functions are calculated in SIMULINK using the specifications

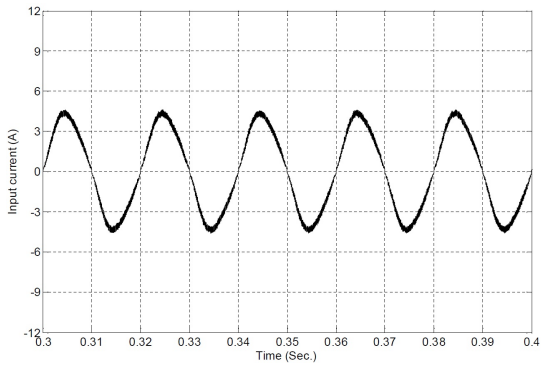


Fig. 3. Steady state input current of PFC rectifier with conventional PI gains (KPI=4.8, TPI=26ms), current THD equals 7.26%.

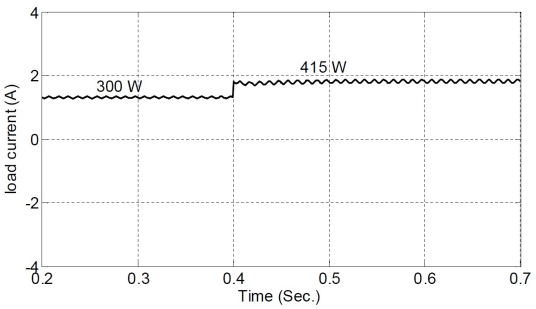


Fig. 4. Step change in the load of PFC rectifier from 300 W to 415 W.

of the system. This causes an error of the quasi steady state. Also, the small signal model approximations, which are needed for obtaining the frequency domain model, and the transfer functions of the rectifier need to be removed. For obtaining the objective functions for each member of each generation, two concerned parameters (PI gains) are sent to SIMULINK and after running it, the values of the steady state input current and the output voltage are returned to the program. With the help of this data the objective functions can be calculated as:

F1: The THD of the steady state input current:

$$THD = \left\{ \sqrt{U_{rms}^2 - U_o^2 - U_{1rms}^2} \Big/ U_{1rms} \right\} \qquad (17)$$

where:

U_{1rms}= the rms value of the fundamental component.

U_0= the DC component.

U_{rms}= the true rms value including the harmonics and the DC component.

F2: Time of dynamic response:

$$T_d = \min t \quad (\ after \quad t = 0.4 \quad Sec.) : e(t) < 4\% \qquad (18)$$

$$e(t) = \frac{230 - V_{out}(t)}{230} \times 100 \qquad (19)$$

In F_2 the error has been considered to be less than 4 percent because the output voltage ripple in the steady state is around 2.5% for a load equal to 300W. Due to a load step change, the output voltage can become unstable or show a poor dynamic response. Therefore, the input current THD and the dynamic response to the step change in the load at time 0.4 Sec. have been considered as objective functions. The SPEA algorithm runs until the stop condition is satisfied. The members of PND

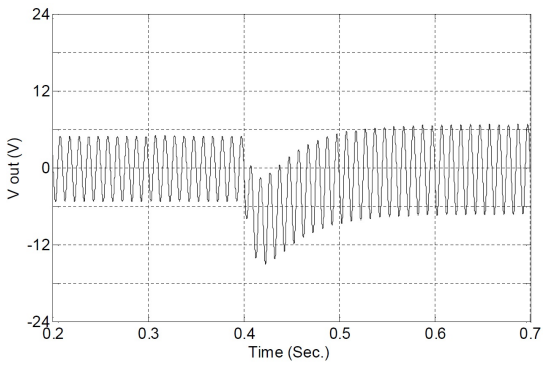


Fig. 5. Dynamic response of PFC rectifier to the step change of the load according to Fig. 4 with conventional PI gains (KPI=4.8, TPI=26ms), time of dynamic response is 82 ms, (AC mode of output voltage has been shown, DC value of output voltage is 230 Volt).

TABLE II
VALUES OF GENETIC ALGORITHM PARAMETERS

Parameter	SPEA
Iteration	25
Population size	30
Chromosome coding	Real-code
External non-dominated set size	30
Selection	Roulette wheel
Recombination	Single-point crossover, with probability of 0.7
Mutation	Discrete, with probability of 1/variables

in the last iteration are the optimized parameters of the PI controller. The optimal gains (Pareto Set) and the optimal results (Pareto Front) for running this program are given in Table III and the Pareto Front is shown separately in Fig. 7.

The dynamic responses and the steady state input current of the PFC rectifier for some points selected from this Pareto Front are shown in Fig. 8 and Fig. 9, respectively. All of these results are optimum, but according to some other technical priorities, any of them can be chosen. As can be seen in Fig. 8 (b) and Fig. 9 (b), a point of the Pareto Front (point 7) has around a 1.5 percent lower THD and a 50 ms faster dynamic response when compare to the input current THD and the dynamic response of a PFC rectifier with the conventional PI gains (Figures 3 and 5). In fact, this point dominates the conventional point. Also, as the Pareto Front shows, points 3-9 dominate the conventional design. When a lower THD is needed, point 1 and 2 can be selected and when a faster dynamic response is the first priority, point 10 can be chosen.

TABLE III
PARETO SET (PI CONTROLLER COEFFICIENTS) AND PARETO FRONT (INPUT CURRENT THD AND TIME OF DYNAMIC RESPONSE TO STEP CHANGE IN THE LOAD)

point	K_{PI}	T_{PI}	Dynamic response(Sec.)	Input Current THD (Percent)
1	0.1000	0.0014	0.1330	4.37
2	0.1000	0.0010	0.1020	4.40
3	0.9267	0.0053	0.0630	4.76
4	0.9267	0.0036	0.0530	4.77
5	0.9267	0.0030	0.0430	4.85
6	0.9267	0.0022	0.0330	4.93
7	2.1990	0.0036	0.0320	5.69
8	1.8777	0.0022	0.0230	5.72
9	2.9618	0.0022	0.0220	6.81
10	5.3768	0.0036	0.0130	8.62

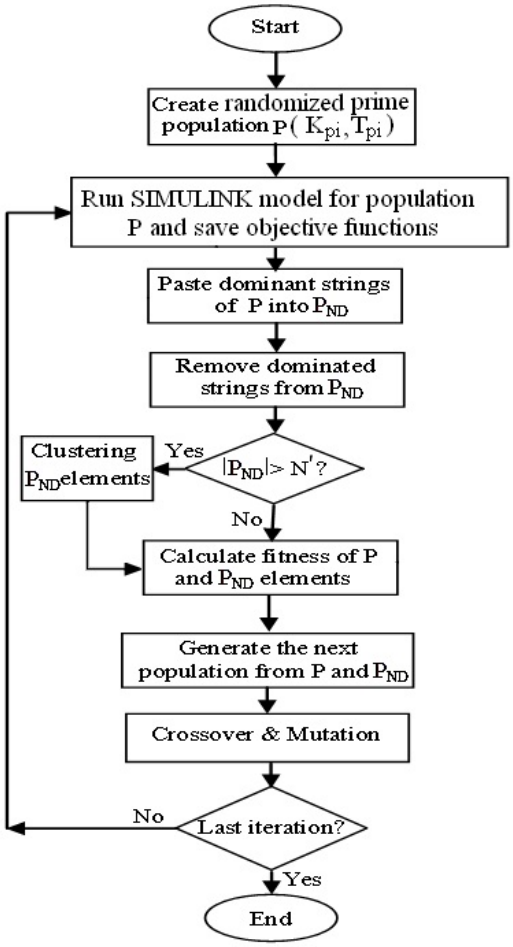


Fig. 6. The algorithm of SPEA used for optimization [27].

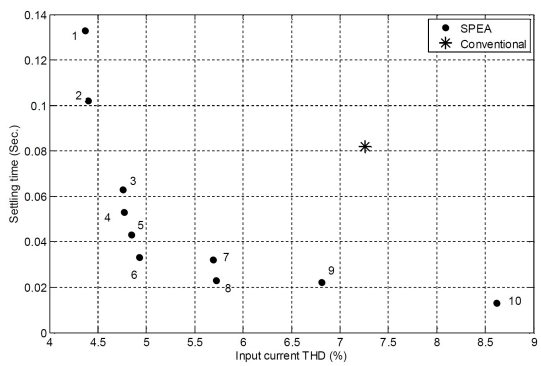


Fig. 7. Pareto Front.

From the Pareto Front, some interesting information can be obtained which helps in carrying out an efficient design. For example, by comparing the two points 6 and 7, as shown in Fig. 7, it can be seen that the two points cause an almost identical dynamic response (around 30 ms). However, point 6 provides an input current THD that is about one percent lower than point 7. Hence, if both the dynamic responses are acceptable, then from a practical point of view, point 6 provides much better results. With the help of the Pareto Front it becomes clear that suffering 1ms longer dynamic response can decrease 0.76 percent of the input current THD. By aging, the PI gains in the controller or the characteristics of the other elements may be changed. By using the Pareto Set and the Pareto Front a designer can see the neighborhood points of the selected optimized point and may consider possible changes.

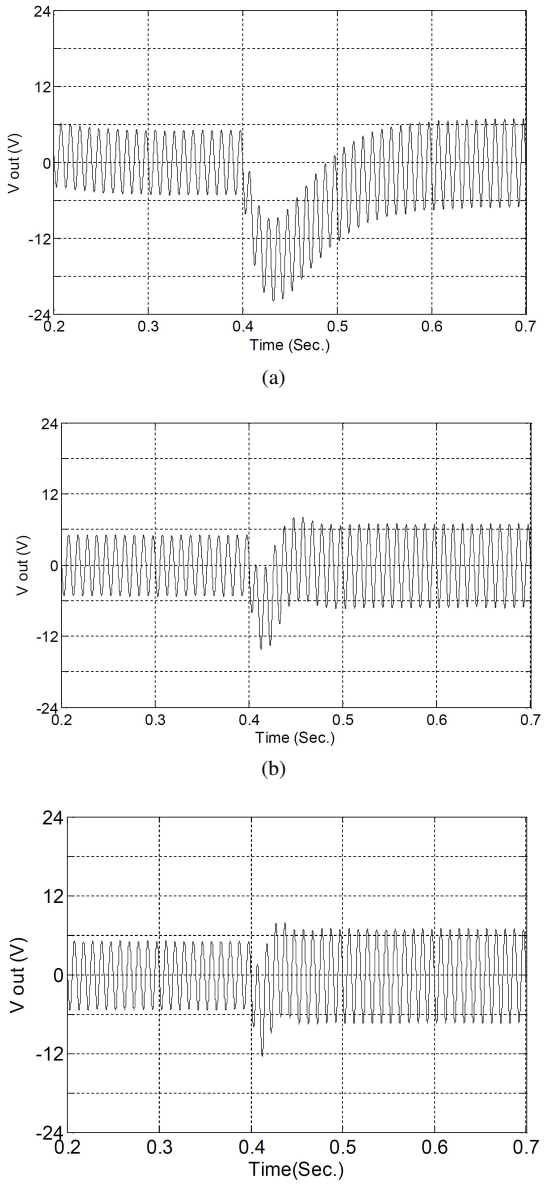
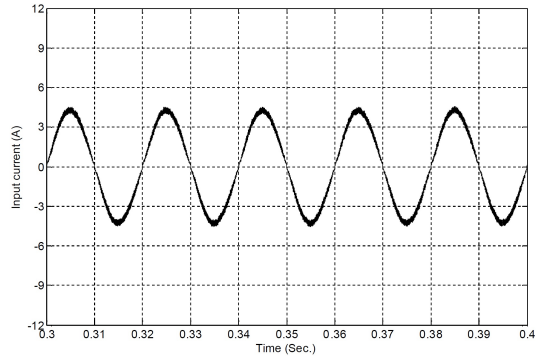


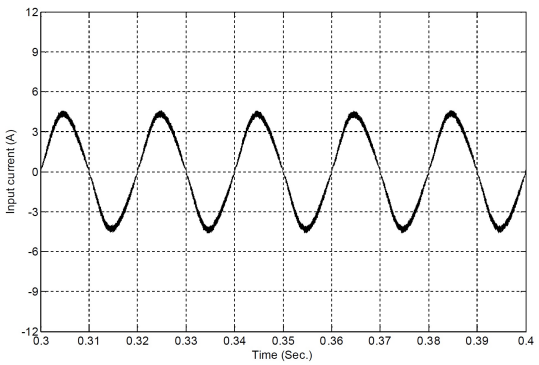
Fig. 8. Dynamic response of PFC rectifier to the step change of the load according to Fig. 4 for some points selected from Pareto Front. (a) Point 1. (b) Point 7. (c) Point 10.

V. Using of Proposed PID Gains in an Advanced Method

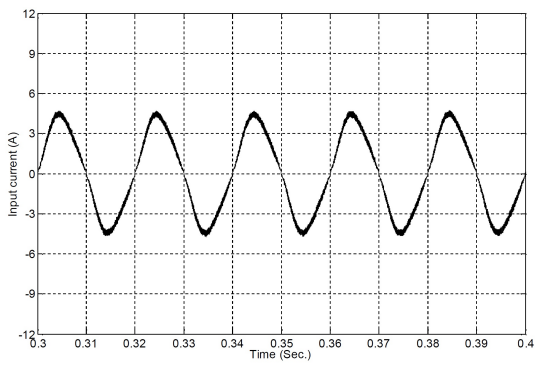
As discussed in the introduction of this paper, some advanced methods use an extra control block and improve the dynamic response of PFC rectifiers without degradation in the input current THD. For example in [4] a generalized feed forward controller has been used which implemented estimators for obtaining the value of the input voltage and the load current. This controller is shown in Fig. 10. The steady state input current and the dynamic response with this controller and the conventional PI gains are shown in Fig. 11 and Fig. 12, respectively. In this condition, due to the feed forward of the load current, the dynamic response is negligible



(a)



(b)



(c)

Fig. 9. Steady state input current of PFC rectifier for some points selected from Pareto Front. (a) Point 1. (b) Point 7. (c) Point 10.

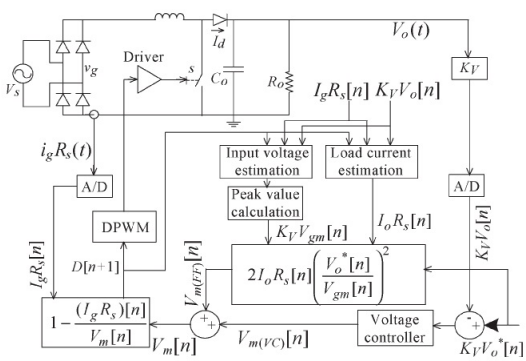


Fig. 10. Boost rectifier system with the generalized feed forward controller by using disturbance observer [4].

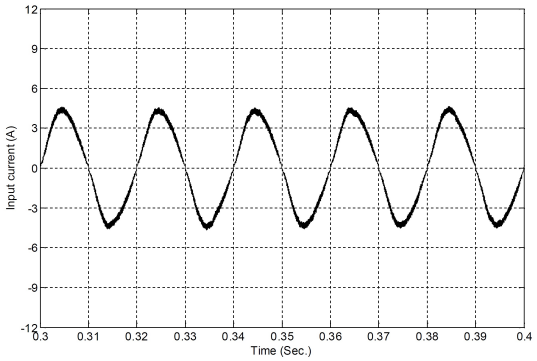


Fig. 11. Steady state input current of PFC rectifier with proposed method in [4] and conventional PI gains, current THD equals 7%.

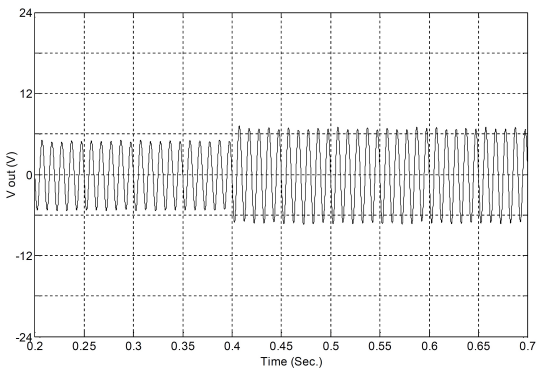


Fig. 12. Dynamic response of PFC rectifier with proposed method in [4] and conventional PI gains.

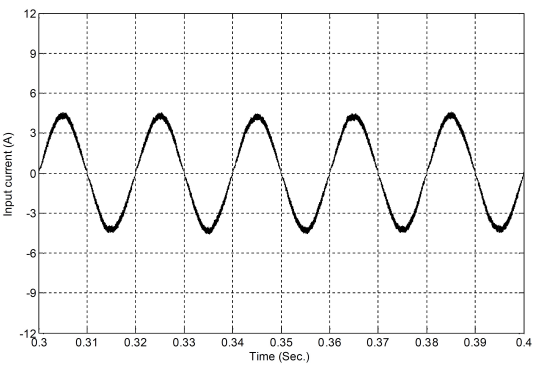


Fig. 13. Steady state input current of PFC rectifier with proposed method in [4] and PI gains according to point one of Table III, current THD equals 4.3%.

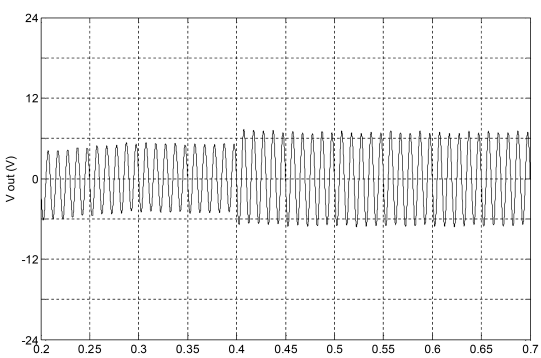


Fig. 14. Dynamic response of PFC rectifier with proposed method in [4] and PI gains according to point one of Table III.

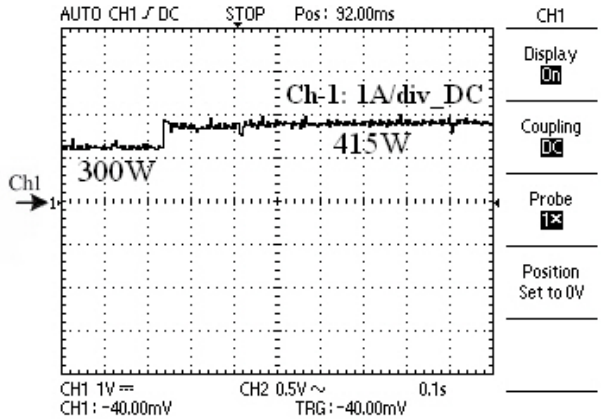


Fig. 15. Step change in the load of PFC rectifier from 300 to 415 W.

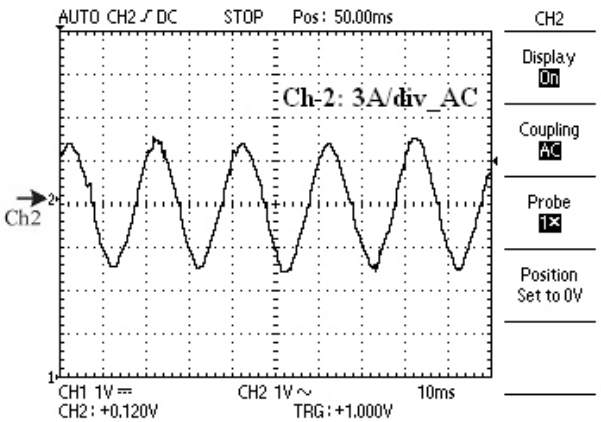


Fig. 16. Steady state input current of PFC rectifier with conventional PI gains, (KPI=4.8, TPI=26ms).Current THD is 7.5%.

and cannot be seen and the input current THD is 7%. With this controller and the proposed PI gains in this paper, point 1 of Table III can reduce the THD to 4.3%. Fig. 13 and Fig. 14 show the input current and the dynamic response in this situation. Since the main goal of this paper is to improve the performance of a PFC rectifier without any extra control block or computational burden, the proposed Pareto based gains will be tested on a simple indirect current controller in the experimental results section.

VI. Experimental Results

The control concept with the PI gains mentioned in section IV is validated on a 300-W Boost based PFC rectifier prototype. The passive elements and the controller parameters are the same as the ones mentioned in section III. The controller scheme was implemented on an eZdsp F2812. To study the dynamic response, a step change in the load from 300 W to 415 W, according to Fig. 15, is considered.

A. Steady state input current and dynamic response with the conventional PI gains

In this part, the experimental results for the PI gains obtained from the conventional way of designing a PI compensator are presented. In Fig. 16 the input current of the PFC rectifier in the steady state and in Fig. 17 the dynamic response to step changes in the load are shown.

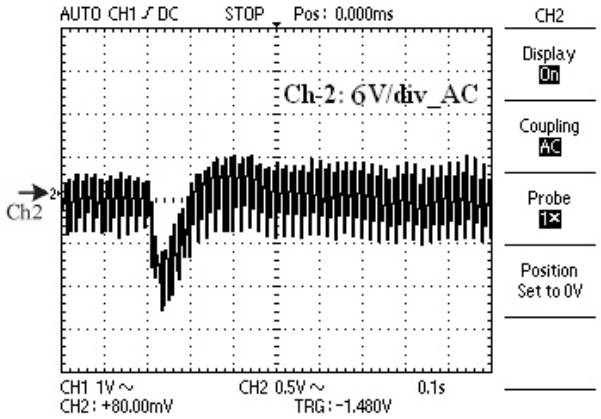


Fig. 17. Dynamic response of PFC rectifier with conventional PI gains, (KPI=4.8, TPI=26ms) Time of dynamic response equals 80 ms. (AC mode of output voltage has been shown, DC value of output voltage is 230 Volt).

B. Steady state input current and dynamic response with the proposed PI gains

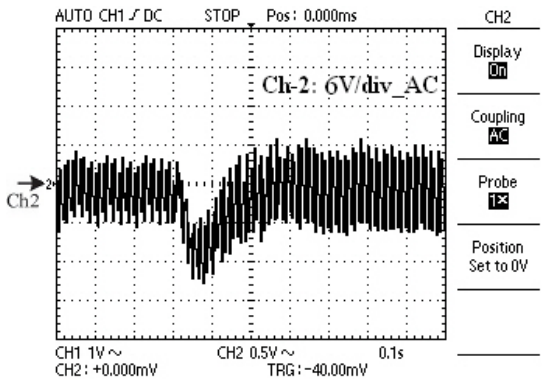
The optimal dynamic responses for step changes in the load for some points of Table III and the corresponding input current waveforms in the steady state are shown in Fig. 18 and Fig. 19, respectively. The dynamic responses of Fig. 18 are caused by a step change in the load from 300 W to 415 W which is shown in Fig. 15. For calculating the objective functions from the measured data (17) and (18), like the simulation condition, have been used. By moving on the Pareto Front, the dynamic response is improved while the input current distortion is increased (Fig. 18 (c) and Fig. 19 (c)). A numerical comparison of the simulation and experimental results is presented in Table IV. As can be seen, they are quite close to each other.

VII. Conclusions

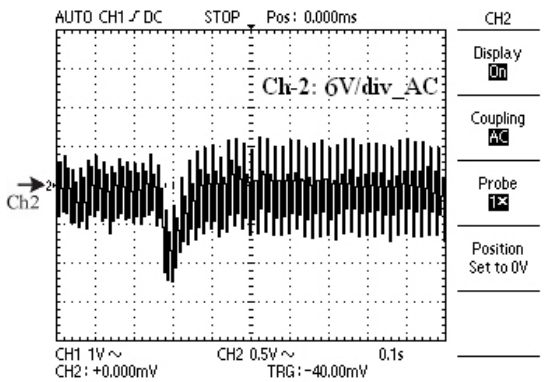
For a PFC rectifier, the input current THD and the dynamic response are conflicting features. Therefore, a multi-objective optimization method such as the Strength Pareto evolutionary algorithm can be useful in improving them simultaneously. In this paper, these features were defined as the objective functions and then optimized. With the help of the Pareto Set and the Pareto Front presented in the paper, designer can easily choose any result based on its features and his own engineering point of view. Simulation and experimental results proved that the PI gains offered in this paper, without any extra control blocks, can improve the dynamic response as well as the input current THD of a Boost based PFC rectifier.

TABLE IV
COMPARISON OF SIMULATION AND EXPERIMENTAL RESULTS

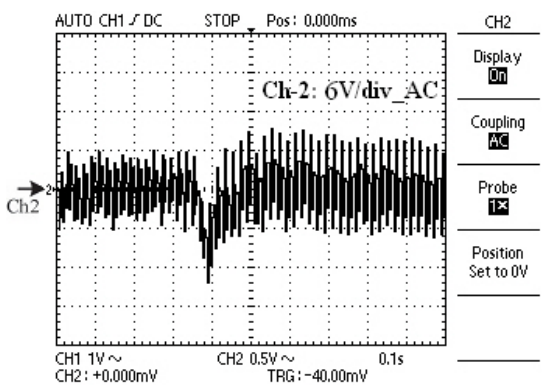
				Simulation results		Experimental results	
		K_{PI}	T_{PI}	Dynamic response(Sec.)	Input Current THD (Percent)	Dynamic response(Sec.)	Input Current THD (Percent)
point 1		0.1000	0.0014	0.1330	4.37	0.140	4.5
point 7		2.1990	0.0036	0.0320	5.69	0.040	5.7
	Conventional	4.800	0.0260	0.0820	7.26	0.080	7.5
	point 10	5.3768	0.0036	0.0130	8.62	0.016	9



(a)

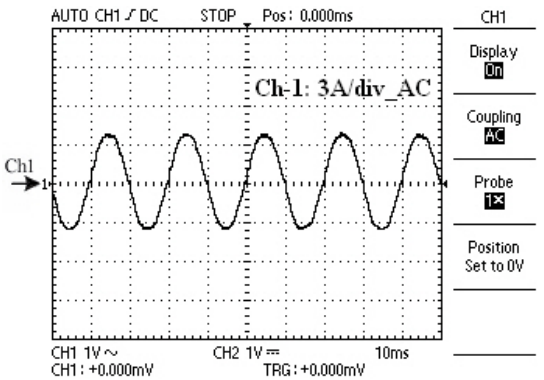


(b)

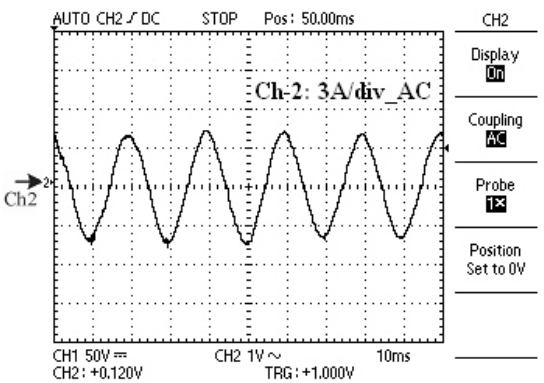


(c)

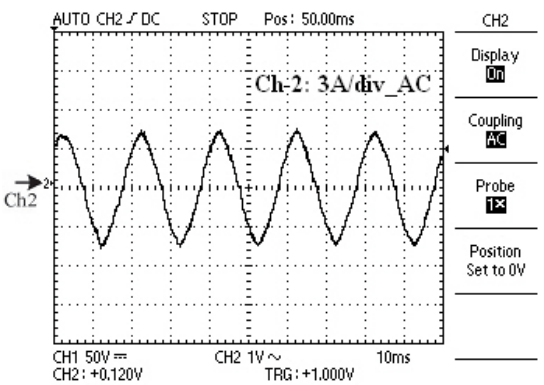
Fig. 18. Dynamic response of PFC rectifier for some points selected from Pareto Front, PI gains are same as points 1, 7, and 10 in Table III respectively. (a) Time of dynamic response equals 140 ms. (b) Time of dynamic response equals 40 ms. (c) Time of dynamic response equals 16 ms.



(a)



(b)



(c)

Fig. 19. Steady state input current of PFC rectifier for some points selected from Pareto Front, PI gains are same as points 1, 7, and 10 in Table III respectively. (a) Current THD is 4.5%. (b) Current THD is 5.7%. (c) Current THD is 9%.

REFERENCES

[1] E. Figueres, J. M. Benavent, G. Garcera, and M. Pascual, "Robust control of power-factor-correction rectifiers with fast dynamic response," *IEEE Trans. Ind. Electron.*, Vol. 52, No.1, pp.66-76, Feb. 2005

[2] J. M. Benavent, E. Figueres, G. Garcera, C. Cerver, and M. Pascual, "Design and evaluation of a power factor correction rectifier with robust control and fast dynamic response," *in Proc. IEEE PESC*, Vol. 3, pp. 2340-2345, Feb. 2004.

[3] E. Figueres, J. M. Benavent, G. Garcera, and M. Pascual, "A control circuit with load current injection for single-phase power factor correction rectifiers," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 3, pp.1272-1281, Feb. 2005.

[4] R. Ghosh and G. Narayanan, "Generalized feedforward control of single-phase PWM rectifiers using disturbance observers," *IEEE Trans. Ind. Electron.*, Vol. 54, No.2, pp. 984–993, Apr. 2007.

[5] M. O. Eissa, S. B. Leeb, G. C. Verghese, and A. M. Slankovic, "A fast analog controller for a unity-power factor AC/DC convener," *in Proc. IEEE APEC'94,* pp. 551-555, 1994.

[6] S. wall and R. Jackson, "Fast controller design for single-phase power-factor- correction systems," *IEEE Trans. Ind. Electron.*, Vol. 44, No. 5, pp. 654-660, Oct. 1997.

[7] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Power factor preregulators with improved dynamic response," *IEEE Trans. Power Electron.*, Vol. 12, No. 2, pp. 343-349, Mar. 1997.

[8] A. Prodic, I. Chen, R.W. Erickson, D. Maksimovic "Digitally controlled low-harmonic rectifier having fast dynamics responses," *in APEC'02*, 2002, pp. 476-482, 2002.

[9] S. Buso, P. Mattavelli, L. Rossetto, and G. Spiazzi , "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Trans. Power Electron.*, Vol. 13, No. 5, pp. 814-823, Sep. 1998.

[10] J. B. Williams, "Design of feedback loop in unity power factor AC to DC converter," *in Proc. IEEE PESC*, Vol. 2, pp. 959-967, Jun. 1989.

[11] A. Prodic, D. Maksimovic, and R. W. Erickson, "Dead-zone digital controllers for improved dynamic response of low harmonic rectifiers," *IEEE Trans. Power Electron.*, Vol. 21, No. 1, pp. 173-181, Jan. 2006.

[12] A. Prodic, J. Chen, D. Maksimovic, and R. W. Erickson, "Self-tuning digitally controlled low-harmonic rectifier having fast dynamics responses," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 420-428, Jan. 2003.

[13] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Methods to improve dynamic response of power factor preregulators: An overview," i*n Proc. EPE*, Vol. 3, pp.754-759,1995.

[14] W. I. Tsai, Y. Y. Sun, and W. S. Shieh, "Modelling and control of single phase switching mode rectifiers with near-optimum dynamic regulation," *in Proc. IEEE IECON'94*, pp. 501-506, 1994.

[15] R. Ghosh and G. Narayanan, "A single-phase boost rectifier system for wide range of load variations," *IEEE Trans. Power Electron.*, Vol. 22, No.2, pp. 4700-479, Mar. 2007.

[16] M. David, K.D. Gusseme, P. M. Alex, and J. A. Melkebeek "Duty-ratio feedforward for digitally controlled boost PFC converters," *IEEE Trans. Ind. Electron.*, Vol. 52, No. 1, pp. 108-115, Feb. 2005.

[17] M. Chen and J. Sun "Feedforward current control of boost single-phase PFC converters," *in Proc. IEEE APEC*, Vol. 2, pp. 1187-1193, 2004.

[18] S. B. Yaakov and I. Zeltser, "The dynamics of a PWM boost converter with resistive input" *IEEE Trans. Power Electron.*, Vol. 46, No. 3, pp. 613-619, Jun. 1999.

[19] Z. Lai and K. M. Smedley "A family of continuous-conduction-mode power-factor-correction controllers based on the general pulse-width modulator" *IEEE Trans. Power Electron*., Vol. 13, No. 3, pp. 501-510, May 1998.

[20] R. Ghosh and G. Narayanan, "A simple method to improve the dynamic response of single-phase pwm rectifiers," *IEEE Trans. Ind. Electron.*, Vol. 55, No.10, pp. 3627-3634, Oct. 2008

[21] H. Singh, "introduction to game theory and its application in electric power markets," *IEEE Computer Application in Power*, Vol.12, pp.18-22, Oct.1999.

[22] P. Hajela and C. Y. Lin, "Genetic search strategies in multicriterion optimal design," *Structural Optimization*, Vol. 4, pp. 99–107, Jun. 1992.

[23] J. Horn, N. Nafpliotis, and D. E. Goldberg, "A niched pareto genetic algorithm for multiobjective optimization," *in Proc. 1st IEEE Conf. Evolutionary Computation, IEEE World Congr. Computational Computation*, Vol. 1, pp. 82–87, 1994.

[24] M. P. Fourman, "Compaction of symbolic layout using genetic algorithms," *in Proc. Int. Conf. Genetic Algorithms and Their Applications*, pp.141-153, Jul. 1985.

[25] N. Srinivas and K. Deb, "Multiobjective optimization using nondominated sorting in genetic algorithms," *Evolutionary Computation*, Vol. 2, No. 3, pp. 221-248, 1994.

[26] E. Zitzler , and L. Thiele, "Multi-objective evolutionary algorithms :A comparative case study and the strength pareto approach," *IEEE Trans. Evol. Comput.,* Vol .3, No. 4 , pp. 257-271, Nov. 1999.

[27] S. M. R. Rafiei, A. Amirahmadi, and G. Griva, "Chaos rejection and optimal dynamic response for boost converter using spea multi-objective optimization approach," *in Proc. IEEE IECON'09*, pp. 3315-3322, Nov. 2009.

Ahmadreza Amirahmadi was born in Damghan, Iran, in 1985. He received his B.S. and M.S. in Electrical Engineering from the Shahrood University of Technology, Shahrood, Iran, in 2007 and 2010, respectively. Since 2010, he has been working towards his Ph.D. at the University of Central Florida, Orlando. His current research interests are in the area of power electronics converters.

Ali Dastfan was born in Iran in 1966. He received his B.E. from the University of Ferdosi, Mashhad, Iran, in 1989, and his M.E. and Ph.D. in Electrical Engineering from the University of Wollongong, Australia, in 1994 and 1998, respectively. He is currently with the Department of Electrical and Robotic Engineering at the Shahrood University of Technology, Iran. His current research interests include power electronics and power quality.

Mohammadreza Rafiei (M'03, SM'04) was born in 1969 in Tehran, Iran. He received his B.S. (with honors) from the Sistan and Baluchistan University, Zahedan, Iran, in 1991, and his M.S. and Ph.D. from the Ferdowsi University of Mashhad, Mashhad, Iran, in 1995 and 2000, respectively, all in Electrical Engineering. Dr. Rafiei is a Senior Member of the IEEE and a member of the IEEE Control Systems, Power Electronics, and Power & Energy Societies. His current research interests include energy systems, control systems, power electronics, and power quality.