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Analysis and Design of the Interface Inductor and the DC Side Capacitor in a STATCOM with Phase and Amplitude Control Considering the Stability of the System

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Abstract

Previous publications regarding the design and specifications of the interface inductor and the DC side capacitor for a STATCOM usually deal with the interface inductor and the DC side capacitor only. They seldom pay attention to the influences of the interface inductor and capacitor on the performance of a STATCOM system. In this paper a detailed analysis of influence of the interface inductor and the DC side capacitor on a STATCOM system and the corresponding design considerations is presented. Phase and amplitude control is considered as the control strategy for the STATCOM. First, a model of a STATCOM system is carried out. Second, through frequency domain methods, such as transfer functions and Bode plots, the influence of the interface inductor and the DC side capacitor on the stability and filtering characteristics of the STATCOM are extensively investigated. Third, according to this analysis, the design considerations based on the phase margin for the interface inductor and the DC side capacitor are discussed, which leads to parameters that are different from those of the traditional design.

Key Words: DC side capacitor, Interface inductor, Phase and amplitude control, Phase margin, STATCOM

I. INTRODUCTION

A Static Synchronous Compensator (STATCOM) is one of the FACTS (flexible AC transmission system) devices. It is an advanced shunt compensator when compared with other compensators. A STATCOM can be utilized to regulate voltage, control power factor, stabilize power flow and improve the dynamic performance of power systems [1]. This compensator has been gaining wide attentions in recent years [2]–[5]. There is a voltage source converter connected to the grid through an interface inductor in a STATCOM system. The interface inductor is a low pass filter.

The design of the interface inductor and the DC side capacitor is very important. Many papers discuss the selection methods for the STATCOM parameters. For example, in [6], [7], the interface inductor must satisfy the ripple current requirement, and, in [8], the voltage drop across the inductor must be taken into consideration to design an interface inductor. The methods mentioned in these three papers are very useful for choosing the parameters of an interface inductor. However, the stability of the STATCOM systems were not considered with any of the selection methods. In practical applications, the filtering performance is usually the main aspect considered. Then, by using the experience of practical applications and many experimental results, the parameters of the interface inductor are usually designed. In terms of the DC side capacitor, many papers reduce the DC side capacitor. For example, in [8] highly reliable film capacitors are used to minimize the capacitor size and cost. This paper also mentioned that the design approaches for the DC side capacitors often depend on three aspects: the maximum ripple current capability of the capacitor, the maximum allowable voltage ripple and the desired ride through capability during grid failures or voltage sags. The design approaches are valid. However, the stability of STATCOM systems should be considered when designing the DC side capacitor. In [9]–[11], methods to reduce the DC side capacitor were presented, and the minimum capacitor size was obtained. In [12]–[14], methods for reducing the voltage ripple to design the DC side capacitor were presented. Previous publications regarding the design and specifications of the interface inductor and the DC side capacitor for a STATCOM usually deal with the interface inductor and the DC side capacitor only, and seldom pay attention to the influences of the interface inductor and the DC side capacitor on STATCOM

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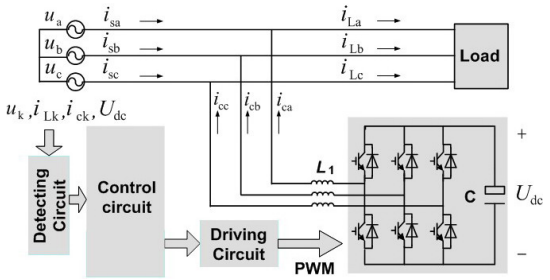

Fig. 1. Main circuit of the STATCOM.

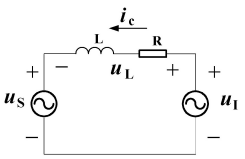

Fig. 2. Single-phase equivalent circuit.

system performance. However, this is not enough.

Therefore, the influence of the interface inductor and the DC side capacitor on the stability of a STATCOM system should be analyzed. Then, the interface inductor and the DC side capacitor can be designed more reasonably and more highly optimized.

In this paper a detailed analysis of the interface inductors and the DC side capacitors that influence STATCOM systems, and the corresponding design consideration are presented. In STATCOM systems, especially in high voltage and power situations, the interface inductor is usually an inductor, and two basic control methods are used. One is the phase-shift control [15]–[18], and the other is the Phase and Amplitude Control (PAC) [19]–[22]. In this paper, the phase and amplitude control is considered as the STATCOM control strategy. First, a model of the STATCOM is carried out. Second, the transfer functions are presented, and the influence of the interface inductor and the DC side capacitor on the STATCOM system stability and filtering characteristics are extensively investigated. Third, based on this analysis, the design considerations for the interface inductor and the DC side capacitor are presented.

II. System Configuration and Control Strategy

The main circuit of a STATCOM is shown in Fig. 1. $u_k(k=a,b,c)$ is the phase to neutral source voltage, i_{Lk} is the load phase current, i_{sk} is the source phase current, i_{ck} is the output phase current, and U_{dc} is the DC side voltage. A single-phase equivalent circuit is shown in Fig. 2. The variables are shown as follows. u_s is the source voltage, u_L is the voltage of the inductor, i_c is the output current, u_I is the output voltage of the converter, and Z ($Z=j\omega L$) is the impedance of the inductor. The losses of the converter are regarded as the active power in the resistor of the inductor [23]-[25].

The mathematical instantaneous three-phase model of a STATCOM is shown as (1) and (2). Using the transformation, equation (1) can be transformed to the synchronously rotating reference frame as (3). With (4) and (5), the STATCOM system model can be carried out as (6) [16], where δ is the phase angle between the source phase voltage and the output phase voltage of the converter. The variable θ is determined by the amplitude of the output voltage. The d axis in the reference frame has

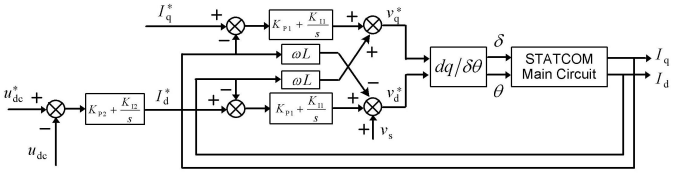

Fig. 3. Phase and amplitude control diagram of STATCOM.

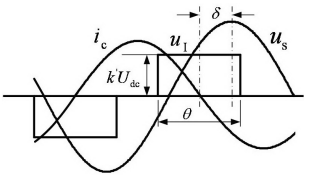

Fig. 4. Control principle of the STATCOM.

the same direction as the phasor of the source voltage, that is, the initial rotating angle is zero. The q axis is perpendicular to the d axis. Therefore, u_{sq}=0. The parameter k is decided by the DC side voltage and the peak value of the output voltage.

$$L\frac{d}{dt}\begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} + \begin{bmatrix} Ri_{ca} \\ Ri_{cb} \\ Ri_{cc} \end{bmatrix} = \begin{bmatrix} u_{Ia} \\ u_{Ib} \\ u_{Ic} \end{bmatrix} - \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{1}$$

$$\frac{d}{dt}u_{dc} = -\frac{1}{C}i_{dc} \tag{2}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{L}\begin{bmatrix} u_d - u_{sd} \\ u_q - u_{sq} \end{bmatrix} - \begin{bmatrix} \frac{R}{L}i_d - \omega i_q \\ \frac{R}{L}i_q + \omega i_d \end{bmatrix} \tag{3}$$

$$u_{dc}i_{dc} = \frac{3}{2}\left(u_d i_d + u_q i_q\right) \tag{4}$$

$$u_d = k u_{dc}\cos\delta \tag{5}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ u_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega & \frac{k}{L}\cos\delta \\ -\omega & -\frac{R}{L} & \frac{k}{L}\sin\delta \\ -\frac{3}{2C}k\cos\delta & -\frac{3}{2C}k\sin\delta & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ u_{dc} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} u_{sd} \\ 0 \end{bmatrix} \tag{6}$$

A phase and amplitude control diagram of a STATCOM is shown in Fig. 3.

The control principle is shown in Fig. 4 [16], and several pulse waveforms can be used instead of rectangular waveforms in order to eliminate the harmonics when the fundamental part of output voltage is just guaranteed.

With the Fourier analysis, the fundamental part is expressed as (7). The relationship between δ/θ and $u_d/u_q$is expressed in (8) [16].

$$\begin{cases} u_d = \frac{4}{\pi}u_{dc}\sin\frac{\theta}{2}\cos\delta \\ u_q = \frac{4}{\pi}u_{dc}\sin\frac{\theta}{2}\sin\delta \end{cases} \tag{7}$$

$$\begin{cases} \theta = 2\arcsin\left(\frac{\pi}{4u_{dc}}\sqrt{u_d^2+u_q^2}\right) \\ \delta = \arctan\left(\frac{u_q}{u_d}\right) \end{cases} \tag{8}$$

III. Model of the STATCOM System

A. Model of the main circuit

By using (6), the main circuit model is expressed in (9). The small signal model is shown in (10). Where, the steady operation points are u_{dc0}, v_{d0}, v_{q0}, i_{d0} and i_{q0}, and k=[4sin(θ/2)]/π.

B. Model of $dq/\delta\theta$

The small signal model equations of $dq/\delta\theta$ are shown as (11) which were obtained by using equation (8).

C. Model of the STATCOM System

From (10) in A and (11) in B, the small signal model from the reference voltages to the output currents is carried out as (12). It is a model of the STATCOM system.

D. Another modeling method

Because the transfer function $dq/\delta\theta$ has no time delay and it is just a mathematical transfer function, the model from the reference voltages to the output currents can be presented directly by using (4). The small signal analysis is shown in (13). The same signal model can be obtained as (12). The two modeling methods have the same small signal model.

$$u_{\mathrm{dc0}}\frac{d\left(\Delta u_{\mathrm{dc}}\right)}{dt}=-\frac{3}{2C}\left(u_{\mathrm{d0}}\Delta i_{\mathrm{d}}+\Delta u_{\mathrm{d}}i_{\mathrm{d0}}+u_{\mathrm{q0}}\Delta i_{\mathrm{q}}+\Delta u_{\mathrm{q}}i_{\mathrm{q0}}\right) \quad (13)$$

IV. Influence of the Parameters on the STATCOM System Characteristic and Design Method

There are two types of closed loops, one is the current loop, and the other is the DC voltage control loop. The designs of the two control loops and the influence of the main power parameters on STATCOM system stability are discussed. The designs of the parameters are also presented.

A. Current control loop

The current control loop is shown in Fig. 5. The two current loops are decoupled in Fig. 3. Because a period of the source current is used to calculate the rms of the current, the calculate part can be expressed as a first-order inertia element and a proportion model [26], [27]. The time delay is $T_f/2$ (T_f is the current period, 20ms).

When a proportion regulator is used, the transfer function of the current control loop is shown in (14).

$$G_{\mathrm{open}}(s)=\frac{k_{\mathrm{P1}}}{\frac{LT_{\mathrm{f}}}{2}s^2+\left(\frac{RT_{\mathrm{f}}}{2}+L\right)s+R} \quad (14)$$

A 50MVA/10kV STATCOM is considered for analysis. In the traditional process, when the model of the STATCOM and the parameters are known, then a P regulator can be used to design a closed loop STATCOM system. However, the parameters of the interface inductor and the DC side capacitor, which are designed using many methods, are not precise enough. In the design process, a change in the interface inductor and the DC side capacitor is not convenient. Therefore, a proper parameter for the P regulator should be chosen, and the influences of the main circuit parameters on the STATCOM system should be analyzed. Then, it can provide a more optimized method to design the interface inductor and the DC side capacitor. An open loop Bode diagram and a closed loop Bode diagram are shown in Fig. 6 and Fig. 7, respectively. The current loop is stable. The cut-off frequency is approximately 10Hz, where C=0.1F, L=3mH, ω=314, R=0.08Ω, and k_p=0.2. The influence of STATCOM system parameters on the STATCOM system stability is presented in Fig. 8 and Fig. 9. From Fig. 8, parameter R has a big influence on magnitudes of low frequency (below 2 Hz). However, it does not have an influence on the magnitudes of medium and high frequency. When the resistor R increases, magnitudes of low frequency decrease. From Fig. 9, parameter L affects magnitudes of medium and high frequency. However, it does not have an affect on magnitudes of low frequency. When inductor L increases, the cut-off frequency decreases and the effect on noise attenuation becomes better. Then, the phase margin of the STATCOM system increases. The relationship between the phase margin γ and the inductor L is illustrated in (15), where, ω_0 is the crossing frequency, which can be obtained according to (16).

$$\gamma=180^\circ-\arctan\frac{\omega_0 T_{\mathrm{f}}}{2}-\arctan\frac{\omega_0 L}{R} \quad (15)$$

$$\frac{k_{\mathrm{P1}}}{\left(1+\frac{T_{\mathrm{f}}}{2}\omega_0\right)(L\omega_0+R)}=1 \quad (16)$$

The phase margin γ, considered as one of input filter parameters, can be used to design the interface inductor. It is good for the stability and reliability of the whole STATCOM system. The interface inductor can be designed by using (17). The more the inductor increases, the bigger the phase margin becomes. An example is shown in Fig. 10, where k_{P1}=0.2, L=5mH, R=0.08Ω, and C=80000μF.

$$L=\frac{R}{\omega_0}\tan\left(180^\circ-\arctan\frac{\omega_0 T_{\mathrm{f}}}{2}-\gamma\right) \quad (17)$$

When the regulator is a PI regulator, the same conclusions are obtained. This is because the integration part increases magnitudes of low frequency and only affects the low frequency part in the open loop Bode diagram.

B. DC side voltage control loop

The DC side voltage control loop is shown in Fig. 11. From (12), the transfer functions can be presented as (18). The relationships between the variables in the synchronously rotating reference frame and the variables in the stationary reference frame (*abc* frame) are shown in (19) and (20), where E_m is the peak value of the source voltage in the *abc* frame and I_m is the peak value of the active current in the *abc* frame. Then, the small signal model is expressed as equation (21).

$$\begin{cases}\dfrac{\Delta u_{\mathrm{dc}}}{\Delta i_{\mathrm{d}}}=\dfrac{-\dfrac{3}{2Cu_{\mathrm{dc0}}}\left(Li_{\mathrm{d0}}s+u_{\mathrm{sd0}}+2Ri_{\mathrm{d0}}\right)}{s}\\ \dfrac{\Delta u_{\mathrm{dc}}}{\Delta i_{\mathrm{q}}}=\dfrac{-\dfrac{3}{2Cu_{\mathrm{dc0}}}\left(Li_{\mathrm{q0}}s+u_{\mathrm{sq0}}+2Ri_{\mathrm{q0}}\right)}{s}\end{cases} \quad (18)$$

$$\frac{d}{dt}\begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \\ u_{\mathrm{dc}} \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & \omega & \dfrac{4}{\pi L}\sin\dfrac{\theta}{2}\cos\delta \\ -\omega & -\dfrac{R}{L} & \dfrac{4}{\pi L}\sin\dfrac{\theta}{2}\sin\delta \\ -\dfrac{6}{C\pi}\sin\dfrac{\theta}{2}\cos\delta & -\dfrac{6}{C\pi}\sin\dfrac{\theta}{2}\sin\delta & 0 \end{bmatrix}\begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \\ u_{\mathrm{dc}} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} u_{\mathrm{sd}} \\ 0 \end{bmatrix} \tag{9}$$

$$\frac{d}{dt}\begin{bmatrix} \Delta i_d \\ \Delta i_q \\ \Delta u_{dc} \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & \omega & \dfrac{4}{\pi L}\sin\dfrac{\theta_0}{2}\cos\delta_0 \\ -\omega & -\dfrac{R}{L} & \dfrac{4}{\pi L}\sin\dfrac{\theta_0}{2}\sin\delta_0 \\ -\dfrac{6}{\pi C}\sin\dfrac{\theta_0}{2}\cos\delta_0 & -\dfrac{6}{\pi C}\sin\dfrac{\theta_0}{2}\sin\delta_0 & 0 \end{bmatrix}\begin{bmatrix} \Delta i_d \\ \Delta i_q \\ \Delta u_{dc} \end{bmatrix} +$$

$$\begin{bmatrix} -\dfrac{4}{\pi L}u_{\mathrm{dc0}}\sin\dfrac{\theta_0}{2}\sin\delta_0 & \dfrac{2}{\pi L}u_{\mathrm{dc0}}\cos\dfrac{\theta_0}{2}\cos\delta_0 \\ \dfrac{4}{\pi L}u_{\mathrm{dc0}}\sin\dfrac{\theta_0}{2}\cos\delta_0 & \dfrac{2}{\pi L}u_{\mathrm{dc0}}\cos\dfrac{\theta_0}{2}\sin\delta_0 \\ \dfrac{3}{\pi C}\sin\dfrac{\theta_0}{2}\left(i_{\mathrm{d0}}\sin\delta_0 - i_{\mathrm{q0}}\cos\delta_0\right) & -\dfrac{3}{\pi C}\cos\dfrac{\theta_0}{2}\left(i_{d0}\cos\delta_0 + i_{\mathrm{q0}}\sin\delta_0\right) \end{bmatrix}\begin{bmatrix} \Delta\delta \\ \Delta\theta \end{bmatrix} \tag{10}$$

$$\begin{cases} \Delta\delta = -\dfrac{\pi}{4u_{\mathrm{dc0}}\sin\dfrac{\theta_0}{2}}\sin\delta_0\Delta u_{\mathrm{d}} + \dfrac{\pi}{4u_{\mathrm{dc0}}\sin\dfrac{\theta_0}{2}}\cos\delta_0\Delta u_{\mathrm{q}} \\ \Delta\theta = 2\dfrac{\pi}{4u_{\mathrm{dc0}}\cos\dfrac{\theta_0}{2}}\cos\delta_0\Delta u_{\mathrm{d}} + 2\dfrac{\pi}{4u_{\mathrm{dc0}}\cos\dfrac{\theta_0}{2}}\sin\delta_0\Delta u_{\mathrm{q}} - \dfrac{2\Delta u_{\mathrm{dc}}\sin\dfrac{\theta_0}{2}}{u_{\mathrm{dc0}}\cos\dfrac{\theta_0}{2}} \end{cases} \tag{11}$$

$$\frac{d}{dt}\begin{bmatrix} \Delta i_{\mathrm{d}} \\ \Delta i_{\mathrm{q}} \\ \Delta u_{\mathrm{dc}} \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & \omega & 0 \\ -\omega & -\dfrac{R}{L} & 0 \\ -\dfrac{3u_{\mathrm{d0}}}{2Cu_{\mathrm{dc0}}} & -\dfrac{3u_{\mathrm{q0}}}{2Cu_{dc0}} & \dfrac{3}{2Cu_{\mathrm{dc0}}^2}\left(i_{\mathrm{d0}}u_{\mathrm{d0}} + i_{\mathrm{q0}}u_{\mathrm{q0}}\right) \end{bmatrix}\begin{bmatrix} \Delta i_{\mathrm{d}} \\ \Delta i_{\mathrm{q}} \\ \Delta u_{\mathrm{dc}} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & 0 \\ 0 & \dfrac{1}{L} \\ -\dfrac{3i_{\mathrm{d0}}}{2Cu_{\mathrm{dc0}}} & -\dfrac{3i_{\mathrm{q0}}}{2Cu_{\mathrm{dc0}}} \end{bmatrix}\begin{bmatrix} \Delta u_{\mathrm{d}} \\ \Delta u_{\mathrm{q}} \end{bmatrix} \tag{12}$$

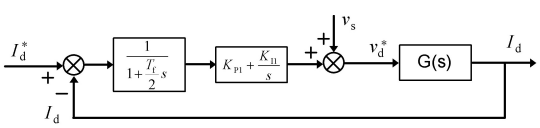

Fig. 5. Current control loop of the STATCOM.

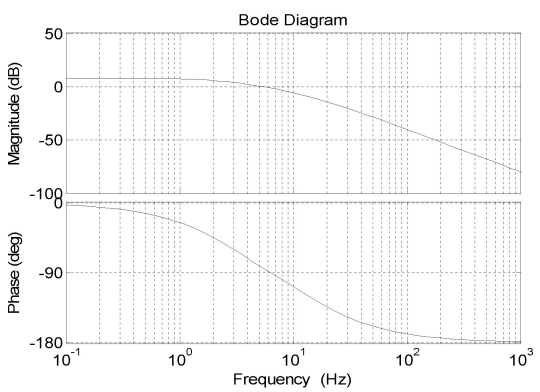

Fig. 6. Bode diagram of the open loop.

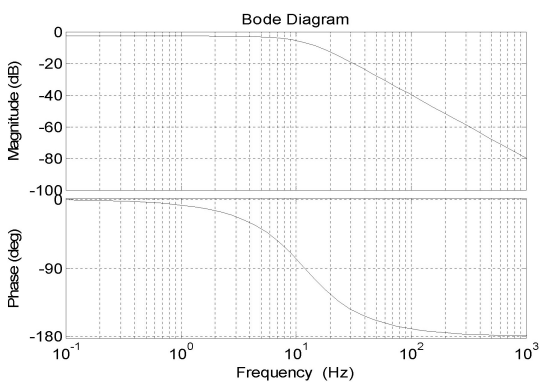

Fig. 7. Bode diagram of the closed loop.

$$u_{\mathrm{d0}} = \sqrt{3}\sqrt{\frac{2}{3}}U_{\mathrm{sa}} = E_{\mathrm{m}} \tag{19}$$

$$i_{\mathrm{d0}} = \sqrt{3}\sqrt{\frac{2}{3}}I_{\mathrm{a}} = I_{\mathrm{m}} \tag{20}$$

$$\frac{\Delta u_{\mathrm{dc}}}{\Delta i_{\mathrm{d}}^*} = -\frac{\dfrac{3k_{\mathrm{P1}}}{2Cu_{\mathrm{dc0}}}\left(E_{\mathrm{m}} + 2RI_{\mathrm{m}} + LI_{\mathrm{m}}s\right)}{s\left(\dfrac{LT_{\mathrm{f}}}{2}s^2 + \left(\dfrac{RT_{\mathrm{f}}}{2} + L\right)s + R + k_{\mathrm{P1}}\right)} \tag{21}$$

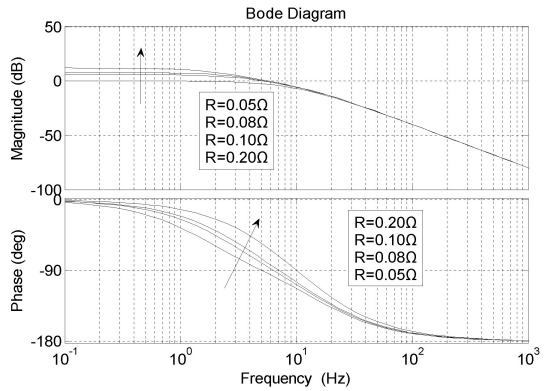

Fig. 8. Influence of R on the open loop.

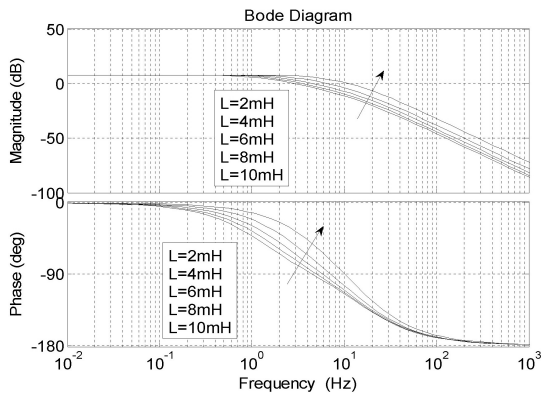

Fig. 9. Influence of L on the open loop.

Because the cut-off frequency of the DC side voltage control loop is much larger than that of the current control loop, the magnitude of the current control loop can be considered as one. The open loop transfer function of the DC side voltage control loop is shown in (22).

$$G_{\mathrm{V}}(s)=k_{\mathrm{P2}}\frac{\Delta u_{\mathrm{dc}}}{\Delta i_{\mathrm{d}}^{*}}=\frac{\dfrac{3k_{\mathrm{P1}}k_{\mathrm{P2}}}{2Cu_{\mathrm{dc0}}}\left(E_{\mathrm{m}}+2RI_{\mathrm{m}}+LI_{\mathrm{m}}s\right)}{s} \tag{22}$$

Bode diagrams of the DC side voltage control's open loop and closed loop are shown in Fig. 12 and Fig. 13. The cut-off frequency is approximately 0.6Hz, where k_{P1}=0.2, k_{P2}=1, L=5mH, R=0.08Ω, C=0.1F, E_m=8164V, I_m=-164A, and u_{dc0}=2.5kV.

From Fig. 14, there is a Right-half Plane Zero. However, the Right-half Plane Zero is very large and it has a small influence on the STATCOM system stability. The influence of the STATCOM system parameter C on the STATCOM system stability is presented in Fig. 15. From Fig. 15, it can be seen that parameter C has a large influence on the magnitude characteristic, and that it does not affect the phase characteristic. When capacitor C increases, the cut-off frequency decreases, and the effect on noise attenuation becomes better. The phase margin of the STATCOM system increases.

When the regulator is a PI regulator, the same conclusions are obtained. This is due to the fact that the integration part affects the low frequency.

The relationship between the phase margin γ and the DC side capacitor C is illustrated in (23), where ω_0 is the crossing

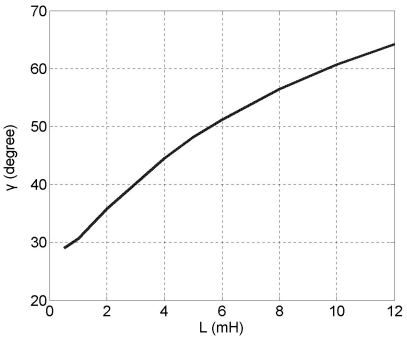

Fig. 10. Relationship between phase margin γ and interface inductor L.

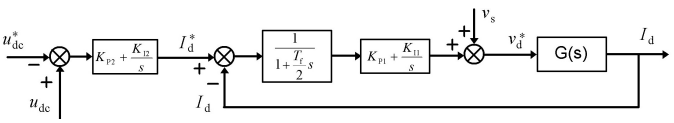

Fig. 11. DC side voltage control loop of the STATCOM.

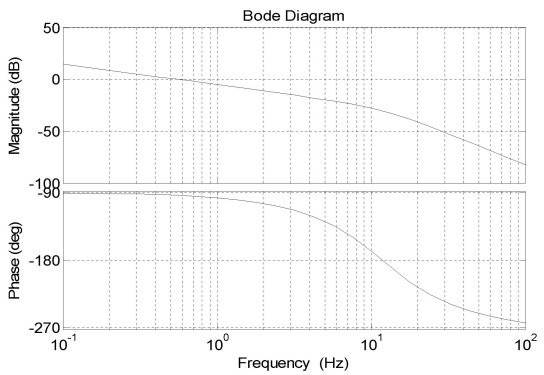

Fig. 12. Bode diagram of the open loop.

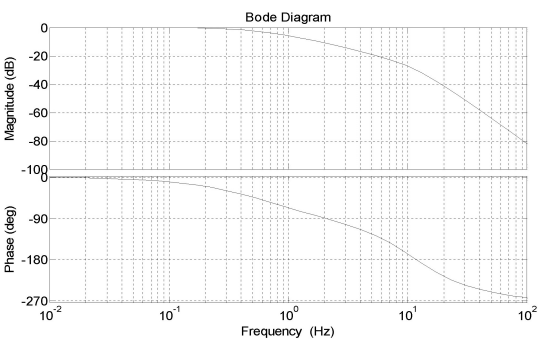

Fig. 13. Bode diagram of the closed loop.

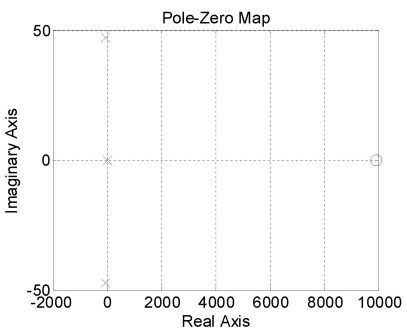

Fig. 14. Pole-zero map of open loop.

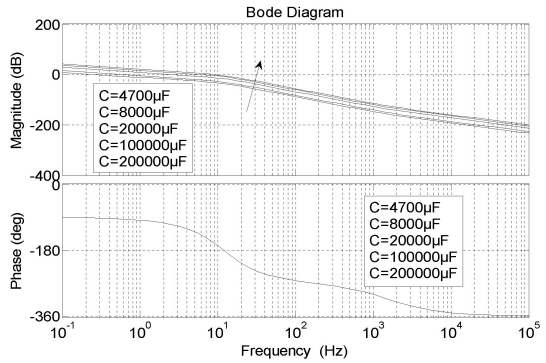

Fig. 15. Influence of C on the open loop.

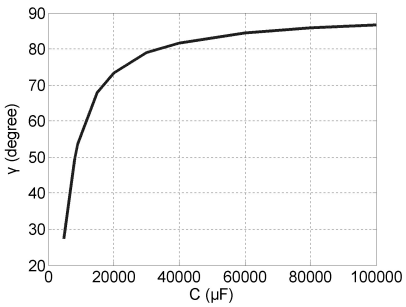

Fig. 16. Relationship between phase margin γ and capacitor C.

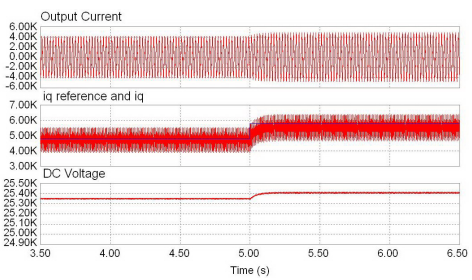

Fig. 17. Current step response at 5 s.

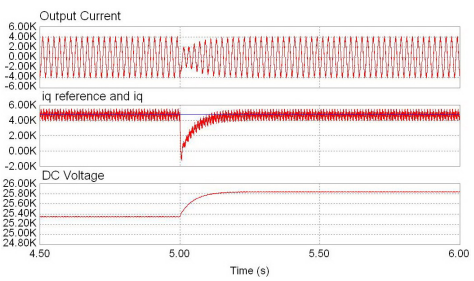

Fig. 18. DC side voltage step response at 5 s.

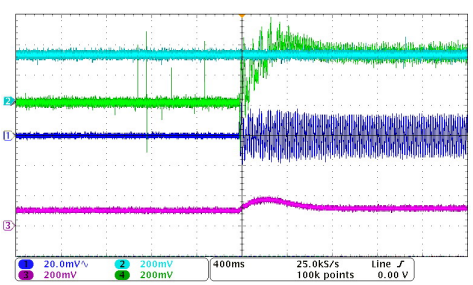

Fig. 19. Current response of dynamic process. Ch1:output current in *abc* frame; Ch2:reference current in synchronously rotating reference frame; Ch3: DC side voltage; Ch4:output current in synchronously rotating reference frame.

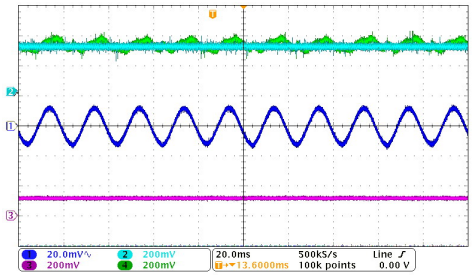

Fig. 20. Current response of stead-state. Ch1:output current in *abc* frame; Ch2:reference current in synchronously rotating reference frame; Ch3: DC side voltage; Ch4:output current in synchronously rotating reference frame.

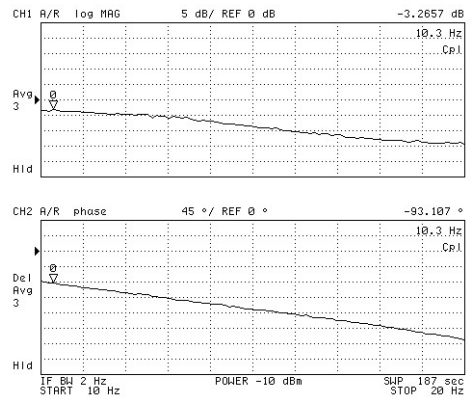

Fig. 21. Bode diagram of current control loop.

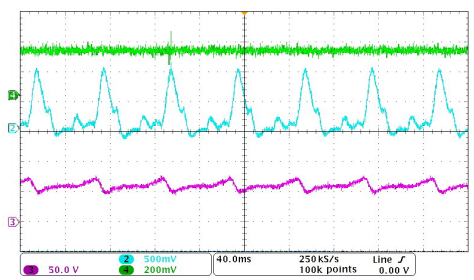

Fig. 22. Unstable current control loop. L=2.2mH, Ch2:reference current in synchronously rotating reference frame; Ch3: DC side voltage; Ch4:output current in synchronously rotating reference frame.

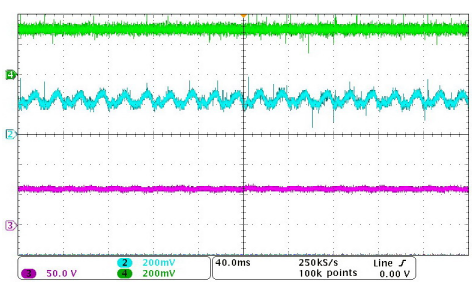

Fig. 23. Stable current control loop. L=5.5mH, Ch2:reference current in synchronously rotating reference frame; Ch3: DC side voltage; Ch4:output current in synchronously rotating reference frame.

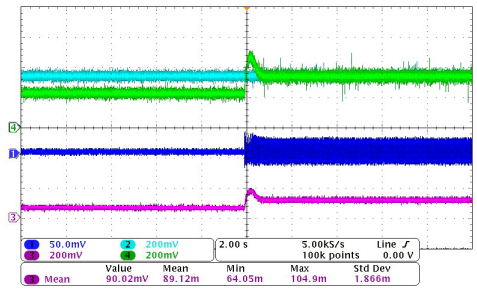

Fig. 24. DC side voltage response of dynamic process. Ch1:output current in *abc* frame; Ch2:reference voltage in synchronously rotating reference frame; Ch3: DC side voltage; Ch4:DC side voltage in synchronously rotating reference frame.

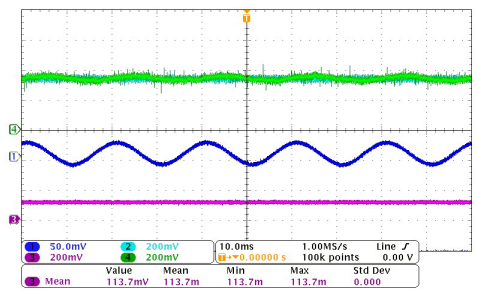

Fig. 25. DC side voltage response of stead-state. Ch1:output current in *abc* frame; Ch2:reference voltage in synchronously rotating reference frame; Ch3: DC side voltage; Ch4:DC side voltage in synchronously rotating reference frame.

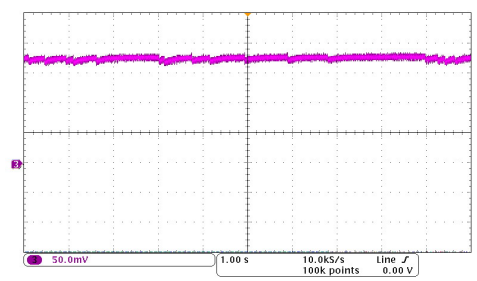

Fig. 26. Unstable voltage control loop with C=3333μF.

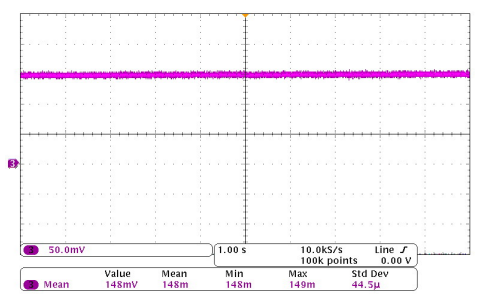

Fig. 27. Stable voltage control loop with C=6666μF.

frequency, and it can be obtained according to (24).

$$\gamma = 90^\circ + \arctan\frac{\omega_0 L I_\mathrm{m}}{E_\mathrm{m} + 2RI_\mathrm{m}} \tag{23}$$

$$\omega_0 = \frac{3k_{\mathrm{P2}}}{2Cu_{dc0}} E_\mathrm{m} \Bigg/ \sqrt{1 - \left(\frac{3k_{\mathrm{P2}}}{2Cu_{\mathrm{dc0}}} L I_\mathrm{m}\right)^2} \tag{24}$$

The phase margin γ considered as one of the variables can be used to design the capacitor. It is good for the stability and reliably of the whole STATCOM system. The capacitor can be designed by using (25). The more the capacitor increases, the bigger the phase margin is. An example is shown in Fig. 16, where k_{P1}=0.2, k_{P2}=0.8, L=5mH, R=0.08Ω, E_m=8164V, and I_m=-164A.

$$C \approx \frac{3k_{\mathrm{P2}}\sqrt{1+\tan^2(\gamma - 90^\circ)}}{2u_{dc0}\tan(\gamma - 90^\circ)} \tag{25}$$

V. Simulation and Experimental Results

In order to verify the analysis and specifications, simulation and hardware experimental investigations were carried out. The current response and the DC side voltage response are shown in Fig. 17 and Fig. 18. From the simulation results, the analysis of the model of is verified.

The low voltage hardware experiment is presented in Fig. 19 to Fig. 27. In terms of the current control loop, in Fig. 19 and Fig. 20, the output current can track the reference current. In order to verify the current loop model, in the experiment, an Agilent 4395A Network/Spectrum/Impedance Analyzer was used to analyze the current control loop, in Fig. 21. The lowest frequency of the equipment is 10Hz. However, the cut-off frequency could be read, and it was approximately 10Hz. There was a time delay of 37degrees because of the calculation time. The experimental result verified the analysis of the current control loop.

Fig. 22 and Fig. 23 verify (15). When the interface inductor was 2.2mH, the STATCOM system was unstable and the output current oscillated. When the interface inductor was increased to 5.5mH, the STATCOM system was stable. It verified the conclusion in (15), that the more the inductor is increased, the bigger the phase margin becomes.

In terms of the DC side voltage control loop, from Fig. 24 and Fig. 25, the DC side voltage can track the reference voltage. The experimental result verified the analysis of the DC side voltage control loop.

Fig. 26 and Fig. 27 verify (23). When the DC side capacitor was 3333μF, the STATCOM system was unstable and the voltage oscillated. When the DC side capacitor was increased to 6666μF, the STATCOM system was stable. It verified the conclusion in (23), that the more the DC side capacitor is increased, the bigger the phase margin becomes.

VI. Conclusions

In this paper, a model of the phase and amplitude control is presented. A detailed analysis of the influences of the interface inductor and the DC side capacitor on the STATCOM systems and the corresponding design considerations are presented. The influences of the interface inductor and the DC side

capacitor on the STATCOM system stability and filtering characteristics are extensively investigated. A method based on the phase margin to design the interface inductor and the DC side capacitor is presented in this paper.

ACKNOWLEDGMENT

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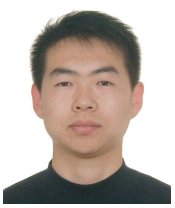

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