JPE 12-2-2

http://dx.doi.org/10.6113/JPE.2012.12.2.242

Switching-Mode BJT Driver for Self-Oscillated Push-Pull Inverters

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Abstract

Self oscillating current fed push pull resonant inverters can be controlled without using special drivers. Dc current flows through the choke coil and the power switches, although the driving signals of the power switches are sinusoidal. When the base current is near zero, the transistors cannot be operated in switching mode. Hence higher switching power losses and instantaneous peak power during off transitions are observed. In this study, an alternative design has been proposed to overcome this problem. A prototype circuit has been built which provides dc bias current to the base of the transistors. Experimental results are compared with theoretical calculations to demonstrate the validity of the design. The proposed design decreases the peak and average power losses by about 8 times, when compared to conventional designs.

Key words: Current Fed Inverter, Self Oscillated Push Pull Inverter, Switching Mode, Transistor Drive Circuit

I. INTRODUCTION

High frequency dc-ac inverters are used in many applications such as motor control and induction heating systems, electronic ballasts [1] and power supplies [2]. In high frequency inverters, the driving scheme can be designed by using an integrated circuit (IC) or by using self oscillating techniques. The gate drive circuits of self oscillating inverters have some advantages over others. The main advantages are low cost, simple structure, not requiring an auxiliary power supply and no switching frequency limitations due to ICs. It has also a disadvantage which is that desired switching frequencies may not be met, due to the tolerances of components [3].

In medium and low power level inverters, MOSFETs and BJTs are commonly used as switching devices [1] ,[4]-[11]. Generally MOSFETs are driven with ICs which increases the cost of the circuit. In many self oscillating inverter design topologies such as push pull and half bridge topologies, BJTs are used as power switches [12]-[21]. In self oscillating current fed applications, the base current of the BJT is in sinusoidal form while the collector current of the transistor is in dc. Because of this, driving BJTs in switching mode becomes a challenge.

In this paper, a solution is proposed in order to drive BJTs in switching mode. A prototype drive circuit for a 65W current fed self oscillating push pull inverter is designed and experimented on.

Manuscript received Mar. 24, 2011; revised Dec. 12, 2011
Recommended for publication by Associate Editor Yong-Chae Jung.
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II. CONVENTIONAL SELF OSCILLATED CURRENT FED PUSH PULL INVERTER

Current and voltage fed self oscillating topologies are used in some power electronic applications. Voltage fed inverters suffer from large start up voltage and current transients. Current fed circuits yield a cleaner sinusoidal waveform than voltage fed circuits.

Fig. 1 shows a self oscillated current fed push pull inverter. The circuit is made up of a push pull transformer (TR), a start up resistance (R3), a choke (Ldc), a dc power supply, a resonance capacitor (Cr), a magnetizing inductance of the push pull transformer (Lr), power transistors (Q1 and Q2) and a load. The conduction duty cycle of each switch is 50% and they are driven by the auxiliary windings of the push pull transformer. The resonant frequency of the circuit, that is the switching frequency, depends on Lr and Cr. This can be calculated from Equation (1).

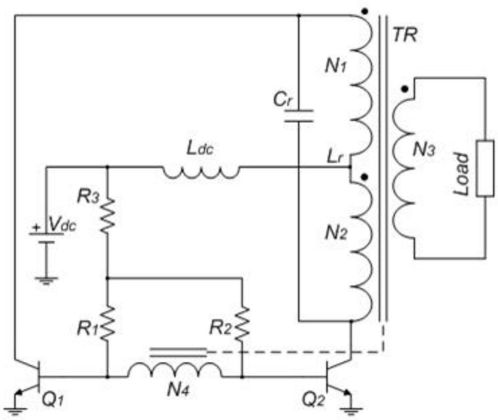

Fig. 1. Self oscillated current fed push pull inverter.

$$f_r = \frac{1}{2 \times \pi \times \sqrt{L_r \times C_r}} \quad (1)$$

The size of the choke is designed to be large enough so that the current which flows into the tap of the primary of the push pull transformer is changed into dc form. The same dc current also flows through the power switches. In this topology, while the collector current is dc, the applied base-emitter voltage of the transistor is ac due to nature of the oscillating topology. Therefore, transistors cannot be driven well in switching mode. This creates a significant problem during switching transitions. The switching power losses of the transistors become higher when the base current is near the zero crossings which causes the transistors to warm up. Heat sinks may become a necessity and the system's efficiency decreases. All of these problems can be avoided by applying an appropriate driving signal to the base of the transistor. That is what is proposed in this paper.

III. Proposed BJT Driver For Self Oscillated Current Fed Push Pull Inverters

As explained in the previous section, driving the transistors in switching mode becomes a challenge. In order to overcome this problem, a new drive circuit, depicted in Fig. 2, is proposed.

Rectified voltage of the secondary winding (Ns) of the choke is applied to the base-emitter of the transistors. The rectified voltage provides some dc current which is independent of the resonant circuit. In this way, some additional current flows to the base of the transistors, when the base-emitter voltage is near zero. To drive the transistor when it is in switch mode, the ratio of the collector and base currents must be equal to the transistor gain.

In order to calculate enough base current, some mathematical analysis needs to be completed. In Fig. 3, a

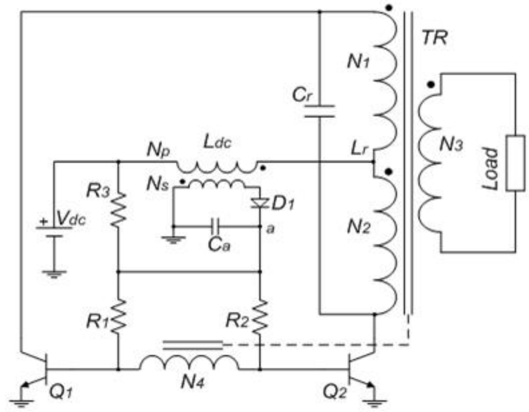

Fig. 2. Self oscillated current fed push pull inverter with the proposed drive circuit.

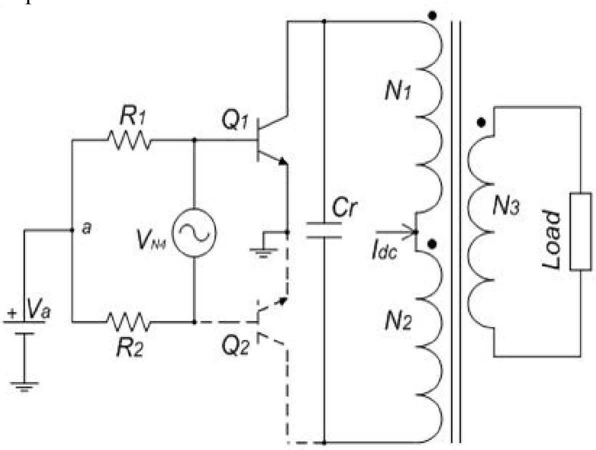

Fig. 3. Simplified equivalent circuit while Q1 is on.

simplified circuit of the design is shown. From the requirement of the load power and the previously estimated efficiency, the power supply current can be calculated. The supply current is the summation of the collector currents.

The base current can be obtained from two different sources, as shown in Fig. 3. The first of which is from the push pull transformer which is modeled as an ac source (VN4) in the figure. The second one is from the choke inductor which is illustrated as a dc source (Va).

From Fig. 3, the average base current can be calculated as follows:

$$I_{B(avg)} = \frac{\frac{2}{\pi} \times \frac{N_4}{N_1} \times \frac{V_{dc} \times \pi}{2}}{R_B} + \frac{\frac{N_S}{N_P} \times V_{dc} \times -V_F - V_{BE}}{R_B/2} \quad (2)$$

where:

N1: Push pull transformer primary turn number
N4: Push pull transformer auxiliary winding turn number
NP: Choke primary turn number
NS: Choke secondary turn number
VF: Diode D1 forward voltage (V)
VBE : The transistor base-emitter voltage (V)
RB= R1=R2 : Base resistance (Ω)

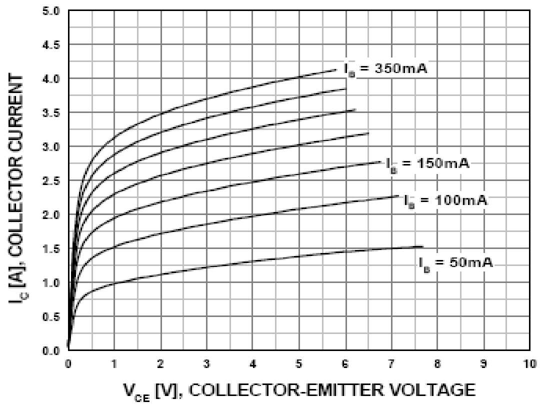

Fig. 4. FJP5321 $I_C - V_{CE}$ characteristic curve [22].

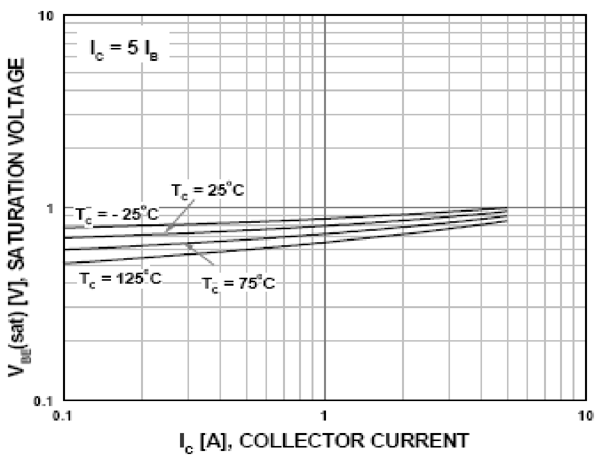

Fig. 5. FJP5321 $I_C - V_{BE}$ characteristic curve [22].

IV. Implementation of the Proposed Design

In this paper, a drive circuit for a high frequency push pull inverter is designed. The inverter has a 130V of dc input and 65W of output. In order to determine the collector current, the efficiency is assumed to be 95%, which is based on practical engineering experience. Therefore, the dc power supply current becomes 0.526A. The voltage, current and resonant frequencies are taken into account for the selection of the BJTs. Among the many possible options, a FJP5321 is selected to be used as power a switch in the inverter.

Depending on the base and collector currents, the transistors can be in different operating points, as shown in Fig. 4. In order to drive the transistor in switching mode, an operating point is selected so that the transistor requires the minimum base current and it has the minimum collector emitter voltage at the desired collector current. In this application, approximately a 50mA base current is enough to drive the transistors in switching mode.

From Fig. 4, for a 50mA base current, the collector emitter voltage (VCE) is less than 0.5 V. From Fig. 5 the base emitter voltage (VBE) is around 1 V [22]. This is acceptable for a switch mode power supply.

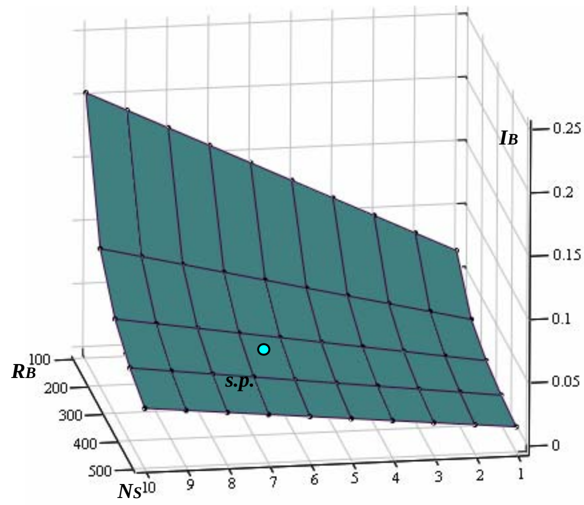

Fig. 6. Change of base current with base resistance and choke coil secondary turn number (IB:0-0.25A, RB:100-500Ω, NS:1-10 turn).

In Equation (2), all of the variables except NS, N4 and RB have already been determined during the inverter design. From the transistor data sheet, the maximum VEBO value has a limit of 7V. The voltage across N4 must be less than the value of VEBO. Because of this, N4 has a single turn in this application and it is not considered as a variable. Fig. 6 shows a solution surface for different base currents which satisfy Equation (2). In this design, NS and RB are selected as 7 turns and 330Ω respectively in order to meet the 50mA base current requirement.

Equation (2) can be separated into two parts to show both of the base sources shown in Fig. 3. The first one, defined in Equation (3), generates some dc offset current to the base.

$$I_{B1(avg)} = \frac{\frac{N_S}{N_P} \times V_{dc} \times -V_F - V_{BE}}{R_B/2} \tag{3}$$

The other one, defined in Equation (4), drives the transistor at the resonant frequency.

$$I_{B2(avg)} = \frac{\frac{2}{\pi} \times \frac{N_4}{N_1} \times \frac{V_{dc} \times \pi}{2}}{R_B} \tag{4}$$

V. Experimental Results and Their Comparison

TABLE I

CIRCUIT PARAMETERS

V_{dc}	130	V	N_1	40	*turns*
P_o	65	W	N_4	1	*turns*
V_{load}	127	V	N_P	128	*turns*
R_B	330	Ω	N_S	7	*turns*
V_{BE}	0.75	V	N_3	38	*turns*
V_F	1	V	C_r	36	*nF*
L_r	1.568	*mH*	f_r	22	*kHz*
R_3	100k	Ω			

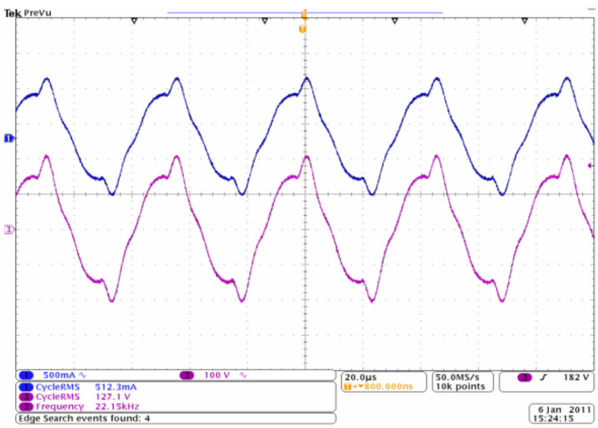

Fig. 7. Load current (CH1) and voltage (CH2).

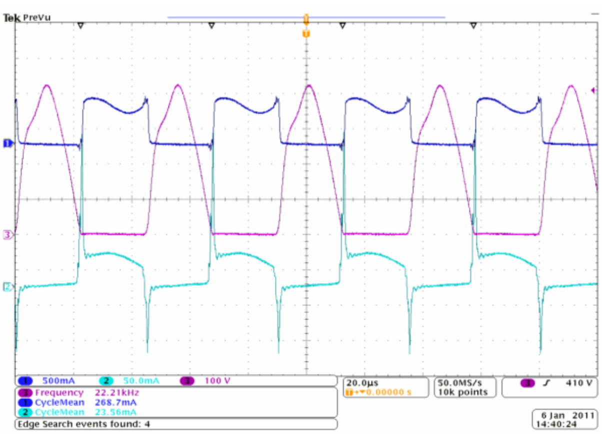

Fig. 8. Transistor collector current (CH1) and base current (CH2) and collector-emitter voltage (CH3).

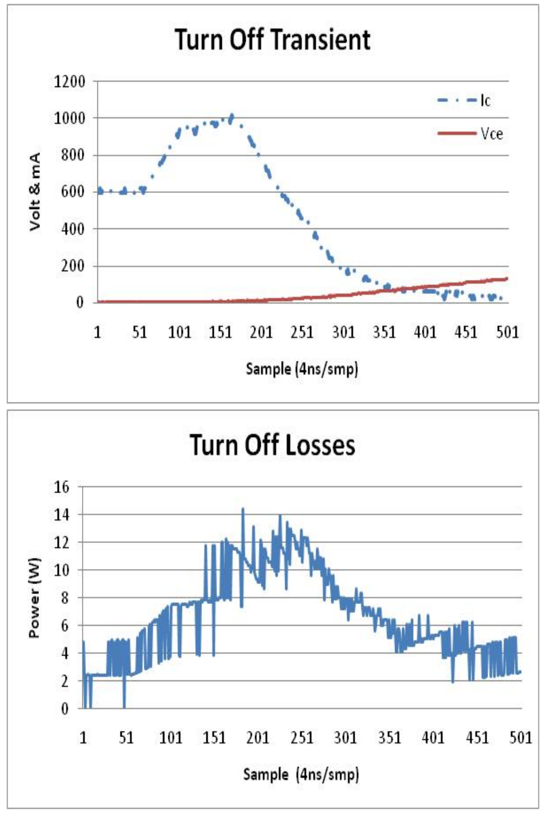

Fig. 9. V_{CE} , I_C and instantaneous power loss for the proposed circuit during turn off transients (4 ns / smp x 500 smp = 2μs).

To verify the performances of both the proposed and conventional designs, the waveforms of the base and collector currents and the transistor turn off power losses are compared in this section.

The base emitter voltage, VBE, and the diode conduction voltage drop, VF, are obtained from the transistor and the 1N4148 diode data sheets [22], [23]. N1, N4, NP and fr are obtained from the push pull inverter design. RB and NS are calculated from Equations (3) and (4). The circuit parameters are listed in Table 1. From Equation (3) and Equation (4), the average currents are calculated as 32.48mA and 10mA respectively.

The output current and voltage are shown in Fig. 7. The rms values of the current and voltage are measured as 512mA and 127V respectively. The output power becomes 65W.

When the proposed technique is implemented, the collector and base currents and the collector emitter voltage of Q1 are shown in Fig. 8. In the same figure, the average values of both currents and the resonant frequency are denoted.

As mentioned earlier, the transistors are on for 50% of the resonant period and the average collector current of Q1 is measured as 0.268A. Therefore, the average collector current during on time becomes (2x0.268mA) 0.536A. The average base current is measured as 23.5mA. Therefore, the average

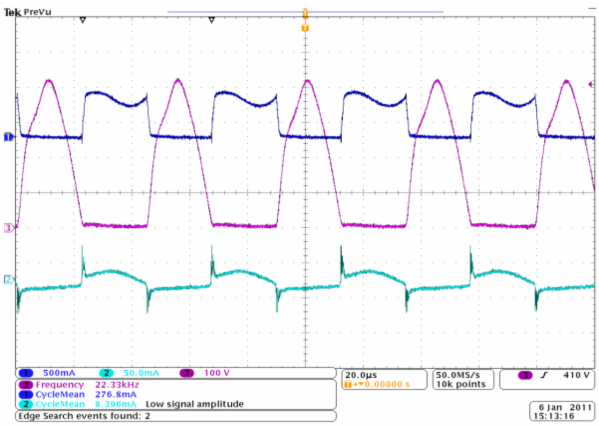

Fig. 10. Transistor collector (CH1) and base current (CH2) and transistor collector-emitter voltage (CH3).

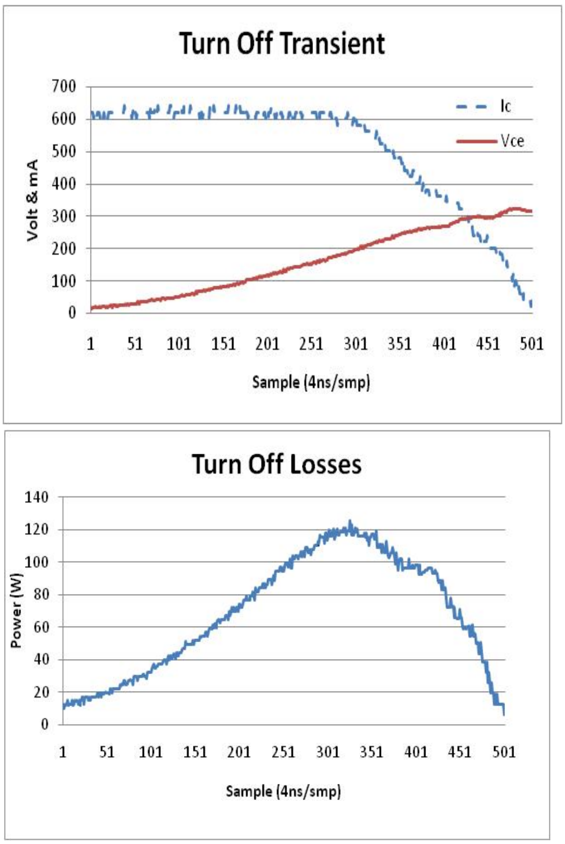

Fig. 11. V_{CE} , I_C and instantaneous power loss for the conventional circuit during turn off transients (4 ns / smp x 500 smp = 2μs).

base current during on time becomes (2x23.5mA) 47mA.

The switching loss of the transistor is improved with the proposed circuit. In order to observe its performance, the turn off loss of the transistor is analyzed.

Fig. 9 shows the turn off transition data obtained from Fig. 8. During the transition, the instantaneous peak power reaches 14W. The average value of the turn off losses in a resonant period is calculated as 0.15W. The efficiency of the inverter is measured as 93%.

TABLE II

EXPERIMENTAL AND DESIGN RESULTS

Current (mA)	***Calculated***	***Measurement***	
		Proposed	***Conventional***
$I_{C(avg)}$	526	536	552
$I_{B(avg)}$	42.48	47	16.8

TABLE III

POWER LOSS COMPARISON

Turn off Power Losses (W)	***Proposed***	***Conventional***
Peak	14	120
Average over resonant period	0.15	1.2

When the proposed solution is not used, the drive circuit is shown in Fig. 1. As can be seen, the power loss of the transistor becomes higher. Fig. 10 shows the collector and base currents and the collector emitter voltage of Q1 as well as the average values of both currents and the resonant frequency.

The average collector current of the transistor in a resonant period is 0.276A. Therefore, the average of the collector current during on time becomes (2x0.276mA) 0.552A. The average base current during on time becomes (2x8.4mA) 16.8mA.

Fig. 11 shows the turn off transition data obtained from Fig. 10. During the transition, the instantaneous peak power reaches 120W. The average value of the turn off losses in a resonant period is calculated as 1.2W. The efficiency of the inverter is measured as 90%.

The results of the calculations and experiments are illustrated in Table 2 and Table 3. With the proposed drive circuit, the transistor base current requirement for switching mode operations is improved. As a result, both the peak and average switching power losses are decreased.

VI. CONCLUSIONS

In this paper, the base drive circuit of a self oscillated current fed push pull inverter is analyzed. In order to drive the transistors in switching mode, enough base current is required. However, self oscillating circuits have sinusoidal voltage and current. In conventional base drive circuits, when the base current is around zero, the transistors cannot be in switching mode. Because of this, the instantaneous peak power of the switching loss and the circuit efficiency become a concern. A 65W self oscillated current fed push pull inverter with the proposed drive circuit has been built. The theoretical calculations were verified by experimental results. With the prototype design, the switching loss is decreased and the instantaneous peak power is significantly lowered.

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