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Interleaved DC-DC Converters with Partial Ripple Current Cancellation

Bor-Ren Lin†, Huann-Keng Chiang*, and Chih-Yuan Cheng*

†*Dept. of Electrical Eng., National Yunlin University of Science and Technology, Yunlin, Taiwan

Abstract

An interleaved PWM converter is proposed to implement the features of zero voltage switching (ZVS), load current sharing and ripple current reduction. The proposed converter includes two ZVS converters with a common clamp capacitor. With the shared capacitor, the charge balance of the two interleaved parts is automatically regulated under input voltage and load variations. The active-clamping circuit is used to realize the ZVS turn-on so that the switching losses on the power switches are reduced. The ZVS turn-on of all of the switching devices is achieved during the transition interval. The interleaved pulse-width modulation (PWM) operation will reduce the ripple current and the size of the input and output capacitors. The current double rectifier (CDR) is adopted in the secondary side to reduce output ripple current so that the sizes of the output chokes and capacitor are reduced. The circuit configuration, operation principles and design considerations are presented. Finally experimental results based on a 408W (24V/17A) prototype are provided to verify the effectiveness of the proposed converter.

Key words: Current Doubler Rectifier, DC Converter

I. INTRODUCTION

Soft-switching converters [1]–[17] have been developed to achieve the features of a high power density and a high efficiency with a high switching frequency and zero voltage turn-on. Asymmetrical half-bridge converters [1], [2] have the ZVS feature to turn on the power switch so that the switching losses can be reduced. However, the primary voltage of the transformer is related to the duty ratio and the magnetizing inductance has a dc current. The voltage and current stresses of the semiconductors at the secondary side are also related to the duty ratio. The phase-shifted full-bridge converter [3], [4] is one kind of popular topology to achieve zero voltage switching (ZVS) turn-on. The voltage rating of the power switches is clamped to the input voltage. However, the drawbacks of the full-bridge converter are a large number of switches and a low efficiency under a light load. Multilevel converters [5], [6] can realize ZVS turn-on and reduce the voltage rating of the switches. But the control scheme is very complicated and not easy to implement using analog commercial IC's. Resonant converters [7], [8] have been presented to regulate the output voltage and to realize ZVS turn-on with a variable switching frequency. Although the switches can be turned on at zero voltage switching (ZVS), the disadvantages of the resonant converters are a variable switching frequency and high voltage or current stresses on power semiconductors especially for high voltage or high current applications. The active-clamping topology [9], [10] is one kind of soft switching technique to achieve ZVS turn-on by utilizing the energy stored in the leakage and magnetizing inductances. Thus the voltage rating of the power switch is clamped to the input voltage and the clamping capacitor voltage. Thus the voltage rating of the switch in the active-clamping forward converter is lower than the voltage rating in the conventional forward converter. Interleaved forward converters [11]-[14] have been proposed to reduce the size of the magnetizing components and to reduce the power losses and the thermal stresses on the power switches. The interleaved PWM technique is a paralleling technique with a phase shift over a switching period to reduce the ripple current at the input and output sides.

This paper presents an interleaved converter to achieve the features of low switching losses, ZVS turn-on, low voltage stress of the clamp capacitor and less ripple current at the output side. Two converter cells are connected in parallel on the input and output sides to reduce the current stresses on the output passive components and the transformers. Two active-clamping circuits with only one clamp capacitor are used to realize the ZVS turn-on for all of the switching devices. Current doubler rectifiers are used in the secondary side. The advantages of a current doubler rectifier are its one diode conduction drop, ripple current reduction on the output inductors and low current rating for transformer secondary winding. The interleaved PWM scheme is used to drive the power switches so that the current ripples on the input and output capacitors are reduced. Thus, the size and weight of the output capacitor are reduced. Finally, experiments based on a laboratory prototype with 408W of rated power are presented to verify the circuit performance.

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†Corresponding Author:linbr@yuntech.edu.tw
Tel: +886-5-5517456, Nat'l Yunlin Univ. of Science and Tech.
*Dept. of Electrical Eng., National Yunlin University of Science and Technology, Taiwan

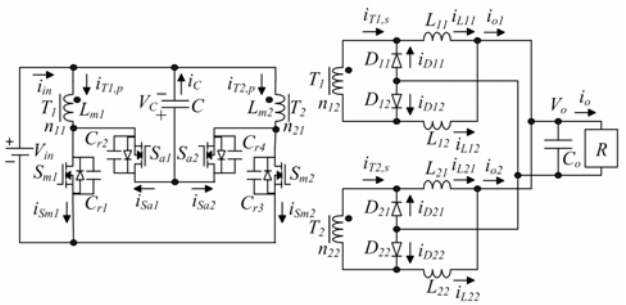


Fig. 1. Circuit configuration of the proposed interleaved ZVS converter.

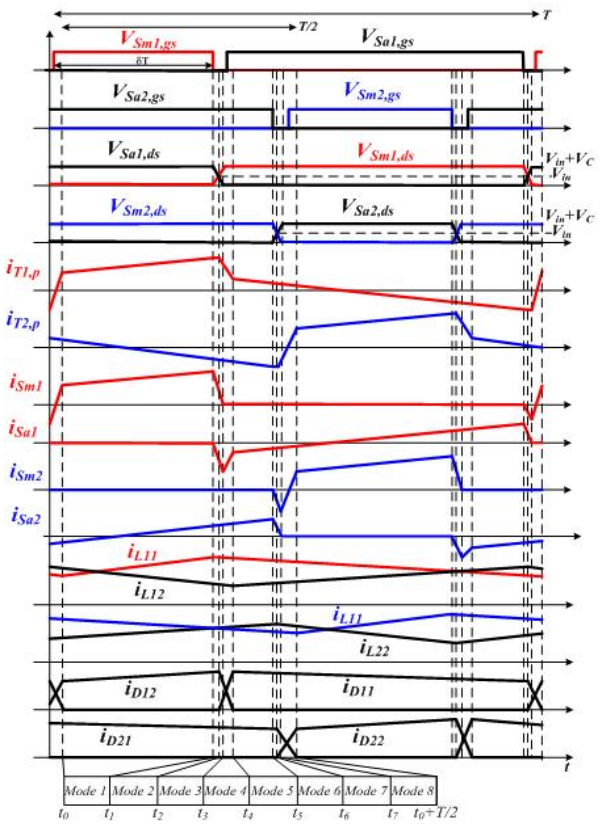


Fig. 2. Key waveforms of the proposed converter.

II. CIRCUIT CONFIGURATION

The circuit configuration of the proposed interleaved converter is shown in Fig. 1. There are two converter modules in the proposed converter. V_{in} and V_o are the input and output voltages. Converter 1 includes V_{in}, T_1, S_{m1}, S_{a1}, C, C_{r1}, C_{r2}, D_{11}, D_{12}, L_{11}, L_{12} and C_o. In the same manner, converter 2 includes V_{in}, T_2, S_{m2}, S_{a2}, C, C_{r3}, C_{r4}, D_{21}, D_{22}, L_{21}, L_{22} and C_o. L_{m1} and L_{m2} are the magnetizing inductances of the transformers T_1 and T_2, respectively. S_{m1} and S_{a1} are main and auxiliary switches in converter 1. S_{m2} and S_{a2} are main and auxiliary switches in converter 2. C is the clamp capacitance to limit the voltage stresses on all of the switches. C_{r1}~C_{r4} are the resonant capacitances. In the secondary side of the transformers T_1 and T_2, two current doubler rectifiers are connected in parallel at the output side. Based on the current doubler rectifier, the output inductor currents partially cancelled each other out and the resultant output ripple current is reduced. Since the two current doubler rectifiers are connected in parallel so that the current stresses of the transformer secondary winding and the copper losses on the output chokes are reduced. Two interleaved converters share the same clamp capacitor C to limit the voltage stresses of all the switches. Switches S_{m1} and S_{m2} are operated by the interleaved PWM scheme. Based on the shared capacitor C, the charge balance of the two interleaved parts is automatically regulated under input voltage and load variations. The interleaved PWM operation further reduces the ripple current and the size of the output capacitor. During the commutation intervals of S_{m1} and S_{a1}, C_{r1}, C_{r2} and leakage inductance of T_1 are resonant to achieve ZVS turn-on of switches S_{m1} and S_{a1} in converter 1. In the same manner, C_{r3}, C_{r4} and leakage inductance of T_2 are resonant in the commutation interval to achieve ZVS turn-on of S_{m2} and S_{a2} in converter 2. Thus all of the power switches are turned on under ZVS in the proposed converter.

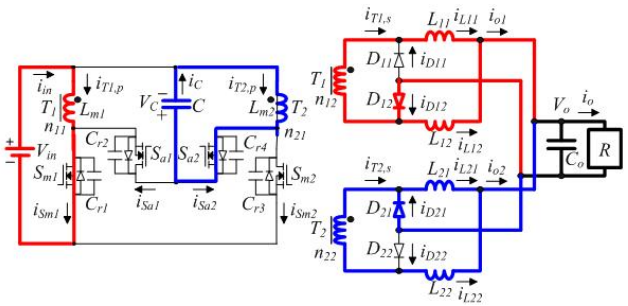
III. OPERATION PRINCIPLE

The key waveforms of the proposed converter in a switching cycle are given in Fig. 2. Based on the on/off states of S_{m1}~S_{a2} and D_{11}~D_{22}, there are eight operation modes during a half switching cycle. Fig. 3 gives the equivalent circuits of each operating mode. In the proposed converter, all of the semiconductors are ideal except for their output capacitances and body diodes. The power transformers T_1 and T_2 are modeled by ideal transformers with the magnetizing inductances L_{m1} and L_{m2} and the leakage inductances L_{lk1} and L_{lk2}. The leakage inductances L_{lk1} and L_{lk2} are much less than the magnetizing inductances L_{m1} and L_{m2}. The capacitances of C and C_o are much greater than the capacitances of C_{r1}~C_{r4}. The turns ratio of the primary winding to the secondary winding of T_1 and T_2 is $n=N_p/N_s$. The energy stored in the leakage inductances L_{lk1} and L_{lk2} are greater than energy stored in the resonant capacitances C_{r1}~C_{r4} to achieve ZVS operation of all of the switches. Prior to time t_0, the switches S_{m1} and S_{a2} are in the on-state and the rectifier diodes D_{11} and D_{12} are in the commutation interval.

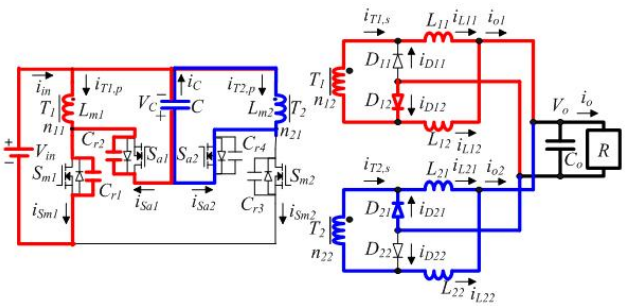
***Mode 1* [$t_0 \le t < t_1$]:** At time t_0, the diode current i_{D11} decreases to zero and turns off. For converter 1, the power is transferred to the output load through V_{in}, T_1, S_{m1}, D_{12}, L_{11} and C_o. The voltage across the leakage inductor L_{lk1} and the magnetizing inductance of T_1 are V_{in}. Thus, the primary current $i_{T1,p}$ and the output inductor current i_{L11} increase. The output inductor current i_{L12} decreases with the slope of $-V_o/L_{12}$. For converter 2, the voltage across the primary winding of T_2 equals $-V_C$. The primary current $i_{T2,p}$ decreases. The energy stored in the leakage and magnetizing inductances of T_2 is transferred to the output load through C, S_{a2}, T_2, D_{21}, L_{22} and C_o. The output inductor currents i_{L21} and i_{L22} are decreased and increased, respectively. The primary currents $i_{T1,p}$ and $i_{T2,p}$ are expressed as:

$$i_{T1,p}(t) \approx i_{T1,p}(t_0) + \frac{kV_{in}}{L_m}(t-t_0) + \frac{i_{L11}(t)}{n},$$

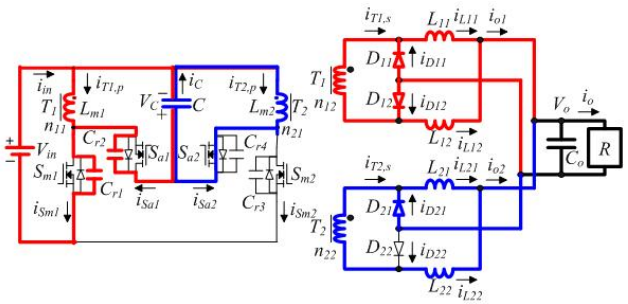
$$i_{T2,p}(t) \approx i_{T2,p}(t_0) - \frac{kV_C}{L_m}(t-t_0) - \frac{i_{L22}(t)}{n} \qquad (1)$$



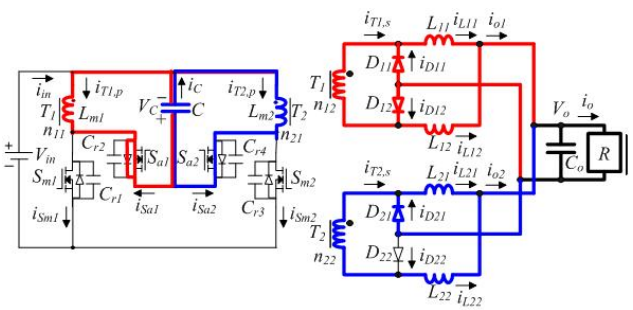
(a) mode 1 (t_0~t_1).



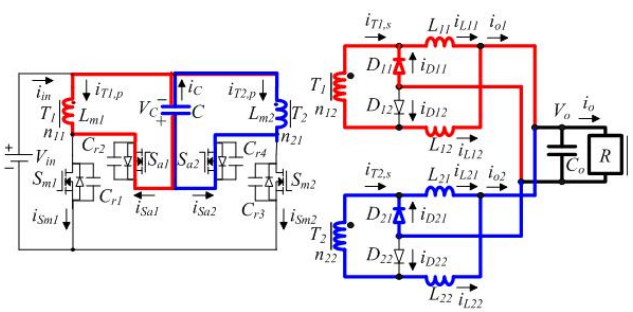
(b) mode 2 (t_1~t_2).



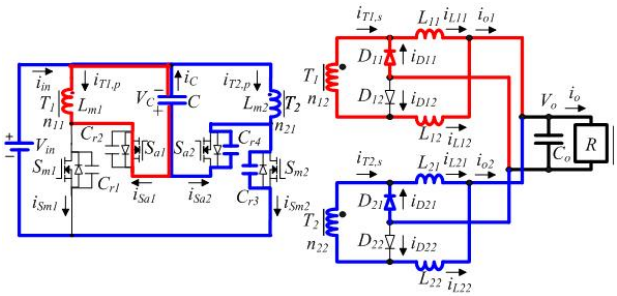
(c) mode 3 (t_2~t_3).



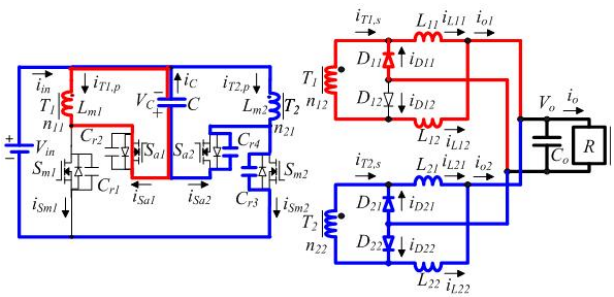
(d) mode 4 (t_3~t_4).



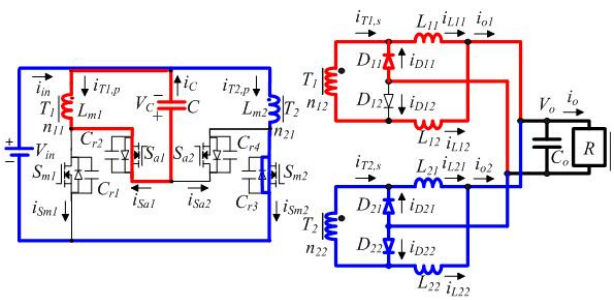
(e) mode 5 (t_4~t_5).



(f) mode 6 (t_5~t_6).



(g) mode 7 (t_6~t_7).



(h) mode 8 (t_7~t_0+T/2).

Fig. 3. Operation modes of the proposed converter during the first half of the switching cycle.

where $k=L_m/(L_m+L_{lk})$. The output inductor currents are expressed as:

$$i_{L11}(t) \approx i_{L11}(t_0) + \frac{kV_{in}/n - V_o}{L_{11}}(t-t_0),$$

$$i_{L12}(t) \approx i_{L12}(t_0) - \frac{V_o}{L_{12}}(t-t_0),$$

$$i_{L21}(t) \approx i_{L21}(t_0) - \frac{V_o}{L_{21}}(t-t_0),$$

$$i_{L22}(t) \approx i_{L22}(t_0) + \frac{kV_C/n - V_o}{L_{22}}(t-t_0) \qquad (2)$$

This mode ends at time t_1 when the main switch S_{m1} is turned off.

***Mode 2* [$t_1 \le t < t_2$]:** At time t_1, S_{m1} is turned off and $i_{T1,p}$ is positive. The current $i_{T1,p}$ charges capacitor C_{r1} from zero to V_{in} and discharges capacitor C_{r2} from $V_{in}+V_C$ to V_C.

$$v_{Cr1}(t) \approx \frac{i_{T1,p}(t_1)}{2C_r}(t-t_1),$$

$$v_{Cr2}(t) \approx V_{in} + V_C - \frac{i_{T1,p}(t_1)}{2C_r}(t-t_1) \qquad (3)$$

where $C_{r1}=C_{r2}=C_{r3}=C_{r4}\equiv C_r$. To ensure that capacitor C_{r2} is discharged to zero voltage, the energy stored in leakage inductor L_{lk1} must be greater than the energy stored in capacitors C_{r1} and C_{r2} at time t_1. Since the capacitances C_{r1} and C_{r2} are small, the time interval in this mode is fast enough to be neglected. The switch current i_{Sm1} decreases from $i_{T1,p}(t_1)$ and the switch current i_{Sa1} decreases from zero. In this mode, the primary current $i_{T1,p}$ is greater than the magnetizing current i_{Lm1} so that diode D_{12} is still conducting. At time t_2, the capacitor voltages $v_{Cr1}=V_{in}$ and $v_{Cr2}= V_C$. At this instant, the magnetizing voltage of T_1 is zero. Thus diodes D_{11} and D_{12} are both conducting. From (3), the time interval in this mode can be obtained.

$$\Delta t_{12} = t_2 - t_1 \approx \frac{2C_r V_{in}}{i_{T1,p}(t_1)} \tag{4}$$

The operation of converter 2 in this mode is the same as the operation in mode 1.

***Mode 3* [$t_2 \le t < t_3$]:** At time t_2, the capacitor voltages $v_{Cr1}=V_{in}$ and $v_{Cr2}=V_C$ such that the primary voltage of T_1 is zero. The diodes D_{11} and D_{12} are in the commutation interval. The diode current i_{D11} increases and i_{D12} decreases. Capacitor C_{r1} is continuously charged from V_{in} to $V_{in}+V_C$ and capacitor C_{r2} is discharged from V_C to zero. This mode ends at time t_3 when the capacitor voltage $v_{Cr2}(t_3)=0$ and the anti-parallel diode of S_{a1} is conducting. The time interval in this mode is expressed as:

$$\Delta t_{23} = t_3 - t_2 \approx \frac{2C_r V_C}{i_{T1,p}(t_1)} \tag{5}$$

The operation of converter 2 in this mode is the same as the operation in mode 1.

***Mode 4* [$t_3 \le t < t_4$]:** At time t_3, $v_{Cr2}=0$. Since $i_{Sa1}(t_3)$ is negative, the anti-parallel diode of S_{a1} is conducting. Therefore, S_{a1} can be turned on at this instant to realize ZVS. In this mode, the diodes D_{11} and D_{12} are still in the commutation mode. The magnetizing voltage v_{Lm1} is zero so that the leakage inductor voltage v_{lk1} is equal to $-V_C$. The primary current $i_{T1,p}$ decreases linearly with the slope of $-V_C/L_{lk1}$. This mode is operated continuously until $i_{D12}=0$ at time t_4. Then diode D_{12} is turned off. The operation of converter 2 in this mode is the same as the operation in mode 1.

***Mode 5* [$t_4 \le t < t_5$]:** At time t_4, S_{a1} and S_{a2} are all in the on-state. The voltage stresses of S_{m1} and S_{m2} are equal to $V_{in}+V_C$. The primary winding voltages of T_1 and T_2 are equal to $-V_C$. The secondary winding voltages of T_1 and T_2 are all negative. Thus diodes D_{11} and D_{21} are conducting and D_{12} and D_{22} are off. Therefore, the primary side currents $i_{T1,p}$ and $i_{T2,p}$ decrease. In converter 1, the energy stored in leakage inductance L_{lk1} is transferred to output capacitor C_o through S_{a1}, C, T_1, D_{11} and L_{12}. In the same manner, the energy stored in leakage inductance L_{lk2} is transferred to output capacitor C_o through S_{a2}, C, T_2, D_{21} and L_{22} in converter 2. The output inductor currents i_{L11} and i_{L21} decrease and i_{L12} and i_{L22} increase. This mode ends at time t_5, when switch S_{a2} is turned off.

***Mode 6* [$t_5 \le t < t_6$]:** At time t_5, S_{a2} turns off. The components of C_{r3}, C_{r4} and L_{lk2} are resonant during this mode. Since the capacitances of C_{r3} and C_{r4} are very small, the interval in this mode is fast enough to be neglected. The primary current $i_{T2,p}$ is almost constant. The switch currents i_{Sa2} and i_{Sm2} both decrease. Capacitor C_{r3} is discharged from $V_{in}+V_C$ to V_C and capacitor C_{r4} is charged from zero voltage to V_{in}.

$$v_{Cr3}(t) \approx V_{in} + V_C + \frac{i_{T2,p}(t_5)}{2C_r}(t - t_5),$$

$$v_{Cr4}(t) \approx -\frac{i_{T2,p}(t_5)}{2C_r}(t - t_5) \tag{6}$$

where $i_{T2,p}(t_5)$ is negative. In this mode, the primary current $i_{T2,p}$ is less than the magnetizing current i_{Lm2} so that diode D_{21} is still conducting. To ensure C_{r3} can be discharged to zero voltage, the energy stored in leakage inductor L_{lk2} must be greater than the energy stored in capacitors C_{r3} and C_{r4} at time t_5. At time t_6, the capacitor voltages $v_{Cr3}=V_{in}$ and $v_{Cr4}=V_C$. At this instant, the primary voltage of T_2 is zero. Thus diodes D_{21} and D_{22} are both conducting. From (6), the time interval in this mode can be derived as:

$$\Delta t_{56} = t_6 - t_5 \approx \frac{2C_r V_C}{-i_{T2,p}(t_5)} \tag{7}$$

***Mode 7* [$t_6 \le t < t_7$]:** At time t_6, $v_{Cr3}=V_{in}$ and $v_{Cr4}=V_C$ so that the primary voltage of T_2 is zero. Diodes D_{21} and D_{22} are in the commutation interval. The diode current i_{D21} decreases and i_{D22} increases. Capacitor C_{r4} is continuously charged from V_C to $V_{in}+V_C$ and capacitor C_{r3} is discharged from V_{in} to zero voltage. This mode ends at time t_7, when the capacitor voltage $v_{Cr3}(t_7)=0$ and the anti-parallel diode of S_{m2} is conducting. The time interval in this mode is approximately expressed as:

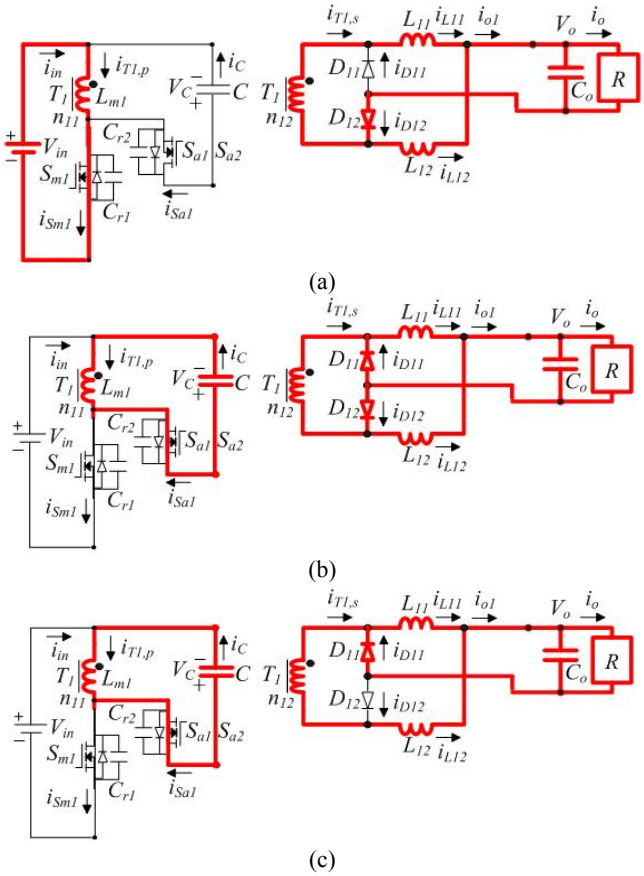
$$\Delta t_{67} = t_7 - t_6 \approx \frac{2C_r V_{in}}{-i_{T2,p}(t_5)} \tag{8}$$

***Mode 8* [$t_7 \le t < t_0+T/2$]:** At time t_7, $v_{Cr3}=0$. Since $i_{T2,p}(t_7)$ is negative, the anti-parallel diode of S_{m2} is conducting. Thus S_{m2} can be turned on at this instant to realize ZVS. During this interval, diodes D_{21} and D_{22} are in the commutation mode. The diode current i_{D21} decreases and i_{D22} increases. The magnetizing voltage v_{Lm2} is zero so that the leakage inductor voltage v_{lk2} is equal to V_{in}. The primary current $i_{T2,p}$ increases linearly with the slope of V_{in}/L_{lk2}. Thus the secondary winding current $i_{T2,s}$ increases from a negative value to a positive value. This mode ends at time $t_0+T/2$, when $i_{D21}=0$ and diode D_{21} turns off. Then the circuit operation of the proposed converter in the first half of switching cycle is completed. The PWM waveforms in the second half of the switching cycle are symmetrical with the PWM waveforms in the first half of the switching cycle.

IV. CIRCUIT ANALYSIS

A. Voltage conversion ratio

In each half of a switching cycle, the transition intervals in modes 2 and 3 in converter 1 and modes 6 and 7 in converter 2 are much shorter. Thus the effect of these modes can be neglected to derive the dc voltage conversion ratio of the



proposed converter. However, the duty cycle losses need to be considered when either the main or the auxiliary switches are on and the rectifier diodes are in the commutation mode. Fig 4 shows the main four operating stages in converter 1 during one switching cycle. Stages 1 and 3 are related to the main switch and auxiliary switch in the on-state when only one diode of current doubler is conducting. In stage 1, switch S_{m1} is on, the transformer primary voltage $v_{T1,p}=V_{in}$ and the secondary winding voltage $v_{T1,s}\approx kV_{in}/n$, where $k=L_m/(L_m+L_{lk})$. The time interval in stage 1 is $(\delta-\delta_{loss,1})T$, where δ is the duty cycle of S_{m1}, $\delta_{loss,1}$ is the duty cycle loss at stage 4 with D_{11} and D_{12} on, and T is the switching period. The output inductor voltages $v_{L11}=kV_{in}/n-V_o$ and $v_{L12}=-V_o$ in stage 1. In stage 2, switch S_{a1} is on and diodes D_{11} and D_{12} are in the commutation mode. Thus the leakage voltage $v_{lk1}=-V_C$ and the secondary winding voltage $v_{T1,s}\approx 0$. The time interval in stage 2 is $\delta_{loss,2}T$. The duty cycle loss $\delta_{loss,2}$ can be expressed as $\delta_{loss,2} \approx L_{lk}I_o/[2nV_CT]$. The output inductor voltages $v_{L11}=v_{L12}=-V_o$ in stage 2. In stage 3, switch S_{a1} and diode D_{11} are conducting. Thus the primary and secondary voltages are expressed as $v_{T1,p}=-V_C$ and $v_{T1,s}\approx -kV_C/n$. The time interval in stage 3 is $(1-\delta-\delta_{loss,2})T$. In stage 4, switch S_{m1} is conducting and diodes D_{11} and D_{12} are in the commutation mode. Thus the leakage voltage $v_{lk1}=V_{in}$ and the secondary winding voltage $v_{T1,s}\approx 0$. The time interval in stage 4 is $\delta_{loss,1}T$. The duty cycle loss $\delta_{loss,1}$ can be expressed as $\delta_{loss,1} \approx L_{lk}I_o/[2nV_{in}T]$. The output inductor voltages $v_{L11}=v_{L12}=-V_o$ in stage 4. Based on the voltage-second balance on the primary windings of T_1, the clamp capacitor voltage V_C can be obtained.

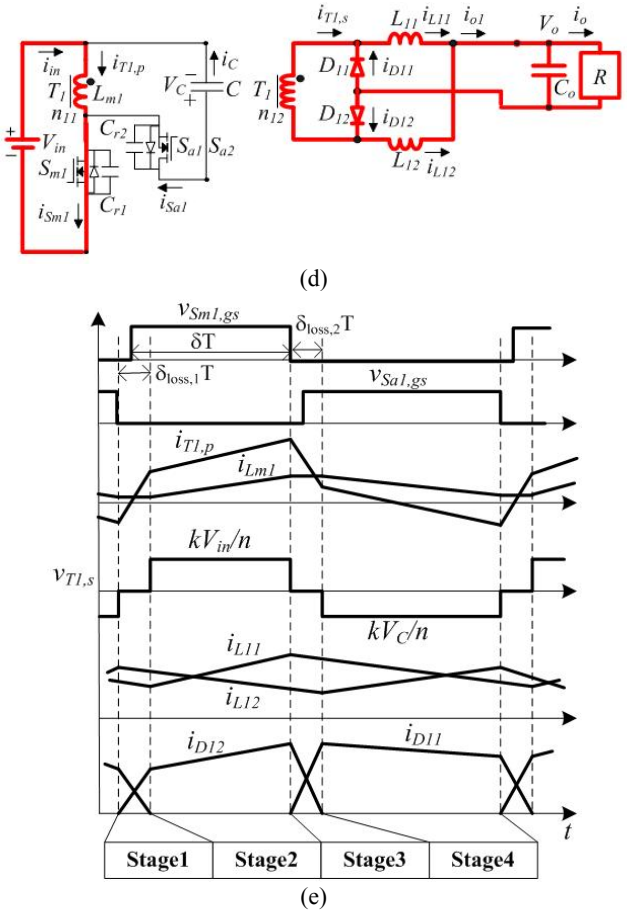


Fig. 4. Simplify main operation stages in converter 1. (a) stage 1. (b) stage 2. (c) stage 3. (d) stage 4. (e) main key waveforms.

$$V_C = \frac{\delta V_{in}}{1-\delta} \tag{9}$$

The average clamp voltage V_C is related to the duty cycle δ and the input voltage V_{in}. Based on the voltage-second balance on the output inductor L_{11}, the output voltage V_o can be obtained.

$$V_o \approx \frac{kV_{in}(\delta-\delta_{loss,1})}{n} = \frac{kV_{in}\delta}{n} - \frac{kL_{lk}I_o}{2n^2T} - V_D \tag{10}$$

where V_D is the voltage drop on rectifier diode D_{11}.

B. Current and voltage stresses of rectifier diodes

It is assumed that the two converters are balanced to supply the load current. Based on the Kirchoff's Current Law, at the secondary winding of the transformers, the average diode currents and inductor currents can be obtained.

$$I_{D11} = I_{D21} \approx \frac{(1-\delta)I_o}{2},\quad I_{D12} = I_{D22} \approx \frac{\delta I_o}{2},$$
$$I_{L11} = I_{L21} \approx \frac{(1-\delta)I_o}{2},\quad I_{L12} = I_{L22} \approx \frac{\delta I_o}{2} \tag{11}$$

The voltage stresses of the rectifier diodes are given as:

$$V_{D11}=V_{D21}\approx\frac{kV_{in}}{n},V_{D12}=V_{D22}\approx\frac{kV_C}{n}=\frac{k\delta V_{in}}{n(1-\delta)} \quad (12)$$

C. Average and ripple currents on magnetizing inductance

Based on Kirchoff's Current Law, the relationship between the average currents at the input side can be given as:

$$I_{in}+I_C=I_{T1,p}+I_{T2,p}=I_{Lm1}+I_{T1,s}/n+I_{Lm2}+I_{T2,s}/n \quad (13)$$

Since the average of the secondary currents $I_{T1,s}$ and $I_{T2,s}$ and the average capacitor current I_C in steady state are all zero, the average magnetizing currents are expressed as:

$$I_{Lm1}=I_{Lm2}=\frac{I_{in}}{2}=\frac{k\delta I_o}{2n}-\frac{kL_{lk}I_o^2}{4n^2V_{in}T}-\frac{V_DI_o}{2V_{in}}\approx\frac{\delta I_o}{2n} \quad (14)$$

where T is the switching period. The ripple components of i_{Lm1} and i_{Lm2} are obtained as:

$$\Delta i_{Lm1}=\Delta i_{Lm2}=\frac{(\delta-\delta_{loss,1})TV_{in}}{L_m+L_{lk}} \quad (15)$$

D. Current and voltage stresses of power switches

Based on the circuit configuration of the proposed converter, the voltage stresses of all of the switches are expressed as:

$$v_{Sm1,stress}=v_{Sa1,stress}=v_{Sm2,stress}=v_{Sa2,stress}=V_{in}+V_C=\frac{V_{in}}{1-\delta} \quad (16)$$

Thus the voltage stresses of all of the switches are related to the input voltage V_{in} and the duty ratio δ. The maximum primary current $i_{T1,p}$ can be approximately expressed as:

$$\begin{aligned}&i_{T1,p,\max}=i_{Sm1,\max}=i_{Lm1}(t_1)+i_{L11}(t_1)/n\\&\approx\frac{\delta I_o}{2n}+\frac{(\delta-\delta_{loss,1})TV_{in}}{2(L_m+L_{lk})}+\frac{(1-\delta)I_o}{2n}+\frac{(kV_{in}/n-V_o)(\delta-\delta_{loss,1})T}{2nL_{11}}\\&=\frac{I_o}{2n}+\frac{(\delta-\delta_{loss,1})TV_{in}}{2(L_m+L_{lk})}+\frac{(kV_{in}/n-V_o)(\delta-\delta_{loss,1})T}{2nL_{11}}\\&\text{or }\frac{I_o}{2n}+\frac{(\delta-\delta_{loss,1})TV_{in}}{2(L_m+L_{lk})}+\frac{V_o(1-\delta+\delta_{loss,1})T}{2nL_{12}}\end{aligned} \quad (17)$$

In the same manner, the maximum primary current of converter 2 can be obtained $i_{T2,p,max}=i_{Sm2,max}=i_{T1,p,max}=i_{Sm1,max}$. The minimum values of $i_{T1,p}$ and $i_{T2,p}$ can be obtained as:

$$\begin{aligned}&i_{T1,p,\min}=i_{T2,p,\min}=-i_{Sa1,\max}=-i_{Sa2,\max}\\&\approx-\frac{(1-\delta-\delta_{loss,2})TV_C}{2(L_m+L_{lk})}-\frac{(kV_C/n-V_o)(1-\delta-\delta_{loss,2})T}{2nL_{12}}\\&\text{or }-\frac{(1-\delta-\delta_{loss,2})TV_C}{2(L_m+L_{lk})}-\frac{V_o(\delta+\delta_{loss,2})T}{2nL_{12}}\end{aligned} \quad (18)$$

E. ZVS condition

Basically ZVS of the auxiliary switches S_{a1} and S_{a2} is naturally achieved by the energy stored in the leakage inductances L_{lk1} and L_{lk2} and in the magnetizing inductances L_{m1} and L_{m2}. The ZVS condition of the main switches S_{m1} and S_{m2} is more difficult to achieved than the ZVS condition of the auxiliary switches S_{a1} and S_{a2}. The ZVS condition of the switches S_{m1} and S_{m2} is determined from (19).

$$L_{lk}\ge 2C_rV_{in}^2/i_{T2,\min}^2\approx\frac{2C_rV_{in}^2}{[\frac{(1-\delta)TV_C}{2L_m}+\frac{V_o\delta T}{2nL_{12}}]^2} \quad (19)$$

where $L_{lk}=L_{lk1}=L_{lk2}$ and $C_r=C_{r1}=C_{r2}=C_{r3}=C_{r4}$.

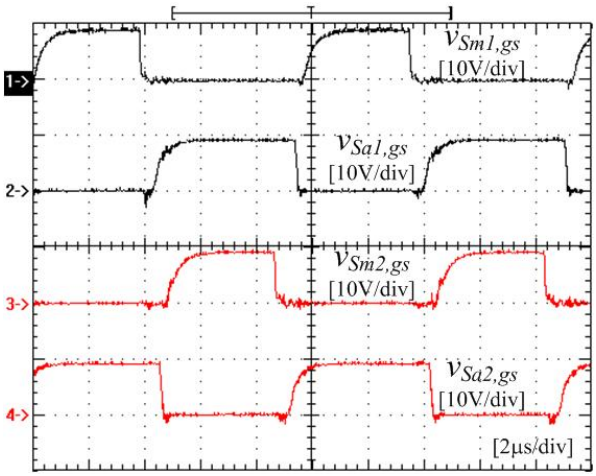


Fig. 5. Measured waveforms of the gate voltages of all switches at full load.

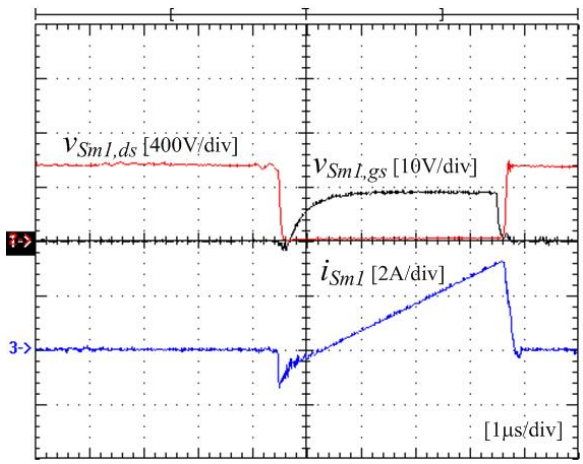


Fig. 6. Measured waveforms of $v_{Sm1,gs}$, $v_{Sm1,ds}$ and i_{Sm1} at full load.

F. Output filter inductances

The current ripples on the output inductors are equal at a duty cycle of δ=0.5. If the current ripple on the output inductor is set to be 20% of the rated output load current, the inductances are calculated as:

$$L_{11}=L_{12}=L_{21}=L_{22}\approx\frac{V_oT/2}{\Delta i_{L11}}=\frac{10V_oT}{i_{o,\max}} \quad (20)$$

G. Resonant inductance and clamp capacitance

To ensure the ZVS operation of switches S_{m1} and S_{m2}, the resonant inductance of L_{lk} is selected from (19). The

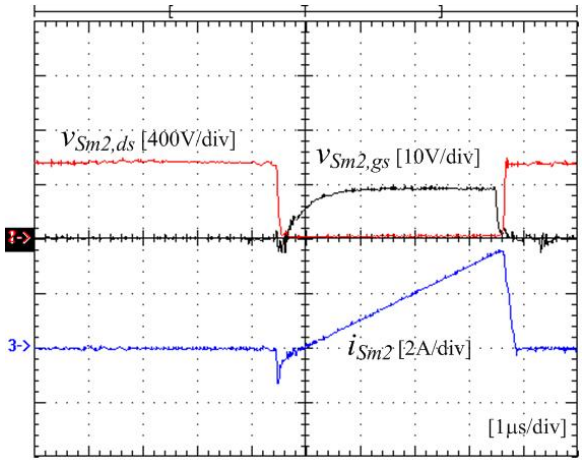


Fig. 7. Measured waveforms of $v_{Sm2,gs}$, $v_{Sm2,ds}$ and i_{Sm2} at full load

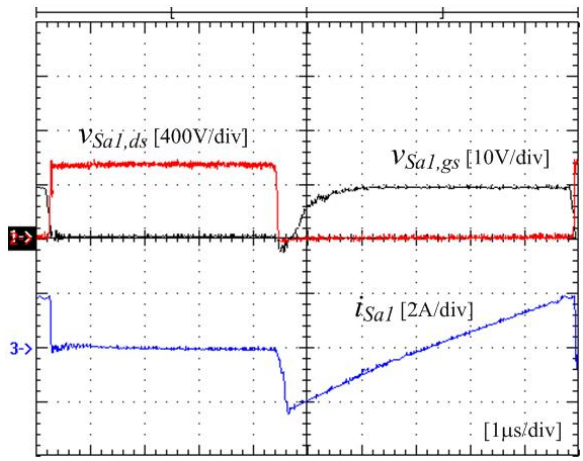


Fig. 8. Measured waveforms of $v_{Sa1,gs}$, $v_{Sa1,ds}$ and i_{Sa1} at full load.

capacitance of C can be expressed as in (21) based on the ripple voltages of the clamp capacitor.

$$C \approx \frac{\delta I_o}{n\Delta v_c f} \tag{21}$$

The other condition of capacitance C can be derived in mode 1. The resonant periods of L_{m2}, L_{lk2} and C must be larger than the turn-off time of S_{m2}. Thus the capacitance of C can be obtained.

$$C >> \frac{(1-\delta)^2 T^2}{4\pi^2 (L_m + L_{lk})} \tag{22}$$

V. Experimental Results

The proposed ZVS converter with current doubler rectifiers was implemented with the following specifications: input voltage V_{in}=380~420V; output voltage V_o=24V; rated output power P_o=408W; switching frequency f=100kHz. The circuit parameters used in this experiment are as follows: L_m=400μH; L_{lk}=16μH; n_p:n_s=50:8; L_{11}=L_{12}=L_{21}=L_{22}=150μH; C_o=3600μF; C=4.4μF; S_{m1}~S_{a2}: FS14SM16A; D_1~D_4: HFA30PA60C. The interleaved PWM

TABLE I

Measured Output Voltage Of The Proposed Converter Under Different Output Loads

P_o (W)	24	96	168	240	312	408
Output voltage (V)	24.13	24.09	24.06	24.01	23.97	23.91

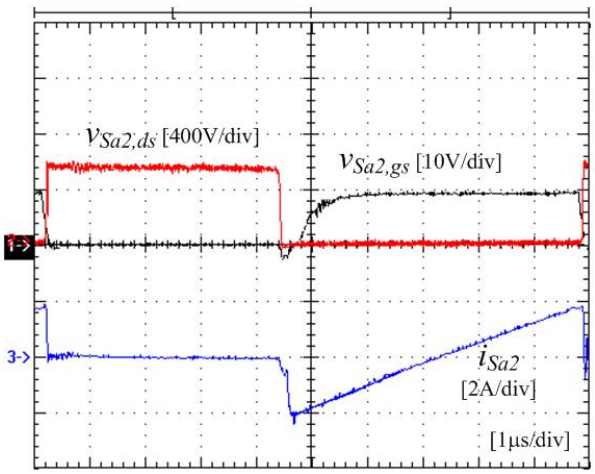


Fig. 9. Measured waveforms of $v_{Sa2,gs}$, $v_{Sa2,ds}$ and i_{Sa2} at full load.

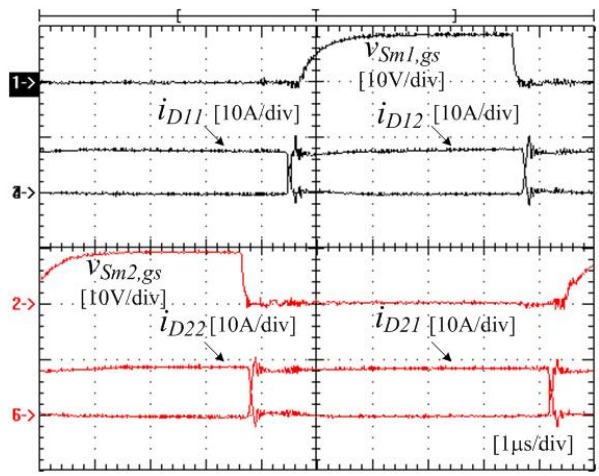


Fig. 10. Measured waveforms of $v_{Sm1,gs}$, i_{D11}, i_{D12}, i_{D21} and i_{D22} at full load.

IC UCC28221 and the isolated gate drives are used to generate the four gate signals of S_{m1}~S_{a2}. Fig. 5 shows the measured waveforms of the gate voltages of switches S_{m1} ~S_{a2} under a full load. The gate voltages of S_{m1} and S_{m2} are phase-shifted one half of a switching cycle. The measured waveforms of $v_{Sm1,gs}$, $v_{Sm1,ds}$ and i_{Sm1} under a full load are shown in Fig. 6. Before switch S_{m1} is turned on, the switch current i_{Sm1} is negative to discharge capacitor C_{r1} until the drain voltage $v_{Sm1,ds}$=0. Then the anti-parallel diode of S_{m1} is conducting. Therefore ZVS turn-on of S_{m1} is achieved. In the same manner, the measured gate voltage, the drain voltage and the switch current of S_{m2}, S_{a1} and S_{a2} under full load are illustrated in Figs 7-9. It is clear that switches S_{m2}, S_{a1} and S_{a2} are all turned on under ZVS. Fig. 10 shows the measured

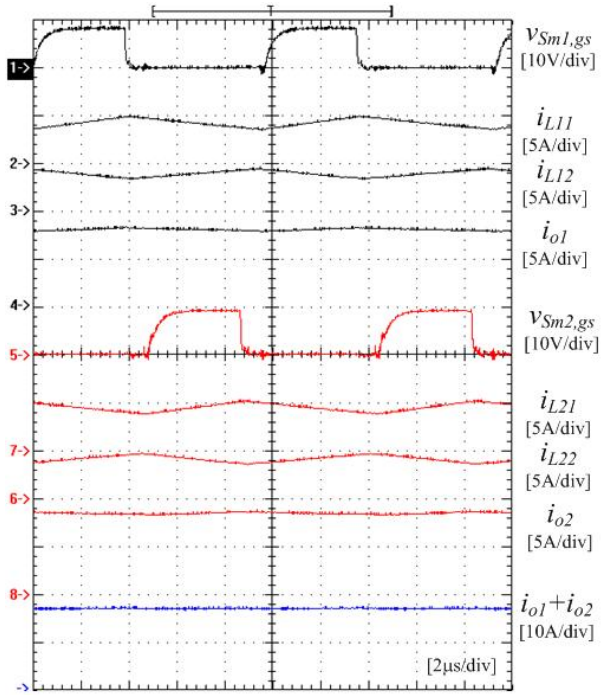


Fig. 11. Measured waveforms of $v_{Sm1,gs}$, i_{L11}, i_{L12}, i_{o1}, $v_{Sm2,gs}$, i_{L21}, i_{L22}, i_{o2} and $i_{o1}+i_{o2}$ at full load.

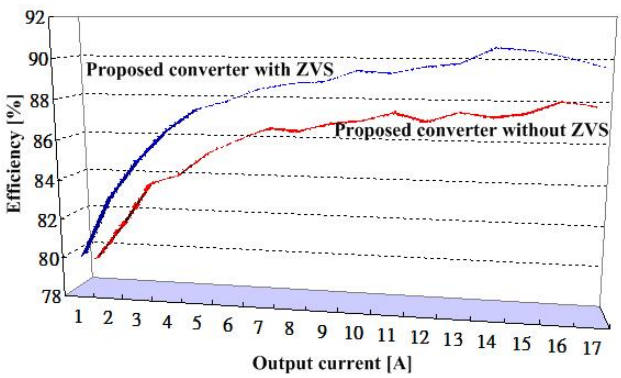


Fig. 12. Conversion efficiency of the proposed converter under different output loads.

waveforms of the gate voltages of S_{m1} and S_{m2} and the diode currents at the secondary side for the full load condition. When S_{m1} is turned on, the diode current i_{D12} equals i_{o1} and the diode current i_{D11}=0 for converter 1. For converter 2, the diode current i_{D22} equals i_{o2} and the diode current i_{D21} equals 0 when S_{m2} is turned on. Fig. 11 gives the measured waveforms of $v_{Sm1,gs}$, i_{L11}, i_{L12}, i_{o1}, $v_{Sm2,gs}$, i_{L21}, i_{L22}, i_{o2} and $i_{o1}+i_{o2}$ under full load. It is clear that the ripple currents on inductors L_{11} and L_{12} are reduced by each other at the current i_{o1} ($=i_{L11}+i_{L12}$). In the same manner, the ripple currents on inductors L_{21} and L_{22} are also reduced by each other at the resultant current i_{o2} ($=i_{L21}+i_{L22}$). Thus the ripple current on the output capacitor C_o is reduced. Basically, the average output inductor currents are not equal (related to the duty cycle). However, the output currents from each current doubler rectifier are almost balanced if the turn ratios of the two isolated transformers and the characteristics of the switches, rectifier diodes and output inductances are identical. Fig. 12 shows the measured efficiency of the proposed converter under different load conditions. From the measured results, the efficiency of the proposed converter is improved due to the ZVS operation. The measured maximum efficiency of the proposed converter is 90.7% at 85% of the rated output power. Table 1 shows the variation of the output voltage under different output loads. It can be seen that the output voltage variation is below 1%.

VI. CONCLUSION

This paper presents an interleaved active-clamping converter with a single clamp capacitor to achieve ZVS turn-on of all of the switches, to reset the transformer flux and to limit the voltage stresses of the power switches. Two converters with the interleaved PWM scheme are adopted to share the load current and to reduce the ripple current at the input and output sides. Thus the root-mean-square current and the power loss on the input and output capacitors are reduced. The current doubler rectifier is adopted at the secondary side to achieve a partial ripple current reduction so that the sizes of the output chokes and capacitor are further reduced. ZVS turn-on of the switches is achieved at the transition interval and the switching losses on the power semiconductors are reduced. Comparing the proposed circuit with the active clamp circuits in references [11]-[12], the PWM waveforms in reference [12] are asymmetrical. The two transformer currents are different and that will affect the transformer magnetizing inductance. Thus the ripple currents on the two transformers are different. The two clamping capacitances are also different with different ripple voltages due to the different clamping currents on the two capacitors. Compared to the circuit in reference [11], the proposed converter can achieve less output ripple current. Therefore, the lower output filter inductances can be used in the proposed circuit to reduce the size and to keep the same total ripple current at the output side. Finally, the experimental results of a laboratory prototype circuit rated at 408W (24V/17A) are provided to verify the effectiveness of the proposed converter.

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Bor-Ren Lin received his B.S. in Electronic Engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1988, and his M.S. and Ph.D. in Electrical Engineering from the University of Missouri, USA, in 1990 and 1993, respectively. From 1991 to 1993, he was a Research Assistant with the Power Electronic Research Center, University of Missouri. Since 1993, he has been with the Department of Electrical Engineering, National Yunlin University of Science and Technology, Douliou, Taiwan, where he is currently a Professor. He has authored and published more than 200 technical journal papers in the area of power electronics. His main research interests include power-factor correction, multilevel converters, active power filters, and soft-switching converters. Dr. Lin is an Associate Editor of the IEEE Transactions on Industrial Electronics and The Institution of Engineering and Technology Proceedings—Power Electronics. He was the recipient of Research Excellence Awards in 2004, 2005, 2007 and 2011 from the College of Engineering, National Yunlin University of Science and Technology. He received best paper awards from the IEEE Conference on Industrial Electronics and Applications 2007 and 2011, from the Taiwan Power Electronics 2007 Conference, and from the IEEE Power Electronics and Drive Systems 2009 Conference.

Huann-Keng Chiang received his M.S. and Ph.D. in Electrical Engineering from the National Cheng Kung University, Taiwan, in 1987 and 1990, respectively. He is a Professor in the Department of Electrical Engineering, National Yunlin University of Science and Technology, Taiwan. His research interests include automatic control, digital control, grey theory, and motor servo control.

Chih-Yuan Cheng is currently working toward his M.S. in Electrical Engineering from the National Yunlin University of Science and Technology, Yunlin, Taiwan. His research interests include the design and analysis of power factor correction techniques, switching mode power supplies, and soft switching converters.