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Analysis, Design and Implementation of an Interleaved Single-Stage AC/DC ZVS Converters

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Abstract

An interleaved single-stage AC/DC converter with a boost converter and an asymmetrical half-bridge topology is presented to achieve power factor correction, zero voltage switching (ZVS) and load voltage regulation. Asymmetric pulse-width modulation (PWM) is adopted to achieve ZVS turn-on for all of the switches and to increase circuit efficiency. Two ZVS half-bridge converters with interleaved PWM are connected in parallel to reduce the ripple current at input and output sides, to control the output voltage at a desired value and to achieve load current sharing. A center-tapped rectifier is adopted at the secondary side of the transformers to achieve full-wave rectification. The boost converter is operated in discontinuous conduction mode (DCM) to automatically draw a sinusoidal line current from an AC source with a high power factor and a low current distortion. Finally, a 240W converter with the proposed topology has been implemented to verify the performance and feasibility of the proposed converter.

Key words: AC-DC Converter, APWM, Power Converter

I. INTRODUCTION

Traditional AC/DC converters with a diode bridge rectifier followed by a bulk capacitor draw a non-sinusoidal current from the AC line which deteriorates the AC line voltage, produces radiated and conducted electromagnetic interference and reduces the input power factor. In order to meet the EN-61000-3-2 class D limit, power factor correction (PFC) has been used as a solution to improve the input power factor and to reduce the amount of harmonic current when the power level of a switching mode power supply (SMPS) is more than 75W. The most popular PFC technology is based on a front-end diode bridge rectifier followed by a boost converter. A passive power filter is the simplest solution to improve the power factor and reduce the harmonic current. However, the drawbacks of passive power filters are that they are bulky and heavy due to the size of the line frequency inductors and capacitors. Two-stage PFC topologies use an input current shaping converter in front of a DC/DC converter to achieve power factor correction and load voltage regulation. Generally two PWM controllers are needed to draw a sinusoidal line current from the utility side and to control the output voltage at a desired value. Different circuit technologies for PFC have been proposed in [1]-[10] to improve the circuit performance with a high power factor and a low harmonic current for medium and high power applications. The main drawbacks of these topologies are that they have too many circuit components and a complex control scheme. For low power applications, a better way to improve the power factor is to combine a boost converter and a DC/DC converter by sharing their active switches to form a single-stage AC/DC converter [11]-[16] with a commercial PWM controller. However, the drawbacks of a conventional single-stage AC/DC converters are high voltage stresses on the power switches, a high DC bus voltage and hard switching on the active switches.

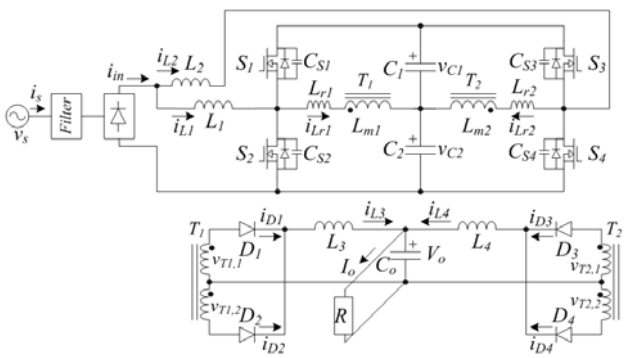

Fig. 1. Circuit configuration of the proposed converter.

An interleaved single-stage AC/DC converter is proposed to achieve power factor correction, low total current harmonics, ripple current reduction at the input and output sides and zero voltage switching (ZVS) for the active switches. Therefore, the performance of the proposed converter meets the EN-61000-3-2 class D limits. There are two circuit modules in the proposed converter. There two

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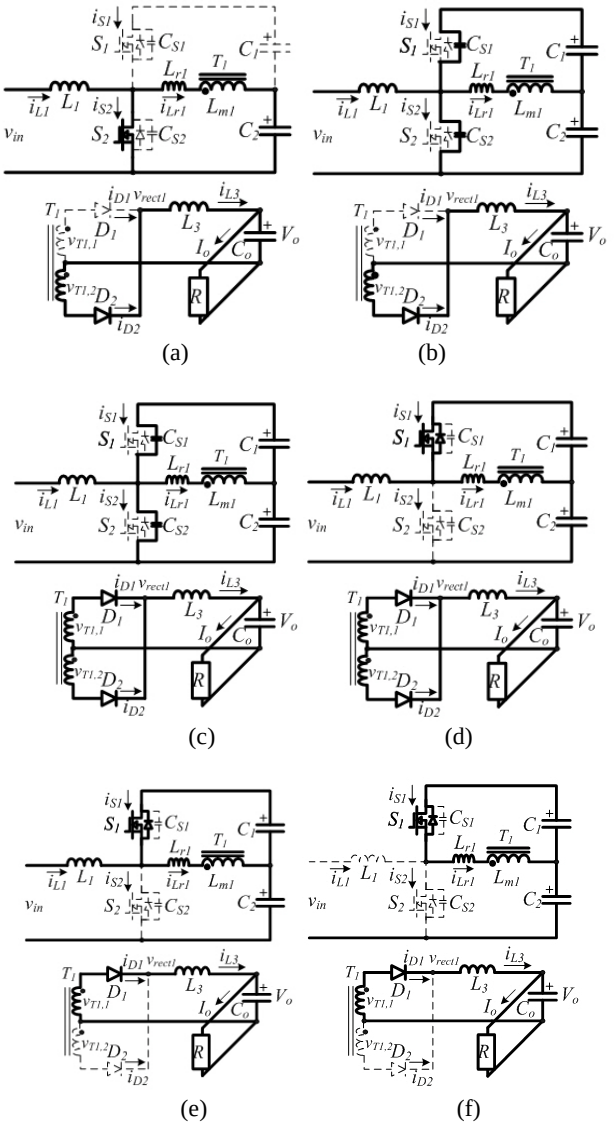


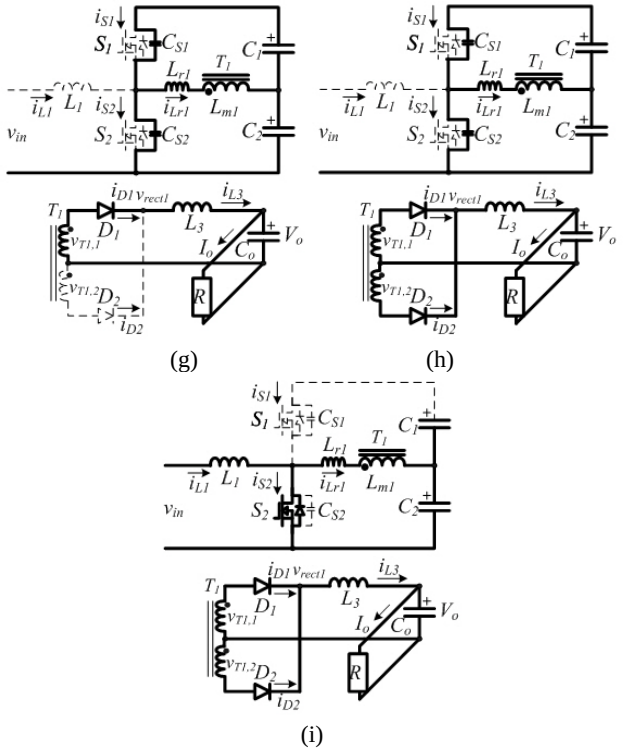


Fig. 2. Equivalent topological modes of the converter 1 operating over one switching cycle. (a) mode 1. (b) mode 2. (c) mode 3. (d) mode 4. (e) mode 5. (f) mode 6. (g) mode 7. (h)

modules are operated with the interleaved pulse-width modulation (PWM) scheme such that the ripple currents at the input and output sides partially cancelled each other out. Thus the conduction losses on the input and output capacitors are reduced. In each circuit module, one boost converter and one half-bridge converter with a center-tapped rectifier have the same active switches to achieve power factor correction and load voltage regulation. The boost converter is operated in the discontinuous conduction mode (DCM) to automatically achieve power factor correction. The half-bridge converter with the asymmetrical PWM scheme is operated in the continuous conduction mode (CCM) to achieve output voltage regulation and ZVS turn-on for all of the switches. The circuit configuration, operation principle and design consideration of the proposed converter are presented and discussed in detailed. Finally, experimental results, obtained from a 240W laboratory prototype, are presented to demonstrate the circuit performance.

II. CIRCUIT CONFIGURATION

The circuit configuration of the proposed AC/DC converter is given in Fig. 1. v_s and V_o are the AC input voltage and the DC output voltage, respectively. L_1 and L_2 are the input boost inductors. C_1 and C_2 are the DC bus capacitances. The DC capacitor voltages v_{C1} and v_{C2} are related to the duty ratio of the switches S_1~S_4. L_{r1} and L_{r2} are the resonant inductances which include the transformer leakage inductance and the external inductance. C_{S1}~C_{S4} are the output capacitances of the active switches S_1~S_4, respectively. Two center-tapped rectifiers are used in the secondary side to realize full-wave rectification. Two boost type AC/DC converters, (L_1, S_1, S_2, C_1 and C_2) and (L_2, S_3, S_4, C_1 and C_2), are operated under the DCM mode and the interleaved PWM scheme to reduce ripple current and to draw a sinusoidal line current from an AC source such that an AC line current with a high power factor and a low harmonic distortion is achieved. The DC bus voltage $v_{DC}=v_{C1}+v_{C2}$ is higher than the peak value of the maximum AC mains voltage. The PWM signals of S_1 and S_2 are complementary to each other with a short dead time. In the same way, the PWM signals of S_3 and S_4 are also complementary. Two asymmetrical half-bridge converters, (S_1, S_2, C_1, C_2, T_1, L_{r1}, D_1, D_2, L_3, C_o) and (S_3, S_4, C_1, C_2, T_2, L_{r2}, D_3, D_4, L_4, C_o), with the interleaved PWM scheme and the continuous conduction mode (CCM) operation is also connected in parallel to reduce the ripple current at the output capacitor C_o and to achieve load current sharing. L_{r1}, C_{S1} and C_{S2} are resonant in the transition interval of S_1 and S_2 to reset the magnetic flux of transformer T_1 such that S_1 and S_2 can be

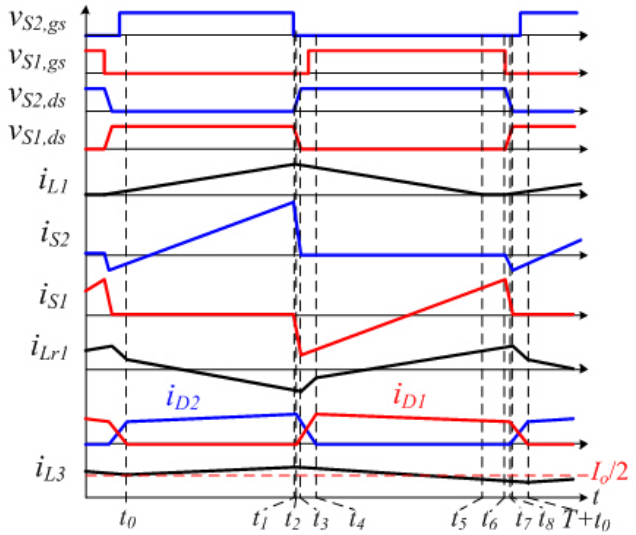


Fig. 3. Key waveforms of converter 1.

turned on under ZVS. In the same manner, S_3 and S_4 are also turned on under ZVS due to the resonant behavior of L_{r2}, C_{S3} and C_{S4} in the transition interval of S_3 and S_4.

III. Operation Principle

Two AC/DC ZVS converters with the interleaved PWM scheme are connected in parallel to share the load current and to reduce the ripple current. In order to simplify the system analysis, only one of the AC/DC converters is discussed in this section. The operation behavior of converter 1 over one switching cycle can be divided into nine operation modes. The equivalent topological modes, given in Fig. 2. Fig. 3, show the key waveforms of the adopted converter 1 over one switching period. In the following analysis, it is assumed that (1) $C_1=C_2>>C_{S1}=C_{S2}$, (2) V_{C1} and V_{C2} are constant over one switching period, (3) all of the power semiconductors are ideal, (4) $L_{r1}<<L_{m1}$, L_1 and L_3, and (5) $i_{L3}=I_o/2$ is a constant current over one switching period. Prior to t_0, S_2 is conducting and diodes D_1 and D_2 are both conducting. The voltage across the resonant inductor L_{r1} equals $-V_{C2}$ such that the inductor current i_{Lr1} and the diode current i_{D1} decrease. The input inductor current increases with the slope of v_{in}/L_1.

***Mode 1* [$t_0 \le t < t_1$, Fig. 2(a)]:** At t_0, the diode current i_{D1} decreases to zero. Thus diode D_1 is off. Since S_2 is conducting and diode D_2 is forward biased, the input inductor voltage $v_{L1}=v_{in}$ and the output inductor voltage $v_{L3}=V_{C2}/n-V_o$, where $n=n_p/n_s$ is the turns ratio of T_1. The inductor currents i_{L1}, i_{Lr1}, i_{Lm1} and i_{L3} and the switch current i_{S2} are given as:

$$i_{L1}(t) = i_{L1}(t_0) + \frac{v_{in}}{L_1}(t-t_0),$$

$$i_{L3}(t) \approx i_{L3}(t_0) + \frac{V_{C2}/n - V_o}{L_3}(t-t_0),$$

$$i_{Lm1}(t) \approx i_{Lm1}(t_0) - \frac{V_{C2}}{L_{m1}}(t-t_0),$$

$$i_{Lr1}(t) = i_{Lm1}(t) - \frac{i_{L3}(t)}{n}, \quad i_{S2}(t) \approx i_{L1}(t) - i_{Lr1}(t) \quad (1)$$

The inductor current i_{L1} increases linearly until switch S_2 is turned off.

***Mode 2* [$t_1 \le t < t_2$, Fig. 2(b)]:** At t_1, switch S_2 is turned off. The positive current i_{L1}-i_{Lr1} charges the capacitor C_{S2} and discharges C_{S1}. Since C_{S1} and C_{S2} are much less than C_1 and C_2, the capacitor voltages v_{CS1} and v_{CS2} can be expressed as:

$$v_{CS1}(t) \approx V_{C1} + V_{C2} - \frac{i_{L1}(t_1) - i_{Lr1}(t_1)}{2C_{S1}}(t-t_1),$$

$$v_{CS2}(t) \approx \frac{i_{L1}(t_1) - i_{Lr1}(t_1)}{2C_{S2}}(t-t_1) \quad (2)$$

The inductor currents i_{L1}, i_{Lr1} and i_{L3} are almost constant in this mode. At t_2, the capacitor voltage v_{CS2} equals V_{C2} such that the primary voltage $v_{Lm1}=v_{T1,1}=v_{T1,2}=0$ and the diodes D_1 and D_2 both conduct. The time interval in this mode can be expressed as:

$$\Delta t_{12} = t_2 - t_1 = \frac{2C_{S2}V_{C2}}{i_{L1}(t_1) - i_{Lr1}(t_1)} \quad (3)$$

***Mode 3* [$t_2 \le t < t_3$, Fig. 2(c)]:** At t_2, the capacitor voltages $v_{CS2}=V_{C2}$ and $v_{CS1}=V_{C1}$. The rectifier diodes D_1 and D_2 are both conducting. The diode currents i_{D1} and i_{D2} are commutated in this mode. The diode current i_{D1} increases and i_{D2} decreases. L_{r1}, C_{S1} and C_{S2} are resonant in this mode. Since the resonant frequency is much higher than the switching frequency, the capacitor voltages v_{CS1} and v_{CS2} are discharged and charged linearly.

$$v_{CS1}(t) \approx V_{C1} - \frac{i_{L1}(t_2) - i_{Lr1}(t_2)}{2C_{S1}}(t-t_2),$$

$$v_{CS2}(t) \approx V_{C2} + \frac{i_{L1}(t_2) - i_{Lr1}(t_2)}{2C_{S2}}(t-t_2) \quad (4)$$

To ensure the ZVS turn-on of switch S_1, the capacitor voltage v_{CS1} should decrease to zero and the capacitor voltage v_{CS2} should be equal to $V_{C1}+V_{C2}$ before the end of this mode. The ZVS condition of S_1 is expressed as:

$$\frac{1}{2}L_1 i_{L1}^2(t_2) + \frac{1}{2}L_{r1} i_{Lr1}^2(t_2) > \frac{1}{2}C_{S1}V_{C1}^2 + \frac{1}{2}C_{S2}[(V_{C1}+V_{C2})^2 - V_{C2}^2] \quad (5)$$

This mode ends at t_3 when the capacitor voltage $v_{CS1}=0$ and the anti-parallel diode of S_1 is conducting. The time duration of this mode is approximately expressed as:

$$\Delta t_{23} = t_3 - t_2 \approx \frac{2C_{S1}V_{C1}}{i_{L1}(t_2) - i_{Lr1}(t_2)} \quad (6)$$

***Mode 4* [$t_3 \le t < t_4$, Fig. 2(d)]:** At t_3, $v_{CS1}=0$ and the anti-parallel diode of switch S_1 is conducting. The diodes D_1 and D_2 are still commutated in this mode. The diode current i_{D1} increases and i_{D2} decreases. The input inductor voltage $v_{L1}=v_{in}-V_{C1}-V_{C2}<0$ such that the inductor current i_{L1} decreases. Before i_{S1} is positive, S_1 must be turned on to achieve ZVS. The inductor current i_{Lr1} increases with the slope of V_{C1}/L_{r1}. This mode ends at t_4 when the diode current i_{D2} is decreased to zero. The inductor current i_{Lr1} increases approximately from $i_{Lm1}(t_3)$-i_{L3}/n (or $i_{Lm1}(t_3)$-$I_o/2n$) to $i_{Lm1}(t_3)$+i_{L3}/n (or $i_{Lm1}(t_3)$+$I_o/2n$). The time interval in this mode is approximately given as:

$$\Delta t_{34} = t_4 - t_3 \approx \frac{I_o L_{Lr1}}{nV_{C1}} \quad (7)$$

In this mode, the voltage across T_1 and L_{r1} is positive. However, the voltage v_{rect1} at the secondary side is zero. Thus the duty loss in this interval can be expressed as:

$$D_{loss,4} = \Delta t_{34} / T \approx \frac{I_o L_{Lr1}}{nV_{C1} T} \quad (8)$$

***Mode 5* [$t_4 \le t < t_5$, Fig. 2(e)]:** At t_4, the diode current i_{D2} decreases to zero. Thus diode D_2 is off. Since S_1 is conducting and diode D_1 is forward biased, the input inductor voltage $v_{L1}=v_{in}-V_{C1}-V_{C2}<0$ such that the inductor current i_{L1} decreases. The output inductor voltage $v_{L3}=V_{C1}/n-V_o$. The inductor currents i_{L1}, i_{Lr1}, i_{Lm1} and i_{L3} and switch current i_{S1} are given as:

$$i_{L1}(t) = i_{L1}(t_4) + \frac{v_{in} - V_{C1} - V_{C2}}{L_1}(t - t_4),$$

$$i_{L3}(t) \approx i_{L3}(t_4) + \frac{V_{C1}/n - V_o}{L_3}(t - t_4),$$

$$i_{Lm1}(t) \approx i_{Lm1}(t_4) + \frac{V_{C1}}{L_{m1}}(t - t_4),$$

$$i_{Lr1}(t) = i_{Lm1}(t) + \frac{i_{L3}(t)}{n}, \quad i_{S1}(t) \approx i_{Lr1}(t) - i_{L1}(t) \quad (9)$$

This mode ends at t_5 when $i_{L1}=0$.

***Mode 6* [$t_5 \le t < t_6$, Fig. 2(f)]:** At t_5, the input inductor current i_{L1} reaches zero. The circuit operation in this mode is the same as the operation in mode 5 except that $i_{L1}=0$. The inductor currents i_{Lm1} and i_{Lr1} both increase in this mode. The switch current $i_{S1}=i_{Lr1}$. This mode ends at t_6 when switch S_1 is off.

***Mode 7* [$t_6 \le t < t_7$, Fig. 2(g)]:** This mode starts at t_6 when switch S_1 is turned off. The positive current i_{Lr1} charges C_{S1} and discharges C_{S2}. In this mode, the capacitor voltages v_{CS1} and v_{CS2} are approximately expressed as:

$$v_{CS1}(t) \approx \frac{i_{Lr1}(t_6)}{2C_{S1}}(t - t_6),$$

$$v_{CS2}(t) \approx V_{C1} + V_{C2} - \frac{i_{Lr1}(t_6)}{2C_{S2}}(t - t_6) \quad (10)$$

The inductor currents i_{Lr1} and i_{L3} are almost constant in this mode. At t_7, the capacitor voltage v_{CS2} equals V_{C2} such that the primary voltage $v_{Lm1}=v_{T1,1}=v_{T1,2}=0$ and the diodes D_1 and D_2 both conduct. The time interval in this mode can be expressed as:

$$\Delta t_{67} = t_7 - t_6 = \frac{2C_{S2}V_{C1}}{i_{Lr1}(t_6)} \quad (11)$$

***Mode 8* [$t_7 \le t < t_8$, Fig. 2(h)]:** At t_7, the capacitor voltages $v_{CS2}=V_{C2}$ and $v_{CS1}=V_{C1}$. The diodes D_1 and D_2 are both conducting. The diode current i_{D1} decreases and i_{D2} increases in this mode. L_{r1}, C_{S1} and C_{S2} are resonant in this mode. The capacitor voltages v_{CS1} and v_{CS2} are approximately given as:

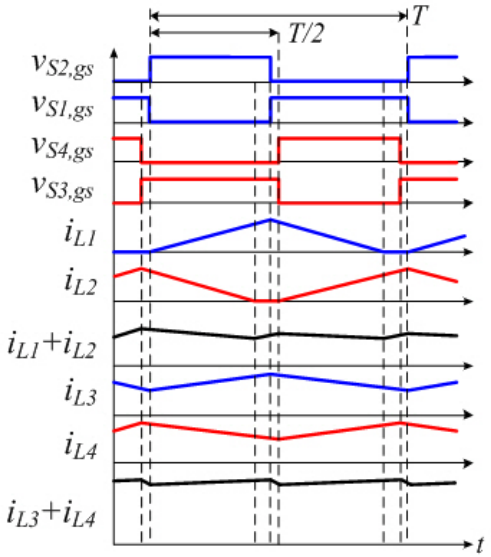


Fig. 4 Key waveforms of the proposed interleaved AC/DC converter.

$$v_{CS1}(t) \approx V_{C1} + \frac{i_{Lr1}(t_7)}{2C_{S1}}(t - t_7),$$

$$v_{CS2}(t) \approx V_{C2} - \frac{i_{Lr1}(t_7)}{2C_{S2}}(t - t_7) \quad (12)$$

To ensure the ZVS turn-on for switch S_2, the capacitor voltage v_{CS2} should decrease to zero and the capacitor voltage v_{CS1} should be equal to $V_{C1}+V_{C2}$ before the end of this mode. The ZVS condition of S_2 is expressed as:

$$\frac{1}{2}L_{r1}i_{Lr1}^2(t_7) > \frac{1}{2}C_{S1}[(V_{C1}+V_{C2})^2 - V_{C1}^2] + \frac{1}{2}C_{S2}V_{C2}^2 \quad (13)$$

This mode ends at t_8 when $v_{CS2}=0$ and the anti-parallel diode of S_2 is conducting. The time duration in this mode is approximately expressed as:

$$\Delta t_{78} = t_8 - t_7 \approx \frac{2C_{S2}V_{C2}}{i_{Lr1}(t_7)} \quad (14)$$

Since the time interval of this mode is much less than the turn-on time of S_2, the input inductor current i_{L1} remains zero even if the input voltage v_{in} is greater than the capacitor voltage v_{CS2}.

***Mode 9* [$t_8 \le t < T+t_0$, Fig. 2(i)]:** This mode begins at t_8, when $v_{CS2}=0$ and the anti-parallel diode of switch S_2 is conducting. The diodes D_1 and D_2 are still commutated in this mode. The diode current i_{D1} decreases and i_{D2} increases. The input inductor voltage $v_{L1}=v_{in}>0$ such that the inductor current i_{L1} increases in this mode. The switch current $i_{S2}=i_{L1}-i_{Lr1}$. Before i_{S2} is positive, S_2 must be turned on to achieve ZVS. The inductor current i_{Lr1} increases approximately from $i_{Lm1}(t_8)+i_{L3}/n$ (or $i_{Lm1}(t_8)+I_o/2n$) to $i_{Lm1}(t_8)-i_{L3}/n$ (or $i_{Lm1}(t_8)-I_o/2n$). The time interval in this mode is approximately given as:

$$\Delta t_{08} = T - t_8 \approx \frac{I_o L_{r1}}{nV_{C2}} \quad (15)$$

The duty loss in this mode can be expressed as:

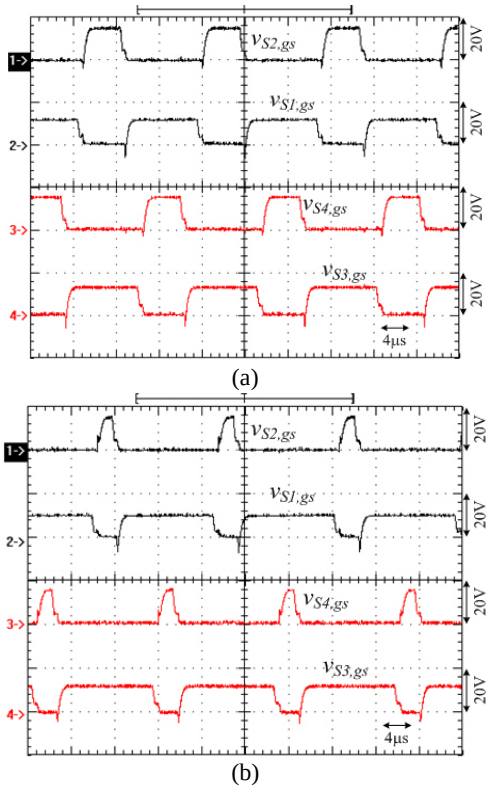


Fig. 5. Measured waveforms of the gate voltages of S_1~S_4 at full load with (a) v_s=110V$_{rms}$ (b) v_s=220V$_{rms}$.

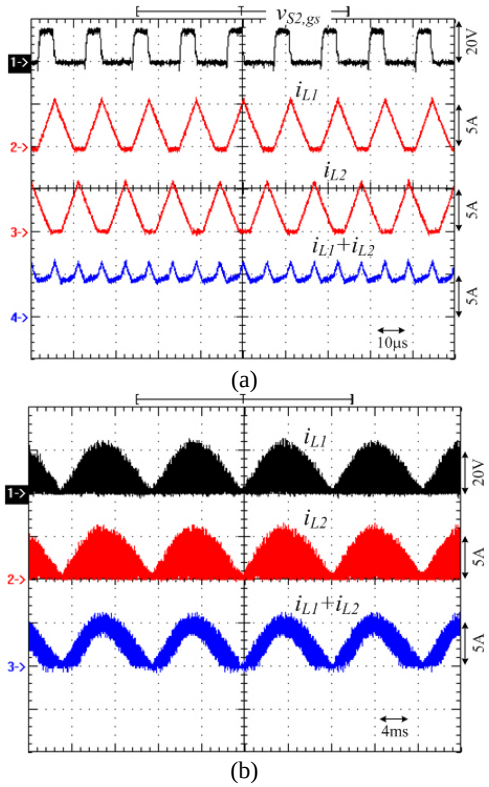


Fig. 6. Measured waveforms of input inductor currents at full load with v_s=110V$_{rms}$ condition. (a) $v_{S2,gs}$, i_{L1}, i_{L2}, i_{L1}+i_{L2} with 10μs time scale. (b) i_{L1}, i_{L2}, i_{L1}+i_{L2} with 4ms time scale.

$$D_{loss,9} \approx \frac{I_o L_{r1}}{nV_{C2}T} \tag{16}$$

This mode ends at T+t_0 when the diode current i_{D1} is decreased to zero. Then the operating modes of one of the proposed converters over one switching period are completed.

In the proposed circuit, two AC/DC converters are connected in parallel to achieve the load current sharing, ripple current reduction, power factor correction and load voltage regulation. Fig. 4 shows the key waveforms of the proposed interleaved AC/DC converter. It is clear that the input and output currents are phase-shifted one-half of a switching period. The ripple currents at the input and output sides are reduced with a double switching frequency.

IV. Design Considerations

Since the boost converters including (L_1, S_1, S_2, C_1 and C_2) and (L_2, S_3 S_4, C_1 and C_2) are designed in the DCM operation, the average inductor currents $i_{L1,av}$ and $i_{L2,av}$ are expressed as:

$$i_{L1,av} = i_{L2,av} = \frac{TV_s D_{S2}^2 |\sin \omega t|}{2L_1(1-\frac{V_s}{V_{C1}+V_{c2}}|\sin \omega t|)} \approx A|\sin \omega t|(1+k|\sin \omega t|+k^2|\sin \omega t|^2) \tag{17}$$

where $A = TV_s D_{S2}^2/(2L_1)$, L_1=L_2, the duty cycles of S_2 and S_4 are identical so that D_{S2}=D_{S4}, k=V_s/(V_{C1}+V_{C2}), T is the switching period, and V_s is the peak value of the line voltage. If the duty cycles D_{S1}=D_{S3} are constant, the average input inductor currents $i_{L1,av}$ and $i_{L2,av}$ are rectified sinusoidal waveforms with second and third order distortions. If the voltage ratio k is decreasing, the current distortion is also decreasing. The input AC line current i_s can be expressed as:

$$i_s \approx 2A\sin \omega t(1+k|\sin \omega t|+k^2|\sin \omega t|^2) = 2A\sin \omega t + \text{distortion} \tag{18}$$

If it is assumed the circuit efficiency is η and the output power is P_o, then the average input power P_{in} can be given as:

$$P_{in} = P_o/\eta \approx \frac{TV_s^2 D_{S1}^2}{L_1 \pi}\int_0^{\pi} \sin^2 \omega t(1+k|\sin \omega t|+k^2|\sin \omega t|^2)d\omega t \tag{19}$$

The maximum constant duty cycle of S_1 and S_3 can be obtained in (20) if the input inductor L_1 and maximum load power are given as:

$$D_{S1,\max} \approx \frac{1}{V_{s,\min}} \times \sqrt{\frac{\pi P_{o,\max} L_1}{\eta T\int_0^{\pi} \sin^2 \omega t(1+k|\sin \omega t|+k^2|\sin \omega t|^2)d\omega t}} \tag{20}$$

Two asymmetrical half-bridge converters are operated in CCM operation to regulate the output voltage, share the load current and achieve ZVS turn-on for all of the active switches.

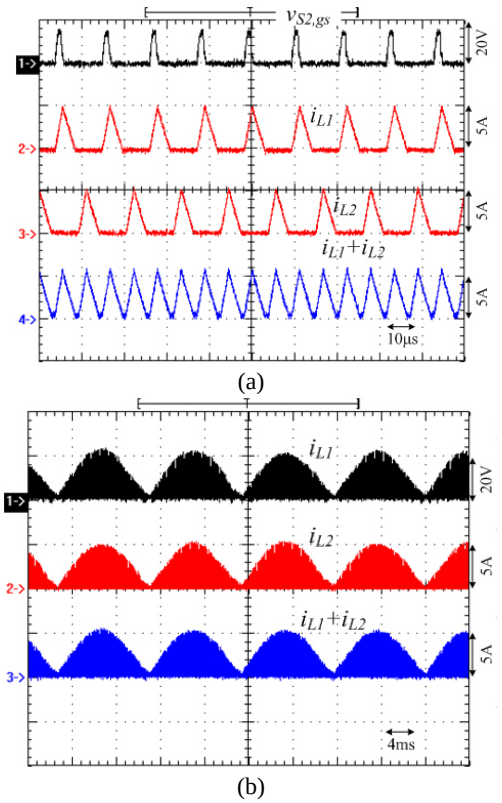


Fig. 7. Measured waveforms of input inductor currents at full load with v_s=220V$_{rms}$ condition. (a) $v_{S2,gs}$, i_{L1}, i_{L2}, i_{L1}+i_{L2} with 10μs time scale. (b) i_{L1}, i_{L2}, i_{L1}+i_{L2} with 4ms time scale.

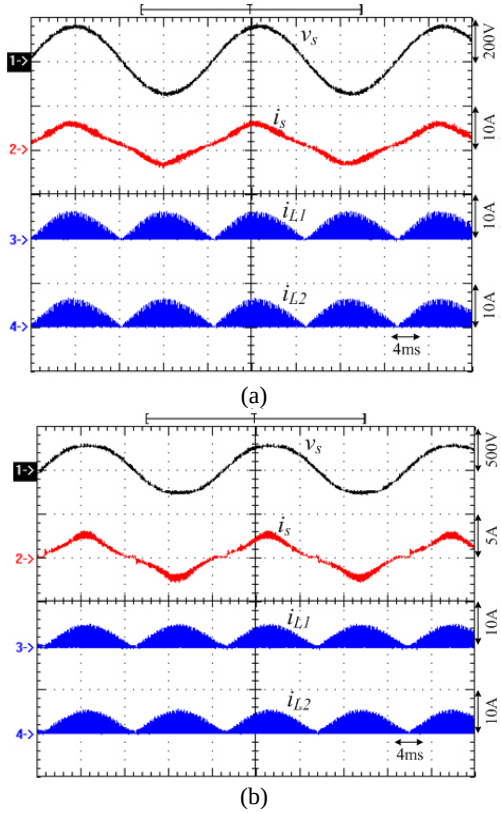


Fig. 8. Measured waveforms of v_S, i_w, i_{L1} and i_{L2} at full load with (a) v_s=110V$_{rms}$ (b) v_s=220V$_{rms}$.

The transition intervals in modes 2-3 and 7-8 between S_1 and S_2 in converter 1 and between S_3 and S_4 in converter 2 are neglected to simplify the system analysis. When S_2 is turned on and S_1 is turned off in modes 1 and 9, the voltage across L_{r1} and L_{m1} equals -V_{C2}. When S_1 is turned on and S_2 is turned off in modes 4-6, the voltage across L_{r1} and L_{m1} equals V_{C1}. Based on the voltage-second balance across L_{r1} and L_{m1}, the following equations can be obtained.

$$\frac{V_{C1}}{V_{C2}} = \frac{D_{S2}}{1-D_{S2}} \tag{21}$$

where D_{S2} is the duty cycle of switch S_2. In converter 1, the output inductor voltage v_{L3} equals V_{C2}/n-V_o in mode 1, -V_o in mode 4, V_{C1}/n-V_o in mode 5, and -V_o in mode 9. Based on the voltage-second balance across the output inductor L_3, the output voltage V_o can be given as:

$$\begin{aligned} V_o &= \frac{V_{C2}}{n}(2D_{S2} - D_{loss,9} - \frac{D_{S2}D_{loss,4}}{1-D_{S2}}) \\ &= \frac{V_{C2}}{n}(2D_{S2} - \frac{I_o L_{Lr1}}{nV_{C2}T} - \frac{D_{S2}}{1-D_{S2}} \cdot \frac{I_o L_{Lr1}}{nV_{C1}T}) \\ &= \frac{2V_{C2}}{n}(D_{S2} - \frac{I_o L_{Lr1}}{nV_{C2}T}) \end{aligned} \tag{22}$$

The voltage stresses of switches S_1~S_4 are approximately equal to V_{C1}+V_{C2}. The voltage stresses of the rectifier diodes D_1~D_4 are given as:

$$v_{D1,stress} = V_{D3,stress} \approx \frac{2V_{C2}}{n}, \quad v_{D2,stress} = V_{D4,stress} \approx \frac{2V_{C1}}{n} \tag{23}$$

The average and *rms* currents of the rectifier diodes D_1~D_4 are expressed as:

$$i_{D1,av} = i_{D3,av} = \frac{(1-D_{S2})I_{o,\max}}{2}, i_{D2,av} = i_{D4,av} = \frac{D_{S2}I_{o,\max}}{2} \tag{24}$$

$$\begin{aligned} i_{D1,rms} &= i_{D3,rms} = \frac{I_{o,\max}\sqrt{1-D_{S2}}}{2}, \\ i_{D2,rms} &= i_{D4,rms} = \frac{I_{o,\max}\sqrt{D_{S2}}}{2} \end{aligned} \tag{25}$$

The ripple current of L_3 can be obtained in mode 1 and expressed in (26).

$$\Delta i_{L3} = \frac{(V_{C2}/n - V_o)(D_{S2} - D_{loss,9})T}{L_3} \tag{26}$$

From (16) and (26), the output inductances L_3 and L_4 can be obtained as:

$$L_3 = \frac{(V_{C2}/n - V_o)(D_{S2}T - \frac{I_o L_{r1}}{nV_{C2}})}{\Delta i_{L3}} \tag{27}$$

To ensure the ZVS turn-on for switches S_1 and S_3 in mode 3, the energy stored in input inductance L_1 (or L_2) and the resonant inductance L_{r1} (or L_{r2}) must be greater than the energy stored in C_{S1} and C_{S2}.

$$\begin{aligned} &\frac{1}{2}L_1 i_{L1}^2(t_2) + \frac{1}{2}L_{r1}i_{Lr1}^2(t_2) \\ &> \frac{1}{2}C_{S1}V_{C1}^2 + \frac{1}{2}C_{S2}[(V_{C1}+V_{C2})^2 - V_{C2}^2] \end{aligned} \tag{28}$$

TABLE I

MEASURED POWER FACTOR, TOTAL HARMONIC DISTORTION AND CIRCUIT EFFICIENCY AT DIFFERENT LOADS AND LINE VOLTAGES

v_s=110V_{rms}	Load Power	60W	120W	180W	240W
	Power Factor	0.94	0.958	0.973	0.986
	THD	36.3%	30%	23.7%	16.9%
	Efficiency	83.1%	85.5%	86.7%	88.3%
v_s=220V_{rms}	Power Factor	0.932	0.952	0.967	0.975
	THD	38.8%	32.1%	26.3%	22.7%
	Efficiency	84.3%	85.9%	88.1%	90.1%

In the same manner, the ZVS condition of S_2 and S_4 in mode 8 can be obtained as:

$$\frac{1}{2}L_{r1}i_{Lr1}^2(t_7) > \frac{1}{2}C_{S1}[(V_{C1}+V_{C2})^2 - V_{C1}^2] + \frac{1}{2}C_{S2}V_{C2}^2 \quad (29)$$

From (28) and (29), it can be observed that the ZVS condition of S_1 and S_3 is easier to meet than the ZVS condition of S_2 and S_4. This is because the boost is operated in DCM and the half-bridge converter is operated in CCM. From (21) and (22), the voltage conversion ratio between the output voltage and the input voltage can be expressed as:

$$\begin{aligned}\frac{V_o}{V_s} &= \frac{V_o}{V_{C2}} \times \frac{V_{C2}}{V_{C1}+V_{C2}} \times \frac{V_{C1}+V_{C2}}{V_s} \\ &> \frac{2}{n}(D_{S2} - \frac{I_o L_{Lr1}}{nV_{C2}T}) \times (1-D_{S2}) \times \frac{1}{1-D_{S2}} \\ &\approx \frac{2}{n}(D_{S2} - \frac{I_o L_{Lr1}}{nV_{C2}T})\end{aligned} \quad (30)$$

V. EXPERIMENTAL RESULTS

The performance and effectiveness of the proposed converter were verified through experimental results. The circuit parameters of the adopted prototype circuit are v_s=90V_{rms}~240V_{rms}, V_o = 24V, P_o=240W, f=80kHz, L_{m1}=L_{m2}=130μH, C_1=C_2=2.2μF, L_1=L_2=100μH, L_3=L_4=180μH, n_p/n_s=24/5, S_1~S_4: IRFP460 and D_1~D_4: BYV42E. A type 2 voltage controller based on a TL431 and an optocoupler PC817 is used to regulate the duty cycle of the power switches. A voltage mode PWM IC TL494 is used to generate two interleaved PWM signals. A gate drive IC L6384 is used to generate the four gate signals of S_1~S_4 with a proper dead time. Fig. 5 gives the measured results of the gate voltages of S_1~S_4 under a full load and low and high line voltage. It is clear that the PWM signals of S_1 and S_2 are phase-shifted with one-half of a switching period with respective to the PWM signals of S_3 and S_4. Fig. 6(a) gives the measured gate voltage $v_{S2,gs}$, input inductor currents i_{L1} and i_{L2} and the resultant input current i_{L1}+i_{L2} under a full load and low line voltage. The inductor currents i_{L1} and i_{L2} are phase-shifted and the resultant input current i_{L1}+i_{L2} has less ripple current than i_{L1} and i_{L2}. The measured waveforms of the input inductor currents i_{L1} and i_{L2} and the resultant input current i_{L1}+i_{L2} under a full load and low line voltage with a 4ms time scale, are shown in Fig. 6(b). The resultant input current i_{L1}+i_{L2} is a continuous conduction mode with less ripple current. In the same manner, Fig. 7 shows the

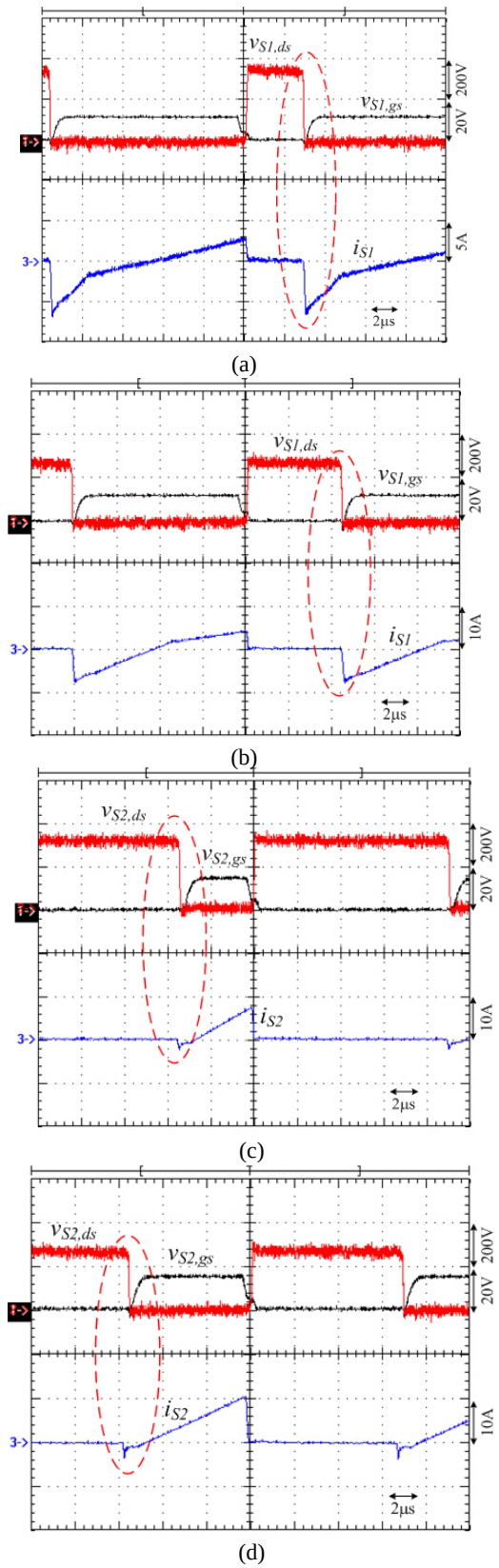
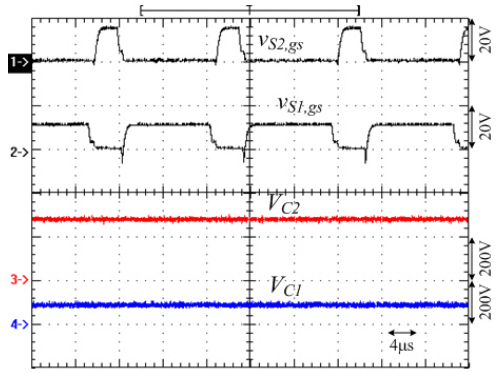
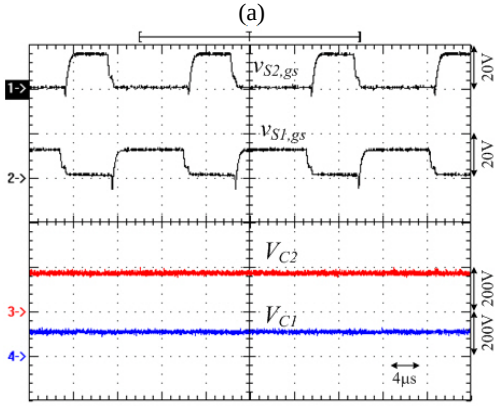


Fig. 9 Measured waveforms of gate voltage, drain voltage and drain current at v_s=110V_{rms} condition (a) $v_{S1,gs}$, $v_{S1,ds}$ and i_{S1} at 30% load (b) $v_{S1,gs}$, $v_{S1,ds}$ and i_{S1} at 100% load (c) $v_{S2,gs}$, $v_{S2,ds}$ and i_{S2} at 30% load (d) $v_{S2,gs}$, $v_{S2,ds}$ and i_{S2} at 100% load.



(a)



(b)

Fig. 10. Measured waveforms of $v_{S1,gs}$, $v_{S2,gs}$, V_{C1} and V_{C2} at v_s=110V$_{rms}$ condition (a) 30% load (b) 100% load.

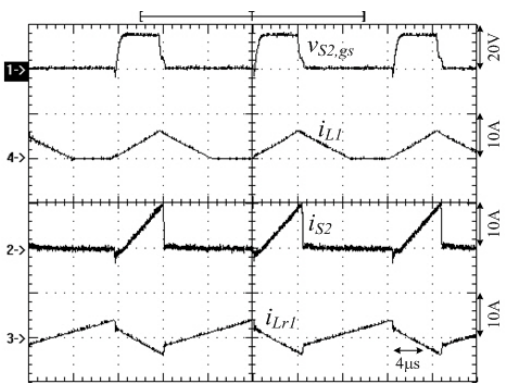


Fig. 11. Measured waveforms of $v_{S2,gs}$, i_{L1}, i_{S2} and i_{Lr1} at full load and v_s=110V$_{rms}$ condition.

measured results of $v_{S2,gs}$, i_{L1}, i_{L2} and i_{L1}+i_{L2} under a full load and with v_s=220V$_{rms}$. Fig. 8 illustrates the measured waveforms of the line voltage, line current and input inductor currents under a full load and low and high line voltage. The line current is in phase with a line voltage with a high power factor and a low harmonic current. The measured power factor, total harmonic distortion and circuit efficiency under different load and line voltages are shown in Table 1. Fig. 9 shows the measured waveforms of the gate voltage, drain voltage and drain current of switches S_1 and S_2 at 30% load and 100% load with v_s=110V$_{rms}$. The drain voltages $v_{S1,ds}$ and $v_{S2,ds}$ have been decreased to zero before switches S_1 and S_2 are turned on. Therefore, the ZVS turn-on of S_1 and S_2 are realized. In the same manner, switches S_3 and S_4 are also turned on under ZVS. Fig. 10 shows the measured waveforms

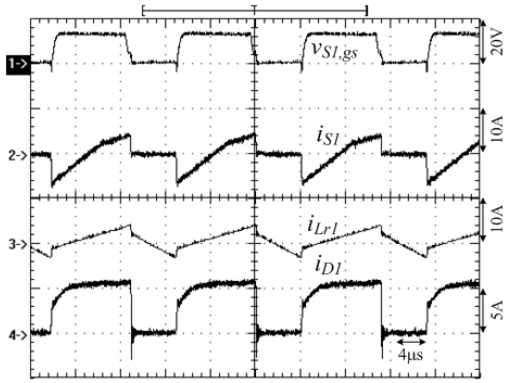


Fig. 12. Measured results of $v_{S1,gs}$, i_{S1}, i_{Lr1} and i_{D1} at full load and v_s=110V$_{rms}$ condition.

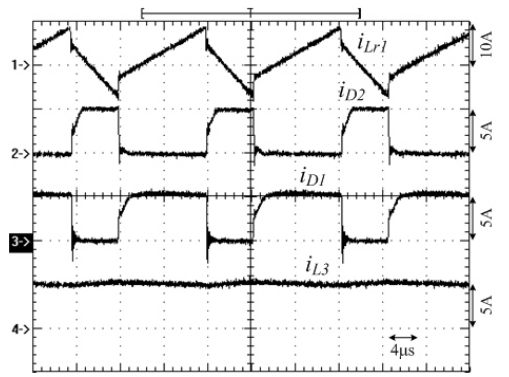


Fig. 13. Measured waveforms of i_{Lr1}, i_{D1}, i_{D2} and i_{L3} at full load and v_s=110V$_{rms}$ condition.

of the gate voltages $v_{S1,gs}$ and $v_{S2,gs}$ and the DC bus voltages V_{C1} and V_{C2} under a light load (30%) and a full load (100%) with v_s=110V$_{rms}$. The capacitor voltages V_{C1} and V_{C2} are related to the duty cycle of switch S_2. Fig. 11 gives the measured waveforms of the gate voltage $v_{S2,gs}$, input inductor current i_{L1}, switch current i_{S2} and inductor current i_{Lr1} under a full load with v_s=110V$_{rms}$. When switch S_2 is in the on state, i_{S2}=i_{L1}-i_{Lr1}. Fig. 12 shows the measured results of the gate voltage $v_{S1,gs}$, switch current i_{S1}, inductor current i_{Lr1} and diode current i_{D1} under a full load with v_s=110V$_{rms}$. When switch S_1 is on, the primary voltage of T_1 is positive and the rectifier diode D_1 is forward biased. The switch current i_{S1}=i_{Lr1}-i_{L1}. Fig. 13 shows the measured waveforms of the inductor current i_{Lr1}, the rectifier diode currents i_{D1} and i_{D2} and the output inductor current i_{L3} under a full load with v_s=110V$_{rms}$. When S_1 is turned on, the primary current i_{Lr1} increases and the diode D_1 is forward biased. If switch S_2 is on, the primary current i_{Lr1} decreases and the diode D_2 is forward biased. Fig. 14 gives the measured waveforms of the output inductor currents i_{L3} and i_{L4} and the resultant output current i_{L3}+i_{L4} at 30% and 100% loads with v_s=110V$_{rms}$. The ripple currents on the output inductors L_3 and L_4 are partially cancelled by each other. Therefore, the ripple current of i_{L3}+i_{L4} is reduced.

VI. CONCLUSION

A parallel AC/DC converter is presented in this paper to achieve the advantages of ZVS turn-on of all of the switches,

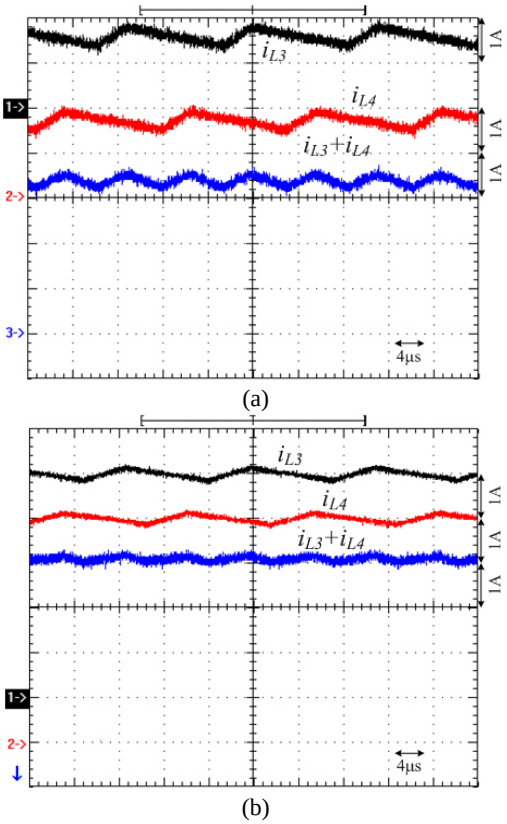


Fig. 14. Measured waveforms of i_{L3}, i_{L4} and $i_{L3}+i_{L4}$ at v_s=110V$_{rms}$ condition (a) 30% load (b) 100% load.

low switching losses, a high power factor, a low total harmonic distortion of the line current, load current sharing, and ripple current reduction at the input and output sides. The input boost converter is operated under DCM operation to draw a sinusoidal line current from an AC source. Asymmetrical half-bridge converters with the interleaved PWM scheme are adopted to achieve ZVS turn-on for all of the active switches and to reduce the output ripple current. Since active switches can be simultaneously operated in the boost and asymmetrical half-bridge converters, the active switches are reduced when compared to a conventional two-stage AC/DC converter. The system analysis and design considerations of the proposed converter are analyzed and discussed in detail. Finally, experiments conducted on a 240W prototype circuit are provided to verify the performance and effectiveness of the proposed converter.

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