DSP-Based Simplified Space-Vector PWM for a Three-Level VSI with Experimental Validation

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Abstract

Multilevel inverters have gained attention in high-power applications due to their numerous advantages in comparison with conventional two-level inverters. In this paper a simplified Space-Vector Modulation (SVM) algorithm for a three-level Neutral-Point Clamped (NPC) inverter is implemented on a Freescale® DSP56F8037. The algorithm is based on a simplification of the space-vector diagram for a three-level inverter so that it can be used with a two-level inverter. Once the simplification has been achieved, calculation of the dwell times and the switching sequences are carried out in the same way as for the two-level SVM method. Details of the hardware design are included. Experimental results are analyzed to validate the performance of the simplified algorithm.

Key words: Inverter hardware, Space-vector PWM, Three-level inverter

I. INTRODUCTION

Multilevel inverter topologies have gained attention in high power applications due to their numerous advantages in comparison with conventional two-level inverters such as a low output voltage harmonic content, low stress in the load due to a significant reduction in the dv/dt, low switching losses, and high voltage and power capabilities [1]-[3].

The three-level Neutral-Point Clamped (NPC) inverter also known as three-level diode clamped inverter is the most popular multilevel inverter topology due to its higher cost-benefits ratio [4]-[6].

In recent decades a lot of research on multilevel inverters has been conducted with Pulse Width Modulation (PWM) techniques used to control the power semiconductors. This research is mainly focused on extending traditional modulation methods to multilevel cases and looking for less complicated control algorithms despite having more power electronic devices to control [2], [3] and [5].

In this paper a Simplified Space-Vector Modulation algorithm for three-level Neutral-Point Clamped inverters is proposed and implemented on a Freescale® DSP56F8037.

TABLE I
SWITCHING STATES AND LINE-TO-MIDPOINT VOLTAGES (X=A,B,C)

Switching States	Switching device states				Line-to-midpoint voltage v_{XZ}
	S_{X1}	S_{X2}	S_{X3}	S_{X4}	
P	ON	ON	OFF	OFF	E
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-E

The aim of this algorithm is to reduce the computing time and complexity of the process to calculate the dwell time for the space vector. The algorithm assumes that the space-vector diagram of a three-level inverter is comprised of six small hexagons and that all of those hexagons represent the space-vector diagram of a two-level inverter [7]. Details of the hardware design are also included.

II. THREE-LEVEL NEUTRAL-POINT CLAMPED INVERTERS

The algorithm assumes that the space-vector diagram of a three-level inverter is comprised of six small hexagons and that of these hexagons represents the space-vector diagram of a two-level inverter [7]. This can be seen in Fig. 2.

The steps to simplify the space-vector diagram of a three-level inverter into a two-level inverter are as follows:
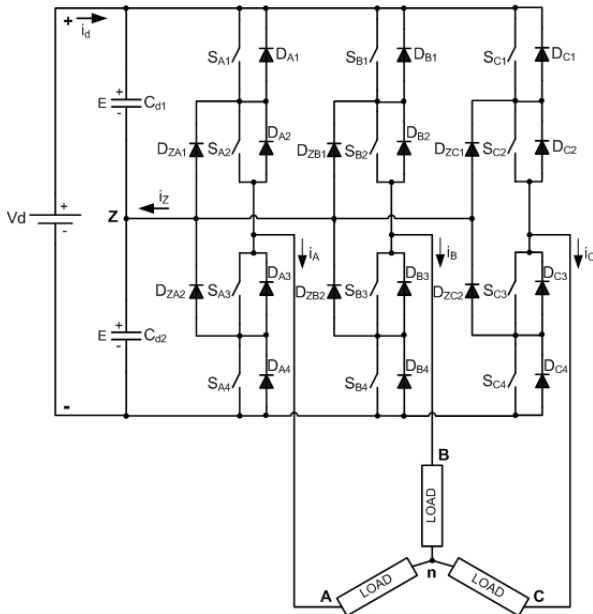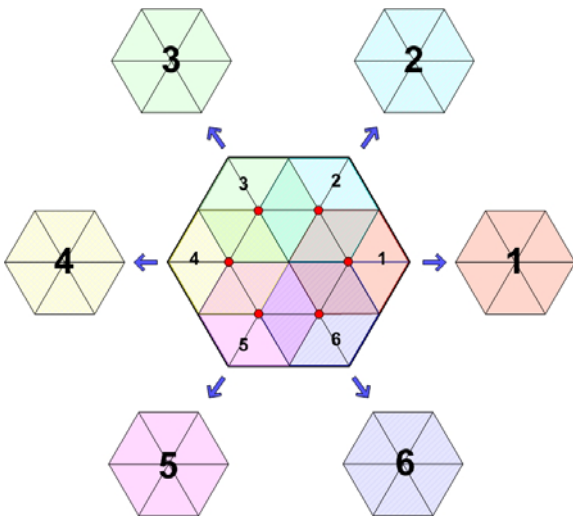
Fig. 1.   Three-level NPC inverter.

Fig. 2.   Three-level space vector diagram.

III. SIMPLIFIED SPACE-VECTOR PWM METHOD

The algorithm assumes that the space-vector diagram of a three-level inverter is comprised by six small hexagons and each one of those hexagons represents the space-vector diagram of a two-level inverter [7]. It can be seen in Fig. 2.

The steps to simplify the space-vector diagram of a three-level inverter into a two-level inverter are as follows:

     1. Identify one of the six two-level hexagons where the vector $\vec{V}_{ref}^{3}$ is located.

     2. Calculate the two-level space vector ($\vec{V}_{ref}^{2}$) from the value of the three-level space vector ($\vec{V}_{ref}^{3}$).
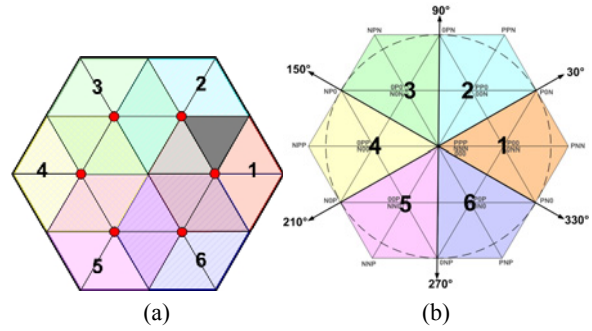

Fig. 3.   Selection of hexagons.

where:

$\vec{V}_{ref}^{3}$: The original reference vector, which is located in a three-level space diagram.

$\vec{V}_{ref}^{2}$: The corrected reference vector, which is located in a two-level space diagram.

Once the space vector simplification has been carried out, the dwell times and the switching sequences are calculated in the same way as the two-level SVM method.

A. Selection of the hexagon

The selection of the two-level hexagon depends on the position of the reference vector $\vec{V}_{ref}^{3}$. However, there are regions that are not well defined because they belong to two hexagons. For example, if the reference-vector $\vec{V}_{ref}^{3}$ is in the shaded, area as it is in Fig. 3(a), any of the two two-level hexagons (hexagons 1 or 2) can be selected.

A solution to avoid hexagon overlapping is illustrated in Fig. 3(b), where the area of each hexagon is redefined, and the three-level space vector is well delimited. In this paper the hexagon identification-algorithm reported in [7] is modified with the aim of further reducing the complexity and the execution time of the simplified SVM algorithm.

The two-level hexagon identification is feasible if the angular displacement of the three-level space vector ($\vec{V}_{ref}^{3}$) is known. It is worth mentioning that it is not necessary to know the value of the angle of the vector $\vec{V}_{ref}^{3}$ at all times. However it is precise to identify the boundary angles where the vector changes from one hexagon to the adjacent one (30^{0}, 90^{0}, 150^{0}, 210^{0}, 270^{0} and 330^{0}).

The identification sequence proposed here is developed in the three-phase reference frame. Fig. 4 shows the three-phase components calculated from the [α, β] components.

By analyzing Fig. 4 it can be seen that the instant where one of the three-phase signals [v_a, v_b or v_c] crosses the zero corresponds to the angle where a change of the hexagon is
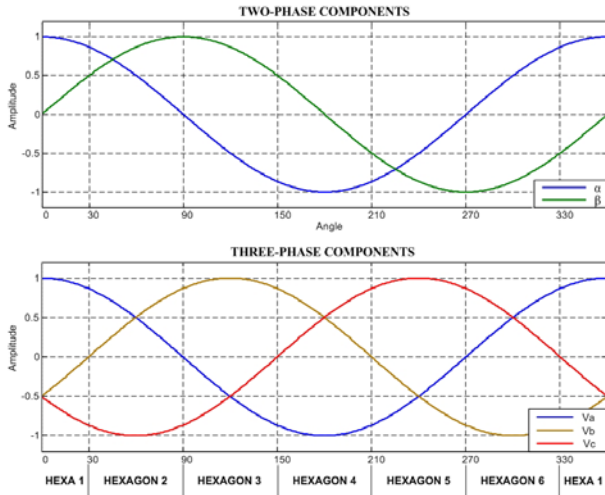
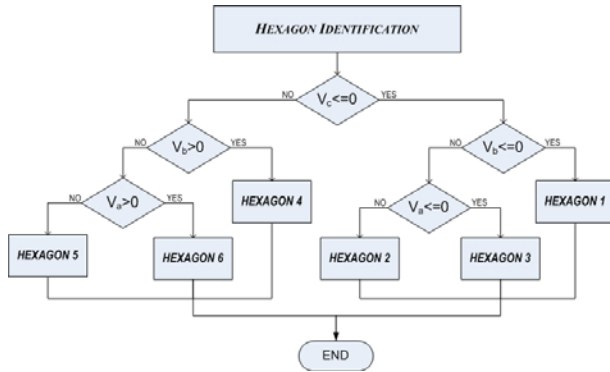Fig. 4.   Two-phase to three-phase component transformation.

Fig. 5.   Hexagon-identification algorithm.

taking place. For example, the instant where $\vec{V}_{ref}^{3}$ has an angle of 30^{0} in the two-phase reference frame corresponds to the instant when v_b crosses the zero from negative to positive values in the three-phase reference frame.

When the angle reaches a value of 90^{0} in the two-phase reference frame (see Fig. 3(b)), it corresponds to the instant when v_a cross the zero from positive to negative values in the three-phase reference frame. This relationship between the three-phase and two-phase reference frames makes it possible to develop an hexagon identification algorithm through a comparison of the signals [v_a, v_b and v_c]. Fig. 5 illustrates the algorithm proposed to identify the hexagons.

B. Correction of the reference vector

Once the two-level hexagon has been identified the origin of the reference vector is moved to the center of the selected hexagon (see Fig. 6). This is done by subtracting the central vector of the selected hexagon from the reference vector $\vec{V}_{ref}^{3}$.

Now the new reference vector $\vec{V}_{ref}^{2}$ is located in a two-level space vector diagram. In the same way as the identification

TABLE II
THREE-PHASE COMPONENTS OF VECTORS POINTING TO THE CENTER OF
EACH HEXAGON

Hex	Auxiliaries		Subtracting Values			
	a	b	Polar	Va	Vb	Vc
1	2	-1	$\frac{1}{\sqrt{3}}\angle0°$	$\frac{1}{\sqrt{3}}$	$-\frac{1}{\sqrt{12}}$	$-\frac{1}{\sqrt{12}}$
2	1	1	$\frac{1}{\sqrt{3}}\angle60°$	$\frac{1}{\sqrt{12}}$	$\frac{1}{\sqrt{12}}$	$-\frac{1}{\sqrt{3}}$
3	-1	2	$\frac{1}{\sqrt{3}}\angle120°$	$-\frac{1}{\sqrt{12}}$	$\frac{1}{\sqrt{3}}$	$-\frac{1}{\sqrt{12}}$
4	-2	1	$\frac{1}{\sqrt{3}}\angle180°$	$-\frac{1}{\sqrt{3}}$	$\frac{1}{\sqrt{12}}$	$\frac{1}{\sqrt{12}}$
5	-1	-1	$\frac{1}{\sqrt{3}}\angle240°$	$-\frac{1}{\sqrt{12}}$	$-\frac{1}{\sqrt{12}}$	$\frac{1}{\sqrt{3}}$
6	1	-2	$\frac{1}{\sqrt{3}}\angle300°$	$\frac{1}{\sqrt{12}}$	$-\frac{1}{\sqrt{3}}$	$\frac{1}{\sqrt{12}}$

algorithm, the correction of the reference vector is done in the three-phase reference frame. This means that the three-phase components of each of the six vectors pointing to the center of each hexagon must be known (see Table II).

To guarantee that the linear PWM region corresponds to the range $0 \leq m \leq 1$, where m is the modulation ratio, the amplitude of the reference voltage-vector must be normalized in the three-level vector space as follows:

$$\text{Normalized vector amplitude} = \sqrt{3} * \left|\vec{V}_{ref}^{3}\right| \qquad (1)$$

With the aim of simplifying the correction algorithm the two auxiliary variables "a and b" [7] are defined. These variables take different values in the function of the two-level hexagon where the reference vector will be displaced to (see Table II). Hence, the three-phase components of the vectors that are pointing to the centers of the six hexagons can be expressed in the function of the auxiliary variables.

$$v_{a\_subtraction} = a * V_d / \sqrt{12}$$

$$v_{b\_subtraction} = b * V_d / \sqrt{12} \qquad (2)$$

$$v_{c\_subtraction} = -v_{a\_subtraction} - v_{b\_subtraction}$$

The three-phase components of the corrected vector, which is now located in the two-level space vector $\vec{V}_{ref}^{2}$, can be obtained by the following equations:

$$v_{a\_corrected} = v_a - v_{a\_subtraction}$$

$$v_{b\_corrected} = v_b - v_{b\_subtraction} \qquad (3)$$

Fig. 6.   Displacement of original reference vector.

Fig. 7.   Two-level space vector diagram.

Fig. 8.   Center-aligned PWM pattern corresponding to a two-level inverter.

$$v_{c\_corrected} = v_c - v_{c\_subtraction}$$

C. Dwell-time calculation.

A two-level inverter is comprised of six switches and it is well known that the top and bottom switches work in a complementary mode. Therefore, when the top switch of one

Fig. 9.   Areas in the three-level hexagon.

leg is ON and the bottom switch is OFF, the corresponding switching state of the two-level inverter is 1 or 0. Since there are two switching states for each phase, the two-level space vector diagram has only 8 vectors and six sectors (see Fig. 7).

The function svmStd (Standard Space Vector Modulation), developed by Freescale®, calculates the appropriate dwell times needed to generate any reference voltage-vector   using a two level Space Vector Modulation technique. Once the function svmStd is applied, it calculates the dwell times t_{phase_A}, t_{phase_B} and t_{phase_C} generating the center-aligned PWM pattern shown in Fig. 8 [10].

It is worth pointing out that the DSP56F8037 does not yet have an embedded subroutine for the control of three-level inverters based on SVM [9], [10]. To face this problem an algorithm to generate the duty cycles of the control signals for three-level inverters by using a two-level SVM embedded subroutine (svmStd) has been developed.

D. Control signals for the switching devices

To calculate the duty cycles of the control signals, the switching sequence needed in the space-vector diagram of a three-level inverter is determined first, and then it is related to the sequence obtained when the space vector is assumed to be a two-level space-vector. With the aim of making the analysis of the switching sequences easier, the three-level space vector diagram is redefined by enumerating all of the space-vector areas as illustrated in Fig. 9.

For example, if the reference vector is in area 1 of the three-level space-vector diagram, the required center-aligned PWM switching sequence is: (POO)-(PON)-(PNN)-(ONN)-(ONN)-(PNN)-(PON)-(POO). On the other hand if the two-level space-vector diagram is considered, the reference vector is in sector I of hexagon 1,
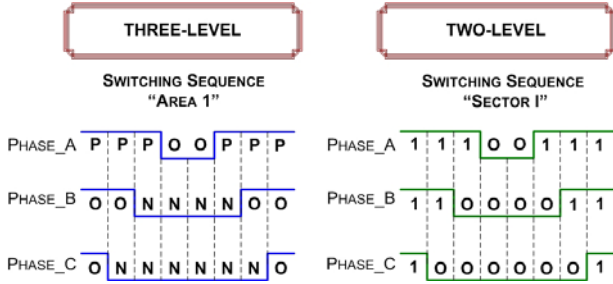
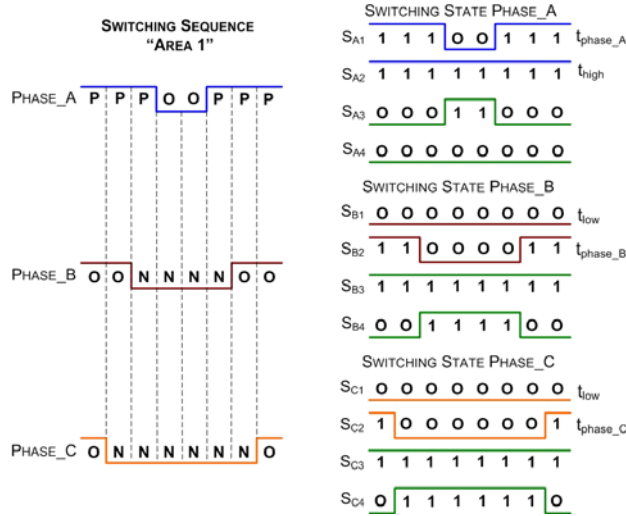Fig. 10. Switching sequence for three and two level inverters.

Fig. 11. States of switches to generate a space voltage-vector in area 1 for the three-level NPC inverter.

and then the switching sequence obtained (see sector I of Fig. 7) with the subroutine svmStd is: (111)-(110)-(100)-(000)-(000)-(100)-(110)-(111).

Fig. 10 shows the signals for the switching sequences corresponding to the three-level and two-level space-vector diagrams. It can be seen that the waveforms are the same for both space-vector diagrams. The only difference is the number of switching states. Hence, it is possible to calculate the switching sequence needed in the three-level space-vector diagram from the switching sequence obtained by the application of the subroutine svmStd.

Fig. 11 illustrates the states of the switches to generate a voltage vector in area 1. The algorithm accounts for the fact that for all of the inverter phases, the pair of switches S_{X1}, S_{X3} and S_{X2}, S_{X4} (X=A, B, C) commutate in a complementary way. Therefore, it is only necessary to calculate the two main control signals for each inverter phase.

It is important to point out that to generate the switching sequence (see Fig. 11), which alternates between the states P and O (phase A), the switch S_{X1} has to be controlled by the signal (t_{phase_X}), which generates the switching sequence (obtained once it is applied to the subroutine svmStd), and the
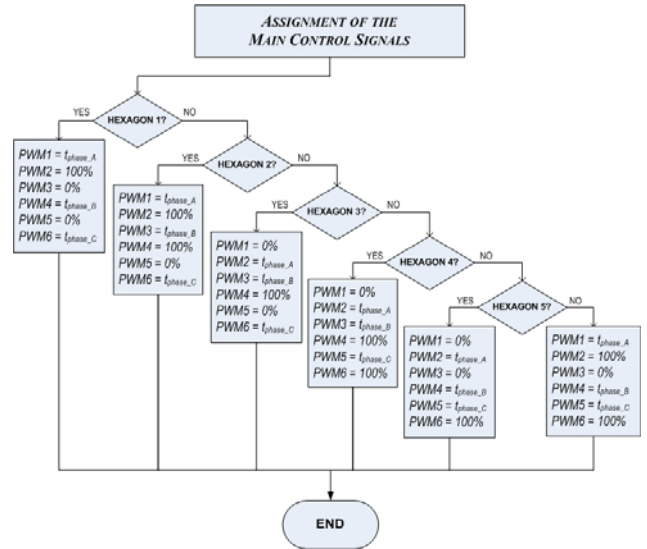

Fig. 12. Flowchart of the algorithm that assigns the duty cycles of the main control signals.

switch S_{X2} has to be kept at a high level (t_{high}). On the other hand when the switching sequence is alternating between the states N and O (phases B and C), the switch S_{X1} has to be kept at a low level (t_{low}) and the switch S_{X2} has to be controlled by the signal (t_{phase_X}), which generates the switching sequence. As a result, the switches S_{X1} and S_{X2} have to be controlled by the main control signals and S_{X3} and S_{X4} have to be controlled by their complementary signals (see Fig. 11).

Once the switching sequence has been defined and analyzed in the 36 areas of the three-level hexagon [8], it can be concluded that to calculate the duty-cycles of the main control signals for the three legs of the three-phase NPC inverter it is only necessary to know the two-level hexagon where the reference vector is located.

Fig. 12 illustrates a flowchart of the algorithm that assigns the duty cycles of the main control signals. PWM1 and PWM2 are the mains control signals of phase A, and so on.

It is worth pointing out that the algorithm can be adapted to any DSP having an embedded subroutine similar to the svmStd from Freescale®.

IV. HARDWARE IMPLEMENTATION

A. Control Circuit

In order to validate the simplified SVM algorithm proposed above a three-level Neutral-Point Clamped inverter was built. Fig. 13 illustrates the control circuit corresponding to phase A. The signals PWM1 and PWM2 are the main control signals as shown in Fig. 12, $\overline{PWM1}$ and $\overline{PWM2}$ are the complementary signals of the main control signals.

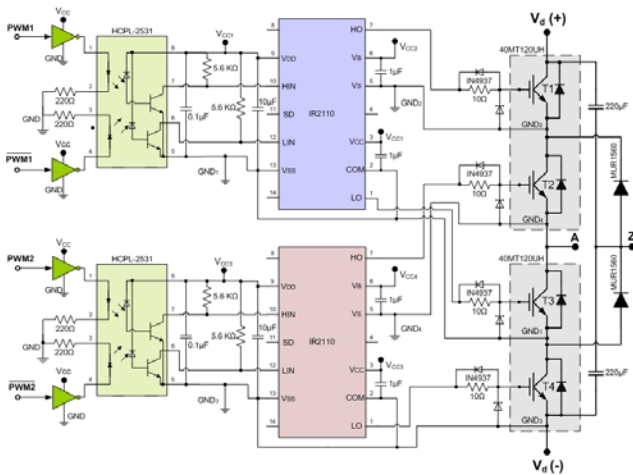Electrical isolation between the control circuits and the

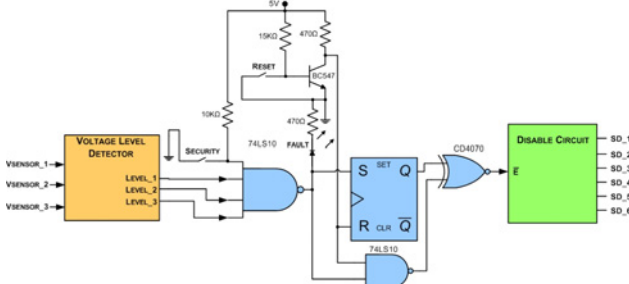Fig. 13.　Hardware used to control a phase of the three level NPC inverter.

Fig. 14.　Protection and restart circuit.

TABLE III
RESTART CIRCUIT SIGNALS

STATE	S	R	Q	OUT	$\overline{E}$	STATE OF THE SYSTEM
START	0	0	1	1	1	DISABLE
RESET	0	1	0	1	0	ENABLE
FAULT	1	0	1	1	1	DISABLE
RESET	1	1	0	0	1	DISABLE
FAULT	1	0	1	1	1	DISABLE
NORMAL	0	0	1	1	1	DISABLE
RESET	0	1	0	1	0	ENABLE

Fig. 15.　Diagram of the experimental setup.

high level voltages of the inverter must be provided. Therefore, the control circuit includes a power stage isolation which was implemented with optocouplers. In order to provide the suitable levels of current and voltage for the gates of the IGBT's an IR2110 gate driver from International Rectifier was used. The IR2110 was designed to control a two-level inverter. However, in this paper the gate driver was used to control a three-level inverter and satisfactory results were obtained. Using a single power supply with a bootstrap circuit for each IR2110, as in the control of a two-level inverter, is not recommended. This is due to the fact that it is not possible to keep the charge of the capacitor for each switching cycle.

B. Protection circuit

Three Hall-effect current sensors were used to implement the protection circuit. The sensors were fitted in such a way that all possible overcurrent faults are detected. The overcurrent detection is based on voltage window detectors which are used to determine whether the current level is in the range of permissible values. Once an overcurrent has been detected the three-level inverter is disabled by means of an input "shutdown SD" of the circuit's IR2110. As the inverter is comprised of six IR2110s, it is necessary to generate six
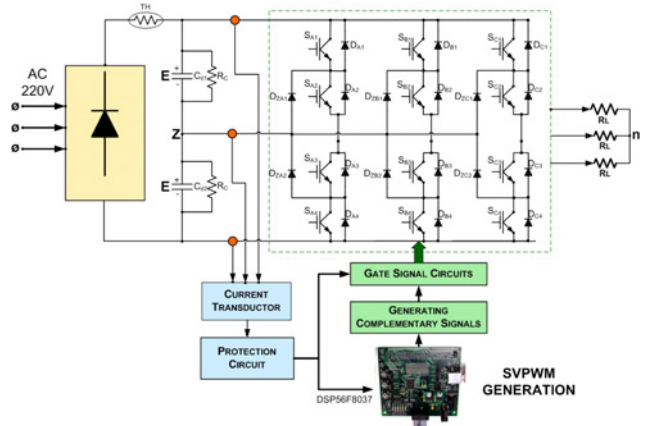
disabling isolated-signals which must be synchronized in order to turn off all the IGBTs at the same time.

Finally, it is necessary to set up a logic circuit to restart the system after a fault condition has been detected. This is very important. Otherwise the system may enter into an oscillating condition (enabling and disabling states). That situation is due to the fact that once a fault is detected the IGBTs are disabled and as a result, the current value decreases until it reaches a value which is within the permissible values and the system is restarted automatically. However if the fault is still there and an overcurrent condition is newly detected then the system goes into an oscillating condition.

To avoid the oscillating condition the restart of the system has been designed to be manual. A normally-open push button is used to restart the system. An additional push-button has been added as a safety measure, this button disables the system under any condition. Fig. 14 shows the implementation of the protection and restart circuits.

Table III shows the possible states of the inverter and the actions of the protection circuits.

V.　EXPERIMENTAL RESULTS

Fig. 16.   Areas involved when the reference vector follows the selected trajectory.

Fig. 17.   Signals obtained by means of the validation algorithm with m=0.8.

With the aim of validating the SVM algorithm an experimental setup was built (see Fig. 15) and a validation test procedure was performed. The experimental validation test consisted of executing the simplified SVM algorithm to make the reference vector follow a trajectory, as illustrated in Fig. 16. The validation algorithm generates a sinusoidal signal and a stepwise waveform by means of digital to analog converters.

The reference values of the modulation index and the fundamental frequency of the output signal are included in the sinusoidal signal. The stepwise signal represents the areas the reference vector goes trough when the SVM algorithm is applied. To generate the stepwise signal, the validation algorithm assigns a voltage level to each area starting from 100 mV for area 1 up to 3.6 V for area 36. Fig. 16 shows a possible trajectory for the reference vector and the areas covered in the trajectory.

Fig. 17 shows the waveforms generated by the validation algorithm. It can be seen that both of the signals have the

Fig. 18.   Interval_1 from 0º to 90º with m=0.8.

Fig. 19.   Interval_2 from 90º to 180º, with m=0.8.

Fig. 20.   Interval_3 from180º to 270º with m=0.8.

Fig. 21.   Interval_4 from 270º to 360º with m=0.8.

Fig. 22. Line-to-midpoint voltage at fSW =1kHz and m=0.8; 5ms/div, 50V/div.
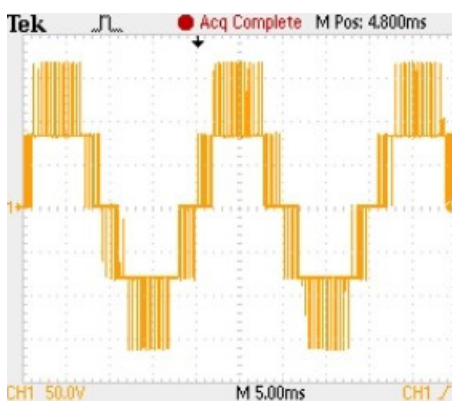

Fig. 23. Line-to-line voltage at fSW =1kHz and m=0.8; 5ms/div, 50V/div.
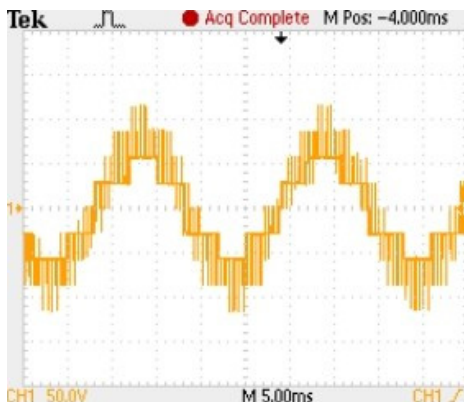

Fig. 24. Line-to-neutral voltage at fSW =1kHz and m=0.8; 5ms/div, 50V/div.

same frequency implying that the algorithm works well.

Figs. 18-21 show the areas covered by the reference vector when it moves along the trajectories previously defined. It can be seen that the areas covered by the vector correspond to the expected trajectory (see Fig. 16). The trajectory of the reference vector can be changed by means of the modulation

ratio and as a result, the areas covered by the reference vector and the time that it stays in each of them changes as well. It is worth pointing out that if only the fundamental frequency desired at the output of the inverter is changed the trajectory does not change. The time that the reference vector stays in those areas is the only thing that will change.

Figs. 22, 23 and 24 illustrate the waveforms of the line-to-midpoint, line-to-line and line-to-neutral voltages. These voltages were obtained by using the simplified SVM algorithm with a switching frequency (f_{sw}) of 1 kHz and a modulation ratio of 0.8.

The line-to-midpoint voltage has three voltage levels +E, 0 and −E. However the inverter never changes directly between states P and N without passing through 0.

The line-to-line voltage has five voltage levels +2E, +E, 0, -E and -2E. Finally, the line-to-neutral voltage has nine voltage levels +4E/3, +E, +2E/3 +E/3, 0, -E/3, -2E/3, -E, and -4E/3.

From the voltage waveforms it can be concluded that the SVM algortihm and the circuit control of the inverter are working well.

VI. CONCLUSIONS

In this paper two algorithms to implement a simplified Space-Vector PWM for a Three-Level VSI were proposed and experimentally validated. The first algorithm for hexagon identification reduces the complexity and execution time of the simplified SVM algorithm reported in [1].

The second algorithm was developed for the assignment of the duty cycles of the main control signals. This algorithm only requires the data of the two-level hexagon in which the reference vector is located. In this second case the embedded subroutine svmStd in the DSP56F8037 of Freescale®, designed for generating SVPWM signals for two-level inverter, was used. In this paper a way to extend this function for three-level inverters was developed.

The design, control and protection of a three-level inverter were experimentally validated. It is worth pointing out that in this paper the use of electronic circuits which were designed to control a two-level inverter were applied in the control of a three-level inverter. Finally a validation procedure to validate the simplified Space-Vector Modulation (SVM) algorithm for a three-level Neutral-Point Clamped (NPC) inverter was developed.

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