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Theoretical Analysis and Control of DC Neutral-point Voltage Balance of Three-level Inverters in Active Power Filters

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Abstract

In recent years, multilevel technology has become an effective and practical solution in the field of moderate and high voltage applications. This paper discusses an APF with a three-level NPC inverter. Obviously, the application of such converter to APFs is hindered by the problem of the voltage unbalance of DC capacitors, which leads to system instability. This paper comprehensively analyzes the theoretical limitations of the neutral-point voltage balancing problem for tracking different harmonic currents utilizing current switching functions from the space vector PWM（SVPWM）point of view. The fluctuation of the neutral point caused by the load currents of certain order harmonic frequency is reported and quantified. Furthermore, this paper presents a close-loop digital control algorithm of the DC voltage for this APF. A PI controller regulates the DC voltage in the outer-loop controller. In the current-loop controller, this paper proposes a simple neutral-point voltage control method. The neutral-point voltage imbalance is restrained by selecting small vectors that will move the neutral-point voltage in the direction opposite the direction of the unbalance. The experiment results illustrate that the performance of the proposed approach is satisfactory.

Key words: Active power filter, DC voltage, Neutral point voltage balancing, Space vector modulation, Three-level NPC inverter

I. INTRODUCTION

Harmonic pollution is regarded as one of the major problems that degrade electric power quality. Particularly, harmonic resonance in power distribution systems can cause excessive voltage and current waveform distortions which can result in consecutive instability, abnormal operation or damage of electric components. Passive filters are sensitive to system impedance and load characteristics. The series and parallel resonance problems of these filters are almost impossible to solve. The control of harmonic perturbations with active power filters (APF) has become a hot topic in the power engineering field. In the past two decades, active power filters have been developed rapidly to suppress harmonics in the power distribution systems of 380V voltage grids [1]-[3]. However, the voltage grids of many power distribution systems for petroleum based power generation is 600V. 690V voltage grids are widely used in power distribution systems for mining and wind power. There are many different voltage grids ranging from 600V to 1000V in the factories for steel-making. Due to the limitations of the voltage and current capability of power devices, it is very difficult to handle nonlinear loads in the voltage grids mentioned above with traditional APFs using two-level inverters in a 380V voltage grid. The DC voltage range of traditional APFs in a 380V voltage grid is usually from 700V to 750V. In these APFs, 1200V IGBTs are widely adopted. If traditional APFs with two-level inverters are adopted in the

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voltage grids mentioned above, a 600V voltage grid needs DC voltage of approximately 1125V, and a 690V voltage grid needs approximately 1294V. A 1000V voltage grid needs a higher DC voltage. Therefore, 1200V IGBTs are not suitable for the voltage grid and only 1700V IGBTs can be applied to a 600V voltage grid after a fashion. The switch frequency of 3300V IGBTs is comparatively low for the application of APFs and their switch loss is high. At present, the general method is combining traditional APFs with a two-level inverter with step-up transformers. However, transformers are very expensive and occupy up to 40% of the total system real estate, which is an excessively large area. Furthermore, their loss is very high and the design of their control system is very difficult due to saturation problems of transformers in transient state.

In recent years, three-level neutral-point-clamped (NPC) PWM inverters have become an effective and practical solution for many moderate voltage application fields. As described in many papers, using this technology, the voltage stress on switches is reduced, the shape of output waveform is improved and the rate of voltage and power can be increased [4], [5]. Evidently, three-level inverters are very suitable for harmonic restriction of the above mentioned voltage grids. Adopting this topology, three-level APFs with 1200V IGBTs may be used direct in a 600V grid and a 690V voltage grid, while three-level APFs with 1700V IGBTs can be directly applied to a 1000V voltage grid. Moreover, the topology can synthesize more output levels which is good for harmonic current tracking. Besides, three-level inverters can be combined with passive filters to form the hybrid filters used in a 6.6kV grid. The hybrid filters can use 1200V IGBTs at a reasonable cost from the market [6]-[9]. At present, APFs with three-level NPC inverters have received more and more attention in recent years [6]-[17].

However, the DC voltage control of active power filters is important for the dynamic performance and stability of filter systems. To make a PWM converter work properly, the DC voltage must be maintained high enough to keep the diodes of the bridge reverse biased. Otherwise proper function of the APF will not be achieved. The DC voltage of a PWM converter drops due to the DC capacitor loss during operation. Therefore, a proper control method should be adopted to keep the DC voltage invariable. Furthermore, the neutral-point (NP) voltage balancing problem, which is an inherent problem of the three-level NPC topology, restricts the development and application of three-level NPC inverters to APFs. To improve the performance of a filter system, it is important to devise a regulator to maintain neutral-point voltage balancing.

In three-level inverters, the AC currents flow out of or into the neutral point as an effect of some of the switching states. These currents produce ripples and excursions in the NP voltage. Without NP voltage balancing control, the excursions in NP voltage will greatly increase, and even the DC-link capacitors and the switching devices will probably be destroyed. In recent years, comprehensive studies have been carried out on the NP voltage balancing control problem [18], [19]. However, these studies have been confined to three-level inverters, STATCOMs and PWM rectifiers with sinusoidal current inputs or outputs.

Because APFs compensate harmonic currents, the components of the AC currents flowing out of or into the neutral point are more complicated for three-level APFs than for three-level inverters, STATCOMs and PWM rectifiers. Few studies have theoretically analyzed the status of the NP voltage caused by the non-sinusoidal harmonic currents flowing out of or into the neutral point. Few studies have addressed voltage-balancing control for three-level APFs. [14] presents a DC voltage control method. However, this control method needs to know accurately the equivalent resistances of the two DC capacitances. This control method is not applied. [15] present the selecting of appropriate small space vectors to control the DC neutral-point voltage balance. Simulation and experimental results were presented to validate that the performance of the scheme is very good. In [6]-[9], the authors propose neutral-point voltage control methods based on triangle-carrier modulation by superimposing the 6th-harmonic zero-sequence voltage and/or the second harmonic negative-sequence voltage with an appropriate amplitude and an initial phase on the active-filter voltage reference in each phase. Experimental waveforms obtained from a 400-V 15-kW down-scaled system verify the viability and effectiveness of the proposed hybrid filter, keeping the two dc capacitor voltages well balanced. However, the methods in these articles [6]-[9],[15] do not consider how to control the NP voltage while restricting the dv/dt of the output voltage and diminishing the switching loss synchronously. These three articles do not analyze comprehensively the status of the NP voltage for tracking different harmonic currents. An auxiliary circuit is used to keep the capacitors charged to equal voltages in [16], [17]. However, these auxiliary circuits makes the main circuit of the equipment more complicated.

This paper mainly focuses on the analysis and control of the DC voltage for three-level APFs. In this paper, a comprehensive analysis of the theoretical limitations of the NP voltage balancing problem for tracking different harmonic currents utilizing current switching functions from the space vector PWM（SVPWM）point of view is set up. The fluctuation of the neutral point, caused by load currents of certain order harmonic frequencies, is reported and quantified. A control method for the DC voltage close loop is presented. A PI controller regulates the DC voltage in the outer-loop controller. In the current-loop controller, this paper researches the issues of neutral-point voltage control from the SVPWM point of view. Then this paper proposes a simple

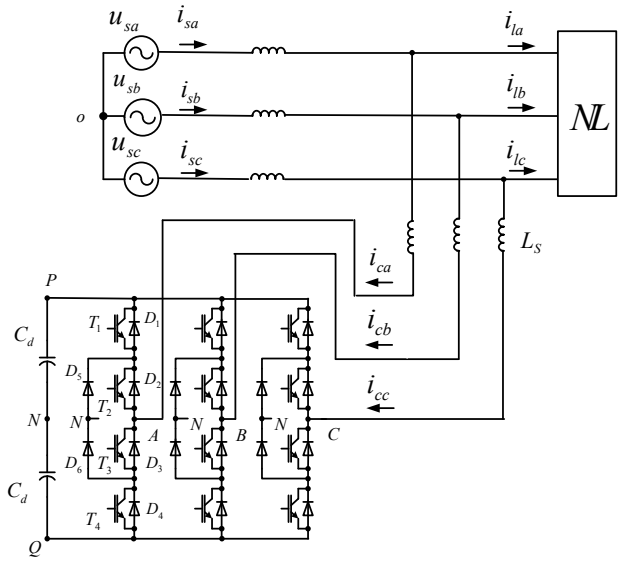

Fig. 1. Schematic diagram of the active power filter with three-level inverter.

neutral-point voltage control method. The method selects appropriate small space vectors to control the neutral-point voltage without increasing the switching loss or the *dv*/*dt* of the output voltage. Experiment results illustrate that the performance of the proposed approach is satisfactory.

II. MATHEMATIC MODEL AND CONTROL SYSTEM

The operating principle behind an APF is shown in Fig.1. The periodic non-sinusoidal current, which flows over nonlinear load (NL), can be resolved into the fundamental current component i_1 and the summation of all of the harmonic current components i_h. The reference directions of the currents are defined as shown in Fig.1. u_{sa}, u_{sb} and u_{sc} are the three-phase voltages, i_{ca}, i_{cb} and i_{cc} are the currents of the APF, and i_{la}, i_{lb} and i_{lc} are the nonlinear load currents. After the load currents flow through the current transformers, the desired currents, which the APF needs to compensate, are obtained by the detecting circuit of the harmonic currents. Then the desired currents are injected into the power system with the APF controlling the PWM inverter. As can be seen from Fig.1, the source current i_s is provided with both the load current i_l and the output current i_c of the APF, i.e., $i_s = i_l + i_c$. Since $i_c = -i_h$, the power source only supplies i_1. Hence i_s, after compensation, becomes a sinusoidal current which has a frequency that is identical to u_s. This is the basic operating principle of an APF.

The three-level NPC inverter applied to the APFs, as shown in Fig. 1, is built-up of twelve switches, each one with its freewheeling diode, and six power diodes that allow the connection of the phase outputs to the middle voltage. The blocking voltage of each switch is 1/4 of the DC voltage.

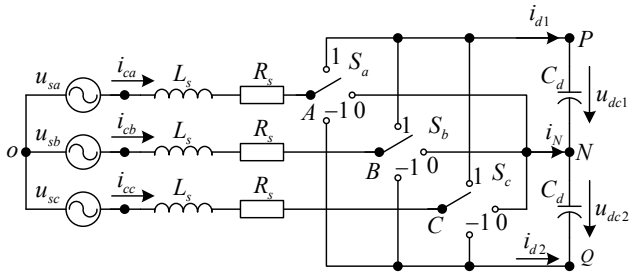

Fig. 2. The equivalent circuit of the active power filter with three-level.

Each arm of the inverter can be clamped to the DC terminals P, N and Q, and they can produce three switching states. When the upper two switches T_1 and T_2 are switched on, the output of this phase is connected to DC terminal P. When the middle two switches T_2 and T_3 are switched on, the output of this phase is connected to middle point N. Similarly when the lower two switches T_3 and T_4 are switched on, the output of this phase is connected to Q. The allowed logic configurations of the NPC switches can provide the three different output voltage values furnished by each NPC inverter phase. The states of T_1, T_2, T_3 and T_4 are complementary. The two switches for each phase of the NPC inverter are closed, whilst the other two are opened during every time instant [4].

In this paper, the losses of the switching devices and snubber circuits are ignored. Based on the concept of switching function (SF), the equivalent switch-circuit of a three-level NPC APF can be obtained as in Fig.2. The power loss on resistor R is assumed to include all of the losses of this filter. The three phase source voltage is assumed to be balance and symmetrical. The switching state of phase A, S_a for the power devices T_{1a}-T_{4a}, is defined as:

$$S_a = \begin{cases} 1, & T_{1a}, T_{2a}\text{ON and } T_{3a}, T_{4a}\text{OFF} \\ 0, & T_{2a}, T_{3a}\text{ON and } T_{1a}, T_{4a}\text{OFF} \\ -1, & T_{3a}, T_{4a}\text{ON and } T_{1a}, T_{2a}\text{OFF} \end{cases} \quad (1)$$

The switch states are coded by the symbols -1, 0 and 1 identifying the three voltage levels in each inverter phase. To get a mathematic model of the APF, S_a is decomposed as:

$$\begin{cases} S_{1a}=1, S_{2a}=0, S_{3a}=0 & S_a=1 \\ S_{1a}=0, S_{2a}=0, S_{3a}=1 & \text{when, } S_a=0 \\ S_{1a}=0, S_{2a}=1, S_{3a}=0 & S_a=-1 \end{cases} \quad (2)$$

Using the same method, S_b and S_c are decomposed too. Then, a comprehensive mathematic model of a three-level inverter in the stator coordinates is established as follows:

$$Z\dot{X} = A \cdot X + B \cdot e \quad (3)$$

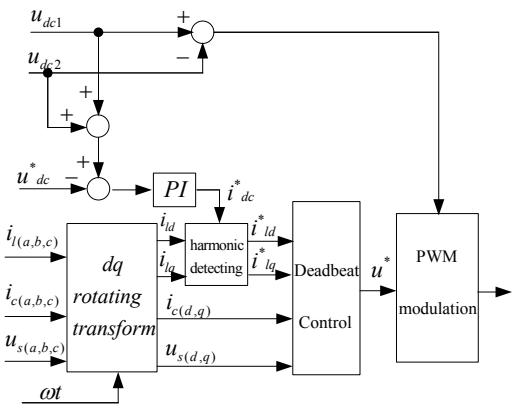

Fig. 3. Block diagram of control system of the active power filter with three-level inverter.

where:

$$Z = diag[L_s \quad L_s \quad L_s \quad C_d \quad C_d]$$

$$X = [i_{ca} \quad i_{cb} \quad i_{cc} \quad u_{dc1} \quad u_{dc2}]^T$$

$$A = \begin{bmatrix} -R_s & 0 & 0 & -S_{1a} + \frac{S_{1a}+S_{1b}+S_{1c}}{3} & S_{2a} - \frac{S_{2a}+S_{2b}+S_{2c}}{3} \\ 0 & -R_s & 0 & -S_{1b} + \frac{S_{1a}+S_{1b}+S_{1c}}{3} & S_{2b} - \frac{S_{2a}+S_{2b}+S_{2c}}{3} \\ 0 & 0 & -R_s & -S_{1c} + \frac{S_{1a}+S_{1b}+S_{1c}}{3} & S_{2c} - \frac{S_{2a}+S_{2b}+S_{2c}}{3} \\ S_{1a} & S_{1b} & S_{1c} & 0 & 0 \\ -S_{2a} & -S_{2b} & -S_{2c} & 0 & 0 \end{bmatrix}$$

$$B = diag[1 \quad 1 \quad 1 \quad 0 \quad 0]$$

$$e = [u_{sa} \quad u_{sb} \quad u_{sc} \quad 0 \quad 0]^T$$

To simplify the mathematic model, the synchronous rotating coordinate transformation is used. A mathematical model of a tri-level system in the rotating *dq* frame is expressed as follows:

$$Z\dot{X} = A \cdot X + B \cdot e \tag{4}$$

where:

$$Z = diag\left[L_s \quad L_s \quad C_d \quad C_d\right]$$

$$X = \left[i_{cd} \quad i_{cq} \quad u_{dc1} \quad u_{dc2}\right]^T$$

$$A = \begin{bmatrix} -R_s & \omega L_s & -S_{d1} & S_{d2} \\ -\omega L_s & -R_s & -S_{q1} & S_{q2} \\ S_{d1} & S_{q1} & 0 & 0 \\ -S_{d2} & -S_{q2} & 0 & 0 \end{bmatrix}$$

$$B = [1 \quad 1 \quad 0 \quad 0]$$

$$e = \left[u_{sd} \quad u_{sq} \quad 0 \quad 0\right]$$

By this means, the three-phase alternating signal is changed into a two-phase alternating signal. Thus the mathematic model of this APF is predigested.

Base on the *dq* mathematic model, the control system of the APF is designed. The diagram of the control system is shown in Fig.3. The control system includes the outer-loop voltage controller and the inner-loop current controller [20]. In the outer-loop controller, the DC voltage value is detected and regulated by the PI controller using the active command current. The inner-loop current controller is divided into the detection module for calculating the harmonic command current and the control module for tracking the command current. The method for detecting the harmonic currents based on the instantaneous reactive power theory is adopted in the detection module. The control module deals with shaping the current waveforms to track the references. The command current of the control module is composed of the DC voltage regulator component and the harmonic current compensator component. In order to control the shape of the output current waveform, the deadbeat control technology is adopted [21]. The command voltage given by the deadbeat control is modulated by the three-level SVPWM strategy.

III. Analysis and Control of DC Voltage

Obviously, regulating DC voltage fast and precisely is one of the keys to designing an APF. As shown in Fig.3, the DC voltage is regulated by the PI controller using the active command current in the outer-loop controller:

$$i_{dc} = (k_p + \frac{k_I}{s})(u_{dc} - u^*_{dc}) \tag{5}$$

The PI controller allows the PWM converter to operate in a self-sufficient manner without a DC source. The DC capacitor is initially given a voltage value. The DC voltage is measured and compared to the reference voltage. An error signal is obtained, and is used to command the magnitude of the three phase active currents in the APF. The PI controller regulates the DC voltage to the reference voltage value by having the PWM converter work as a PWM rectifier. Finally, the DC voltage is maintained invariable by the PI controller during the APF operation.

Obviously, the mean value of the DC voltage should be the control objective. The adaptive filter is adopted to detect the mean value of the DC voltage. The adaptive filter has the advantages of good bandwidth behavior, a simple algorithm, automatic tracking of the grid frequency and robustness to circuit parameter variations. As a result, it has received a great deal of attention in recent years [22]. A block diagram of the adaptive filter is shown in Fig.4, where *n* refers to the *n*-th calculation, the filter input signal $u_{dc}(n)$ is sampling the datum of the DC voltage value u_{dc}, the filter referring the input signal $x(n)$ is 1, ω is a weighting factor which expresses the weighting value of the referring input signal $x(n)$, $y(n)$ represents the filter output signal and $e(n)$ is the feedback error signal. Based on the principle of the adaptive

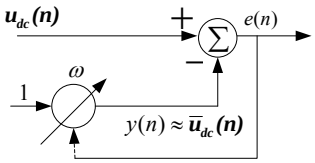

Fig. 4. The block diagram of adaptive filter.

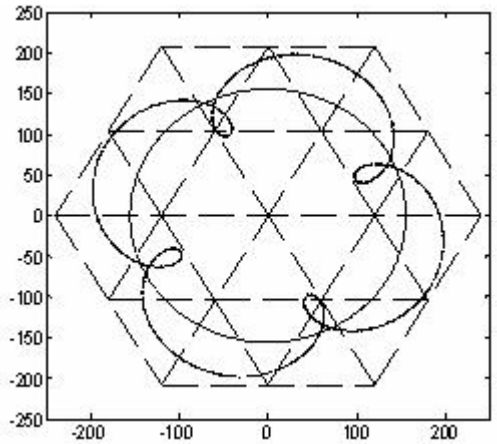

Fig. 5. The command voltage tracking 5th harmonic current.

filter, the adaptive filter output $y(n)$ can be expressed as:

$$y(n)=\omega(n)\cdot x(n)=\omega(n)\cdot 1 \tag{6}$$

Therefore, the equation for the feedback error signal $e(n)$ is:

$$e(n)= u_{dc}(n)-y(n)= u_{dc}(n)- \omega(n) \tag{7}$$

In the Least-Mean-Square algorithm, the iterative equations of the weighting vector ω can be represented as:

$$\omega(n+1)= \omega(n)+\mu e(n) \tag{8}$$

where μ is the step-size parameter. In this algorithm, the average value of u_{dc} is the expected signal. The system uses the error signal $e(n)$ to update the weight $\omega(n)$ to track the change of $\omega^*(n)$. $\omega^*(n)$ is the weight which expresses the weighting value of the detection system. In this way, $y(n)$ can track changes in the average value of u_{dc}. The output signal $y(n)$ approximates the average value of u_{dc}. Thus an adaptive filter for detecting the DC voltage is realized. When the average value of u_{dc} is put into equation (5), the active command current is gained.

In three-level inverters, the AC currents flow out of or into the neutral point to produce ripples and excursions in the NP voltage as an effect of some of the switching states. The neutral-point voltage unbalance of DC capacitors leads to instability of the whole system. The switching state sequence is determined by the modulation strategy, and therefore the imbalance issues of the neutral-point voltage from the SVPWM point of view can be studied. The three-level

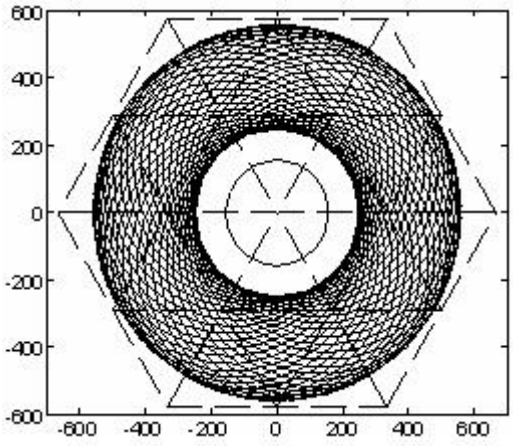

Fig. 6. The command voltage tracking 43th harmonic current.

inverter is characterized by 27 different switch configurations. These configurations produce 19 different voltage space vectors. The 19 voltage vectors of the three-level inverter divided the vector plane into 6 major triangular sectors. Each major sector contains 4 minor triangular sectors. According to the magnitudes of the space voltage they can be classified into four kinds, six large vectors, six medium vectors, twelve small vectors and three zero-voltage vectors.

The process of performing the SVPWM strategy is determined by the command voltage. Because the APFs compensate for the harmonic currents, the command voltage has a large harmonic component. The command voltage of the APF is different from that of the inverter. The trajectory of the corresponding reference vector of the command voltage tracking a certain harmonic current is theoretically analyzed. The command voltage is expressed as follows:

$$\begin{cases} u_a^* = -R_s \cdot i_{ca}^* - L_s \cdot \dfrac{di_{ca}^*}{dt} + u_{sa} \\ u_b^* = -R_s \cdot i_{cb}^* - L_s \cdot \dfrac{di_{cb}^*}{dt} + u_{sb} \\ u_c^* = -R_s \cdot i_{cc}^* - L_s \cdot \dfrac{di_{cc}^*}{dt} + u_{sc} \end{cases} \tag{9}$$

i_{ca}^*, i_{cb}^* and i_{cc}^* are the command currents. The trajectory of the reference vector is gained with the Matlab software from expression (9). If the command currents are 5th harmonic currents with a current peak value of 15A, the trajectory of the calculated reference vector is shown in Fig.5. The parameters of the matlab simulation system are listed in Table I. The parameters of the simulation system are consistent with the experimental system below. A suitable DC voltage is chosen to modulate the command voltage properly. The broad line is the trajectory of the reference vector and the circle is the trajectory of the power voltage. The broken line is the three-level space vector diagram. The

TABLE I

THE PARAMETERS OF SIMULATION SYSTEM

Symbol	Experiment	Explanation
U_s	110V	RMS phase voltage value
f_s	50Hz	Power frequency
L_s	2mH	Inductance of APF output filter
R_s	0.5Ω	Resistor of the inductance L_s
U_{dc}	360V	DC voltage of the APF
C_d	4700μF	DC voltage capacitance
I_c	15A	Output peak current value of the APF
f_5	250Hz	Output current frequency

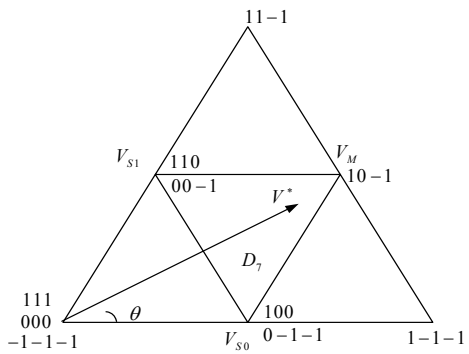

Fig. 7. Space vector diagram.

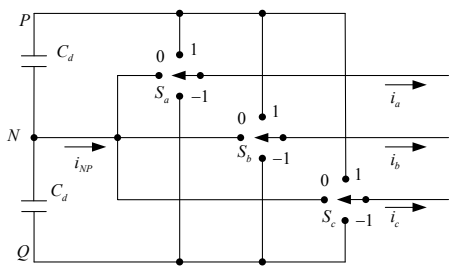

Fig. 8. The equivalent circuit of three-level inverter.

trajectory of the reference vector is compared with the harmonic currents of different frequencies having the same current peak value. When the command current is the 43th harmonic current with a current peak value of 15A, the calculated trajectory of the reference vector is shown in Fig.6. When the frequency of the harmonic currents increases, the voltage of the APF output filter increases. As a result, the command voltage increases too. In order to modulate the command voltage properly, the DC voltage of the APF is increased to 1000V.

The command voltage can be resolved into the fundamental voltage component u_s and the harmonic voltage component $-R_s \cdot i_{ca}^* - L_s \cdot \frac{di_{ca}^*}{dt}$. Evidently, the harmonic voltage component of the command voltage tracking 43th harmonic current is larger than that tracking 5th harmonic current. The relative duration of the fundamental voltage component and the harmonic voltage component will change when the frequency of the harmonic currents increase. When the frequency of the harmonic currents is higher, the proportion of the harmonic voltage component is larger and the command voltage will vary more quickly. Fig.5 and Fig.6 demonstrate that the reference vector of the APF sweeps more triangular sectors than that of the inverters. Therefore, the neutral-point voltage unbalance problem is more complicated for three-level APFs.

TABLE II

NEUTRAL-POINT CURRENTS FOR SWITCHING STATES

0-1-1	i_a	00-1	$-i_c$	10-1	i_b
-10-1	i_b	-100	$-i_a$	01-1	i_a
-1-10	i_c	0-10	$-i_b$	-110	i_c
110	i_c	100	$-i_a$	-101	i_b
011	i_a	010	$-i_b$	0-11	i_a
101	i_b	001	$-i_c$	1-10	i_c

The reference vector may be synthesized using the space vector modulation of the three switching state vectors that are nearest to the reference vector in every sampling instant. As shown in Fig. 7, when the reference vector V^* falls into sector D_7, V^* is synthesized by V_{S1}, V_{S0}, and V_M. V_M has only one switching state. V_{S1} and V_{S0} have two redundant switching states. Each phase output can be connected to either P, N or Q in different switching states. In this case, the phase output is connected to the neutral point N, which results in the current disturbing the NP voltage balance. Fig.8 shows an equivalent circuit of the three-level APF employing a three-state switch to replace each three-level bridge leg. Each switching state affecting the NP balance is analyzed and the results are summarized in Table II.

As shown in Table II, the large vectors do not affect the NP balance because they connect the phase currents to either the positive or negative dc rail, and the NP remains unaffected. Medium vectors connect one of the phase currents to the NP making the NP potential dependent, in part, on the power system conditions. They are the most important source of NP potential unbalance. Small vectors come in pairs. Their redundant switching states generate the same output voltages. A small vector that connects a phase current to the NP without changing the sign of the current will be referred to as a positive small vector. The other one, which connects a phase current with a negative sign, will be called a negative small vector. Small vectors are controllable for NP potential unbalance. The relative duration of positive and negative small vectors may be adjusted within the duty cycle of the small vector.

The NP current produced by small and medium vectors depends not only on the reference vector, but also on the AC currents flowing out of or into the neutral point. Moreover, the components of the AC currents flowing out of or into the

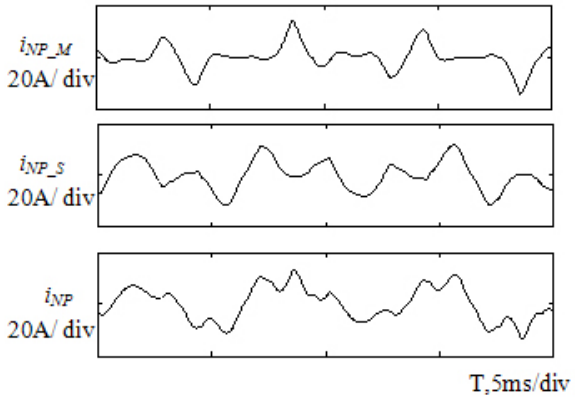

Fig. 9. The NP current caused by 5th harmonic current.

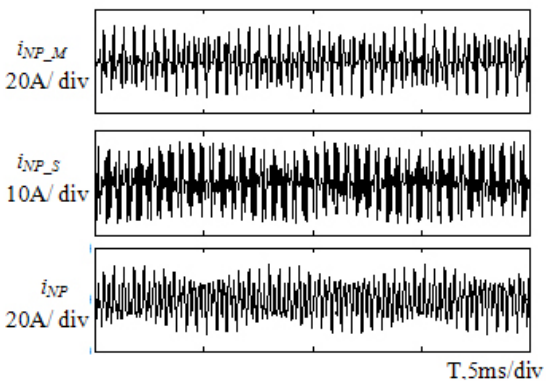

Fig. 10. The NP current caused by 43th harmonic current.

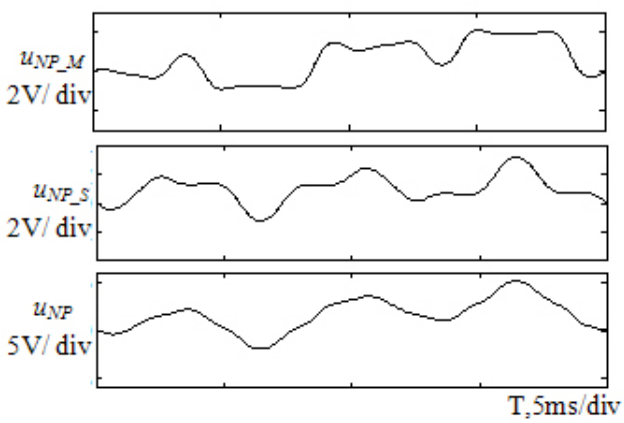

Fig. 11 The excursion in NP voltage caused by 5th harmonic current

neutral point are more complicated for three-level APFs. In [18], the NP current produced by medium vectors can be represented as:

$$i_{NP\_mediu\_vector} = d_M \cdot [M_a \quad M_b \quad M_c] \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{10}$$

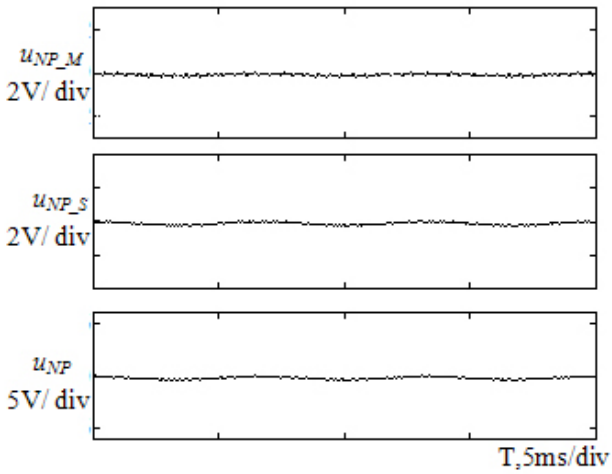

Fig. 12. The excursion in NP voltage caused by 43th harmonic current.

d_M is the duty cycle of the medium switching state vector. However, it represents the duty cycle of different switching state vectors in different sectors over the output voltage line cycle. The current switching functions M_a, M_b and M_c define a mapping between the duty cycle of the different switching state vectors used in different sectors, and the NP current that those vectors produce.

In [18], the NP current produced by the small vectors can be represented as:

$$i_{NP\_small\_vector} = [m_{S0} \quad m_{S1}] \cdot \begin{bmatrix} d_{S0} & 0 \\ 0 & d_{S1} \end{bmatrix} \cdot \begin{bmatrix} S0_a & S0_b & S0_c \\ S1_a & S1_b & S1_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{11}$$

d_{S1} and d_{S0} are the duty cycles of the small switching state vectors. The current modulation index m_{S1}, m_{S0} is the relative duration of the positive and negative small vectors within the duty cycle of the small vector. In other words, the duty cycle of the vector V_{S0}(100) is $(1+m_{S0})\ d_{S0}/2$, and the duty cycle of the vector V_{S0}(0-1-1) is $(1-m_{S0})\ d_{S0}/2$, $m_{S0}, m_{S1} \in [-1,1]$. $S0_a$, $S0_b$, $S0_c$, $S1_a$, $S1_b$ and $S1_c$ are the current switching functions of the small vectors. By combining expressions (10) and (11), a single expression valid for the NP current over the entire line cycle can be defined as:

$$i_{NP} = d_M \cdot [M_a \quad M_b \quad M_c] \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \tag{12}$$

$$[m_{S0} \quad m_{S1}] \cdot \begin{bmatrix} d_{S0} & 0 \\ 0 & d_{S1} \end{bmatrix} \cdot \begin{bmatrix} S0_a & S0_b & S0_c \\ S1_a & S1_b & S1_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

The fluctuations and excursions in the NP voltage caused by certain order harmonic currents using the same parameters given above are quantifiably analyzed. The NP current is calculated using the formulas (10), (11) and (12). Fig.9 shows the NP current caused by the 5th order harmonic current.

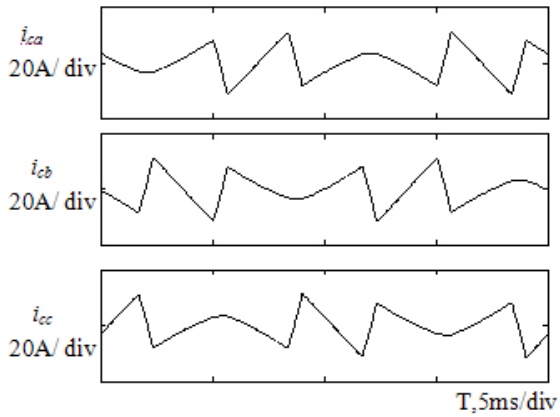

Fig. 13. The typical harmonic currents.

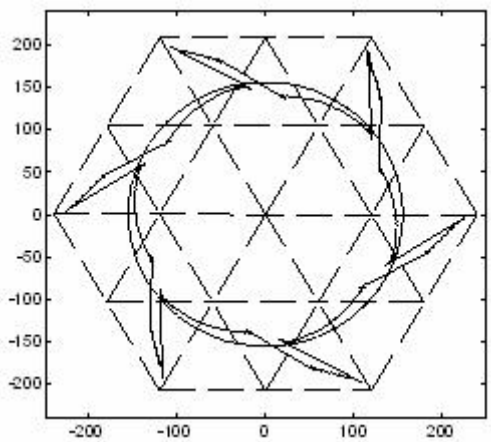

Fig. 14. The command voltage tracking typical harmonic current.

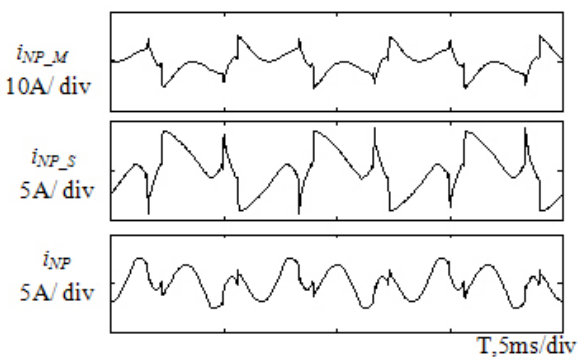

Fig. 15. The NP current caused by typical harmonic current.

Fig.10 shows the NP current caused by the 43rd order harmonic current. Weighing factors are set when only positive small vectors are used (i.e., m_{S0}= m_{S1}=*1*). From the circuit diagram in Fig.8, the excursion in the NP voltage caused by the NP current can be calculated as:

$$u_{NP} = u_{dc1} - u_{dc2} = \int_0^{+\infty} \frac{i_{NP}}{C_d} dt \qquad (13)$$

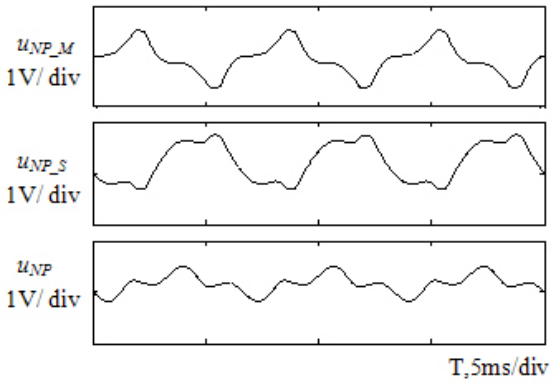

Fig. 16. The excursion in NP voltage caused by typical harmonic current.

The excursion in the NP voltage is calculated using the formula (13). Fig.11 shows the excursion in the NP voltage caused by the 5th order harmonic current. Fig.12 shows the excursion in the NP voltage caused by the 43rd order harmonic current.

The trajectory of the command voltage and the command harmonic current determine the value of the NP current from formulas (10) and (11). The reference vector varies more quickly for tracking the 43rd order harmonic current. The duty cycles of small and medium vectors vary more acutely for tracking the 43rd order harmonic current too. Moreover, the frequency of the 43th harmonic current is obviously higher than that of the 5th harmonic current. Therefore, Fig.9 and Fig.10 show that the fluctuation frequency of the NP current for tracking the 43th harmonic current is higher than that for tracking the 5th harmonic current. Based on formula (13), the amplitude of the fluctuation in the NP voltage caused by the harmonic current is worked out. The amplitude of the fluctuation in the NP voltage caused by the 43th harmonic current is smaller than the 5th harmonic current from Fig.11 and Fig.12. It is concluded that the amplitude of the fluctuation in the NP voltage caused by a high frequency harmonic current is smaller than that of a low frequency harmonic current. This is based on a large numbers of simulation results. Therefore, the NP voltage can be controlled more easily when the frequency of the command harmonic current is higher.

In order to further explain this conclusion, two extreme conditions are analyzed as follows. When the command harmonic current is very small, the harmonic voltage component is very small. Therefore, the command voltage is approximately equal to the power voltage u_s. The trajectory of the command voltage and the command harmonic current determine the value of the NP current from formulas (10) and (11). Therefore, if the trajectory of the command voltage is similar, the NP current is determined by the command harmonic current. If the frequency of the command harmonic current is higher, the fluctuation frequency of the NP current

is higher. Therefore, the amplitude of fluctuation in the NP voltage caused by a high frequency harmonic current is smaller than that of a low frequency harmonic current.

When the command harmonic current is very large, the harmonic voltage component is very large. The command voltage is approximately equal to the harmonic voltage component $-R_s \cdot i_{ca}^* - L_s \cdot \frac{di_{ca}^*}{dt}$. The reference vector tracking the *N*-order harmonic current circles around the centre of the circle approximately *N* times over the entire line cycle. When the harmonic currents have the same current peak value, the harmonic voltage components increase along with the frequency of the harmonic current. In order to contrast the fluctuation of the NP voltage in different frequencies, DC voltage is chosen to make three-level APFs work appropriately in approximately the same modulation index. Evidently, when the reference vector tracking the *N*-order harmonic current circles *N* times, the frequency of the duty cycles of small and medium vectors and current switching functions is *N* times the fundamental frequency. Therefore, the frequency of the NP current is *N* times the fundamental frequency. Thus the amplitude of the fluctuation in the NP voltage caused by a high frequency harmonic current is smaller than that of a low frequency harmonic current.

Similarly, the weighing factors are set when only negative small vectors are used (i.e., $m_{S0}= m_{S1}=-1$). This conclusion is in agreement with only positive small vectors. The weighing factors are set when the positive and negative small vector are alternatively selected in each new switching cycle. The NP current caused by small vectors is approximately equal to zero. The NP current is determined by medium vectors. Only medium vectors can cause a fluctuation in the NP voltage and they can not produce an excursion in the NP voltage. When the frequency of the command harmonic current is higher, the fluctuation frequency of the NP current caused by the medium vectors is higher. This conclusion is in agreement with the above paragraphs. Evidently, a conclusion can be drawn that an unsuitable choice of the positive and negative small vectors might cause an excursion in NP voltage and a suitable choice of the positive and negative small vectors may counteract the NP current caused by the medium vectors from Fig.9 , Fig.10 , Fig.11 and Fig.12.

The actual load harmonic current is a summation of the harmonic currents of different frequencies. A typical three-phase bridge rectifier with an inductance and a resistance is analyzed. The nonlinear load is consistent with the following actual experiment circuits. The load harmonic currents are shown in Fig.13. The trajectory of the reference vector is shown in Fig.14. Fig.15 shows the NP current caused by a typical harmonic current. Fig.16 shows that the excursion in the NP voltage caused by the NP current.

As shown in Fig.13, the typical load harmonic current is mostly a low frequency harmonic current. Fig.14 show that the reference vector tracking a typical harmonic current varies acutely when the typical harmonic current has an abrupt change. The fluctuation amplitude of the NP current and the NP voltage are relatively large from Fig.15 and Fig.16. It was found that the amplitude of the fluctuation in the NP voltage may be larger when the amplitude of the harmonic current increases in the simulation results. Furthermore, a perfectly balanced load and a perfectly balanced PWM scheme are unlikely to happen in practice. The experiment results of an actual power circuit will be different from Fig.11, Fig.12 and Fig.16. The method of controlling the NP voltage with only positive small vectors, negative small vectors or selecting the positive and negative small vectors alternatively in each new switching cycle will produce not only fluctuations but also excursions in the NP voltage. Thus an appropriate method must be presented to control the NP voltage.

Through an analysis of the above paragraphs can be determined that NP voltage may be adjusted by controlling the positive and negative small vectors to produce the opposite NP current with medium vectors. Based on this information, the adopted control method of balancing the NP voltage requires knowledge of the current direction in each phase and selection of the small vectors that will move the NP voltage in the direction opposite the direction of the unbalance. Moreover, the small vectors should be selected without increasing the switching loss and the dv/dt of the output voltage.

As mentioned above, when the reference vector V^* falls into sector D_7, V^* is synthesized by V_{S1}, V_{S0}, and V_M. In order to restrict the switching loss and the dv/dt of the output voltage in a small range and to implement the transition between different sectors smoothly, the switching states of the reference vector may modulate as following sequence: (110)→(100)→(10–1)
→(00–1)→(0–1–1)→(0–1–1)→(00–1)→(10–1)→(100)→(110). The switch state of one phase only changes every time and the changing amplitude does not exceed $u_{dc}/2$.

As shown in Fig.7 and Table II, the switching states of V_{s0}, (100) and (0–1–1) cause the phase currents $–i_a$ and i_a to flow into the NP, respectively. V_{s1}, (110) and (00–1) cause i_c and $–i_c$ to flow into the NP. When the NP voltage is higher than the reference voltage, the switching states moving the NP voltage lower are selected [19]. Similarly, the switching states moving the NP voltage higher are rejected. On the other hand, when the NP voltage is lower than the reference, the same principle is employed. For example, when the NP voltage is lower than the reference voltage and i_c and i_a are bigger than zero, the switching states (110) and (0–1–1) moving the NP voltage lower are rejected. Thus the switching state sequence changes from: (110)→(100)→(10–1)
→(00–1)→(0–1–1)→(0–1–1)→(00–1)→(10–1)→(100)→(110) to (100)→(10–1)→(00–1)→→(00–1)→(10–1)→(100).

TABLE III
THE NP CONTROL METHOD IN SECTOR D_7

NP potential	Output current	Modulation strategy
ΔV_{NP} ≥0	i_c≥0 i_a≥0	(110)→(100)→(10–1)→(00–1)→(0–1–1) →(0–1–1)→(00–1)→(10–1)→(100)→(110)
	i_c≥0 i_a<0	(110)→(100)→(10–1)→(00–1)→(00–1)→(10–1)→(100)→(110)
	i_c<0 i_a≥0	(100)→(10–1)→(00–1)→(0–1–1)→(0–1–1)→(00–1)→(10–1)→(100)
	i_c<0 i_a<0	(100)→(10–1)→(00–1)→(00–1)→(10–1)→(100)
ΔV_{NP} <0	i_c≥0 i_a≥0	(100)→(10–1)→(00–1)→(00–1)→(10–1)→(100)
	i_c≥0 i_a<0	(100)→(10–1)→(00–1)→(0–1–1)→(0–1–1)→(00–1)→(10–1)→(100)
	i_c<0 i_a≥0	(110)→(100)→(10–1)→(00–1)→(00–1)→(10–1)→(100)→(110)
	i_c<0 i_a<0	(110)→(100)→(10–1)→(00–1)→(0–1–1)→(0–1–1)→(00–1)→(10–1)→(100)→(110)

By doing this, the SVPWM merits of restricting the switching loss and the *dv*/*dt* of the output voltage in a small range still remain when the small vectors are selected. This modulation strategy is shown in Table III in detail. The principle is applied to whichever sector the reference vector falls into.

IV. EXPERIMENT RESULT

Theoretical analysis results are necessary to further verify the actual circuits. A diagrammatic sketch of the experimental power circuits is shown in Fig.1. The parameters of the circuit and the control system model for the experiment are listed in Table IV. All of the control algorithms are implemented in digital-signal processors (DSP) TMS320F2407. The nonlinear load is the three-phase bridge rectifier with an inductance and a resistance. The source voltage is u_s=110V/50H, and the impedance of the voltage source is L_S=1mH. A P-MOSFET 2SK1020 is selected as the switching device. Some important experimental oscillograms are shown as follows:

During the APF startup operation, the DC capacitors are initially given a voltage value of 270V by the freewheeling diodes of the switches working as a three-phase bridge rectifier. The DC voltage is compared to a reference voltage of 360V, and then the PI controller regulates the DC voltage

TABLE IV
THE PARAMETERS OF THE CIRCUIT AND CONTROL SYSTEM

Symbol	Experiment	Explanation
U_s	110V	the RMS phase voltage value
f	50Hz	Power frequency
L_s	2mH	the filter inductance
R_s	0.5Ω	the resistor of APF output filter
u_{dc}	360V	DC voltage of the filter
C_d	4700μF	DC capacitor of the filter
f_s	9.6kHz	sampling ¥switch frequency
k_p	1.6	the DC controller parameter
k_I	64	the DC controller parameter

to the reference voltage value by the PWM converter working as a PWM rectifier. When the output command current of the PI controller is larger than 0.5A, the output command current is restricted to 0.5A. The NP voltage is synchronously controlled. Fig.17 shows the experimental waveforms of the DC voltage and the neutral-point voltage difference during the APF startup operation, where waveform 1 is the DC voltage u_{dc} (u_{dc1}+u_{dc2}) and waveform 2 is the voltage difference u_{dc1}-u_{dc2}. As shown in Fig.17, the DC capacitors are charged with electricity to 360V on an even keel. The voltage difference u_{dc1}-u_{dc2} is initially 6V. Finally, the voltage difference u_{dc1}-u_{dc2} is regulated to fluctuate in a small range by the DC voltage control during the APF startup operation.

Fig.18 shows the experimental steady waveforms of the load current and the system supply current, where waveform 1 is the load current i_s and waveform 2 is the system supply current i_s through the APF filtering. The THD (total harmonic distortion) of the load current i_l is calculated to be 22.32%. The THD of i_s is 2.98%. Fig.18 proves that the proposed APF has good steady filtering capability. Fig.19 shows the experimental waveforms of the DC voltage and the neutral-point voltage difference during the steady operation, where waveform 1 is the DC voltage u_{dc} and waveform 2 is the voltage difference u_{dc1}-u_{dc2}. It can be seen from waveform 1 that the voltage of the DC capacitances is kept approximately invariable in the steady state. Waveform 2 shows that the ripple of the NP is restricted in a small range.

Fig.20 presents the dynamic experimental waveforms, where waveform 1 is the DC voltage and waveform 2 is the output current of the APF, when the nonlinear load is added abruptly. It is obvious that the DC voltage is controlled very steadily. Fig.20 proves that the proposed APF has a good dynamic response under the load adding process. The experimental waveforms of u_{AN} and u_{AB} are illustrated in Fig.21, where waveform 1 is u_{AN} and waveform 2 is u_{AB}. It is obvious that the output voltage u_{AN} furnished by each NPC inverter phase is three-level and that the line-line output voltage u_{AB} is five-level. Fig.21 shows that the proposed APF

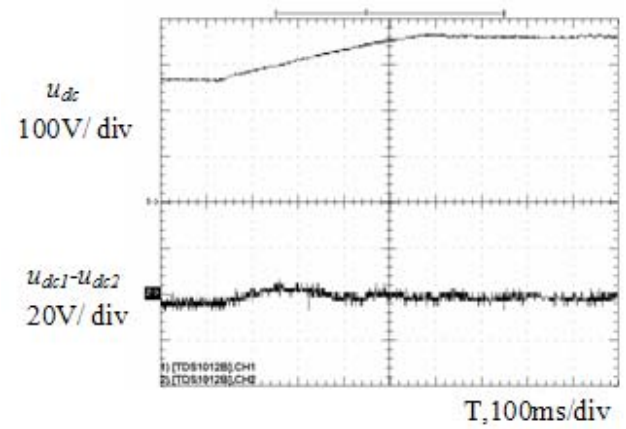

Fig. 17. Experimental startup waveform of DC voltage and neutral-point voltage difference.

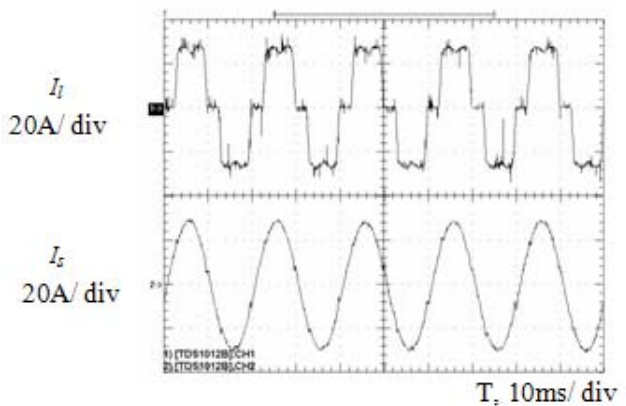

Fig. 18. Experimental steady waveforms of load current and system supply current.

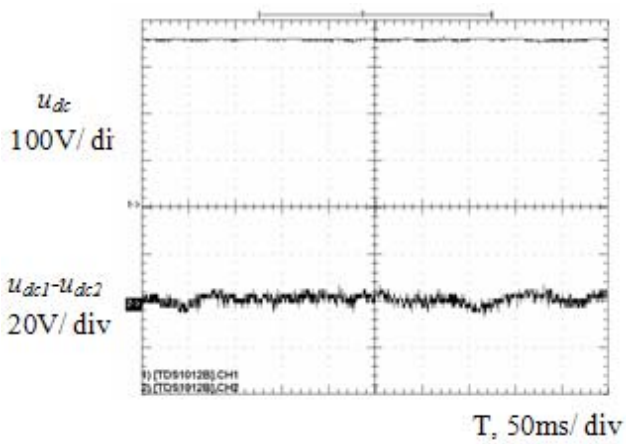

Fig. 19. Static experimental waveform of DC voltage and neutral-point voltage difference.

is fit for application in voltage grids ranging from 600V to 1000V.

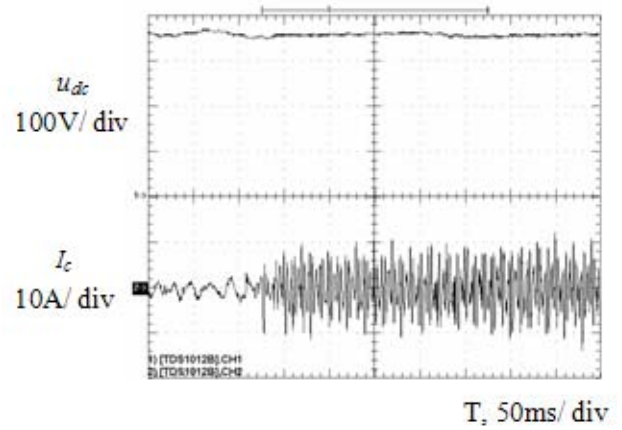

Fig. 20. Experimental dynamic waveform of DC voltage.

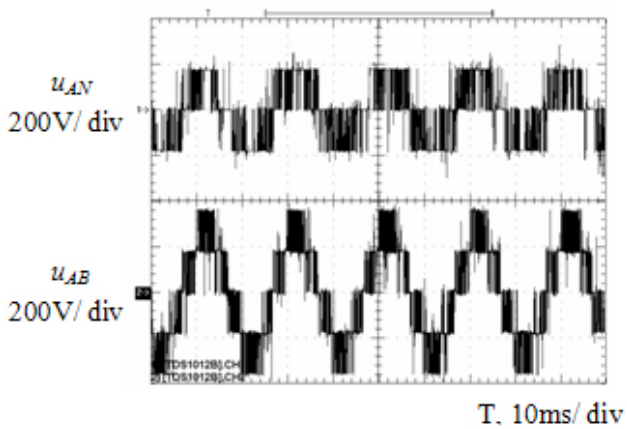

Fig. 21. Experimental waveforms of u_{AN} and u_{AB}.

V. CONCLUSIONS

This paper comprehensively analyzes the theoretical limitations of the neutral-point voltage balancing problem for three-level APFs tracking the harmonic currents of different frequencies and it draws a rule between the amplitude of the fluctuation in the NP voltage and the frequency of the harmonic currents. Then, this paper proposes a digital control algorithm for DC voltage. A PI controller regulates the DC voltage in the outer-loop controller. In the current-loop controller, this paper adopts a simple neutral-point voltage control method which requires knowledge of the current direction in each phase and the neutral-point voltage ripple direction. Based on that information, the small vectors that will move the neutral-point voltage in the direction opposite the direction of the unbalance are selected. The experimental results illustrate that the DC voltage can be controlled in a satisfactory way.

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REFERENCES

[1] D. Rivas, L. Moran, J. W. Dixon, J. Espinoza, "Improving passive filter compensation performance with active techniques," *IEEE Trans. Ind. Electron.*, Vol. 50, No. 1, pp. 161-170, 2003.

[2] S. Srianthumrong, H. Akagi, "A DC module for transient analysis of a series active filter integrated with a double-series diode rectifier," *IEEE Trans. Ind. Appl.*, Vol. 39 No. 3, pp. 864-873, May/Jun. 2003.

[3] T. Jin, K. M. Smedley, "Operation of one-cycle controlled three-phase active power filter with unbalanced source and load," *IEEE Trans. Power Electron.*, Vol. 21, No. 5, pp. 1403-1412, Sep. 2006.

[4] N. Akira, I. Takahashi, H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, Vol. 17, No. 3, pp. 518-523, Sep. 1981,

[5] J. Rodriguez, J. S. Lai , F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Appl.*, Vol. 49, No. 4, pp. 724-738, Aug. 2002.

[6] H. Akagi, "A transformerless hybrid active filter for integration into a medium-voltage motor drive with a passive front end," *Proceedings of the 2007 IEEE ICPE*, pp. 1-8, 2007.

[7] W. Tangtheerajaroonwong, T. Hatada, H. Akagi, "A transformerless hybrid active filter using a three-level diode-clamped pwm converter," *Proceedings of the 2007 IEEE PCC*, pp. 667-673, 2007.

[8] H. Akagi and R. Kondo, "A transformerless hybrid active filter using a three-level PWM converter for a medium-voltage motor drive," *Proceedings of the 2009 IEEE ECCE*, pp. 1732-1739, 2009.

[9] H. Akagi and T. Hatada, "Voltage balancing control for a three-level diode-clamped converter in a medium-voltage transformerless hybrid active filter," *IEEE Trans. Power Electron.*, Vol. 24, No. 3, pp. 571-579, Mar. 2009.

[10] H. Rudnick, J. Dixon, and L. Moran, "Delivering clean and pure power," *IEEE Power and Energy Magazine*, Vol. 1, No. 5, pp. 32-40, 2003.

[11] M. C. Wong, J. Tang, and Y. D. Han, "Cylindrical coordinate control of 3-D PWM technology in 3-phase 4-wire tri-level inverter," *IEEE Trans. Power Electron.*, Vol. 18 , No. 1, pp. 208 -220, 2003.

[12] N. Y. Dai, M. C. Wong, and Y. D. Han, "Application of a three-level NPC inverter as a three-phase four-wire power quality compensator by generalized 3DSVM.," *IEEE Trans. Power Electron.*, Vol. 21, No. 2, pp. 440-449, Mar. 2006.

[13] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "A multilevel converter-based universal power conditioner," *IEEE Trans. Ind. Appl.*, Vol. 36, No. 2, pp. 596-603, Mar./Apr. 2000.

[14] M. Postan and A. R. Beig, "A three phase active filter based on three level diode clamp inverter," *Proceedings of the 2008 IEEE POWERCON*, pp. 1-8, 2008.

[15] E. I. Gutierrez and J. L. Duran-Gomez, "Power quality improvement of a current-pulsed power supply based on a three-level NPC PWM VSI scheme as an active power filter[C]," *Proceedings of the 2006 IEEE IPEC*, 2006.

[16] M. Basu, S. P. Das, G. Dubey, "Parallel converter scheme for high-power active power filters[J]," *IEE Proceedings Electric Power Applications*，Vol. 151, No. 4, pp. 460-466, 2004.

[17] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kv transformerless statcom based on a five-level diode-clamped pwm converter: system design and experimentation of a 200-v 10-kva laboratory model," *IEEE Trans. Ind. Appl.*, Vol. 44, No. 2, pp. 672-680, Mar./Apr. 2008.

[18] N. Celanovic and D. Voroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, Vol. 15, No. 2, pp. 242-249, Mar. 2000.

[19] L. Lin, Y. P. Zou, Z. Wang, and J. Hongyuan, "Modeling and control of neutral-point voltage balancing problem in three-level NPC PWM Inverters," *Proceedings of the 2005 IEEE PESC*, pp. 861-866, 2005.

[20] C. J. Zhan, M. C. Wong, Y. Han, "Universal custom power conditioner(UCPC) in distribution networks," *Proceedings of the 1999 IEEE PEDS*, pp. 1025-1029, 1999.

[21] K. Zhang, Y. Kang, and J. Xiong, and C. Jian, "Control of PWM inverter with repetitive disturbance prediction," *Proceedings of the 1999 IEEE APEC*, pp. 1026-1031, 1999.

[22] S. G. Luo and Z. C. Hou, "An adaptive detecting method for harmonic and reactive currents," *IEEE Trans Industrial Electronics*, Vol. 42, No. 1, pp. 85-89, Feb. 1995.

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