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Placement Optimization of Power Components in Static Power Converters under Spatial and Thermal Constraints

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Abstract

This paper deals with an optimization approach of 3D space placement of power components under volume and thermal constraints. It consists in optimizing semiconductors positions on a heat sink by respecting the components junction temperatures and minimizing the heat sink size. The aim is to remove risks on the 3D converter components placement and ensure their effective integration before carrying out the first physical prototype. This approach is based on coupling an optimization environment with a thermal finite element simulation tool. A pre-sizing step using analytical models is performed to set the optimization computations coupled to numerical simulation.

Key words: *3D* placement, Optimization, Power components, Power converters

I. INTRODUCTION

Power static converters are increasingly used in many industrial application domains. In the transportation domain particularly, a strong need is expressed by manufacturers and equipment suppliers regarding design methodologies to facilitate the development of static converters considering multi-physic constraints. In this field, prototypes are expensive hence the need to reduce the development cost of these converters by removing the maximum of risks before carrying out the first physical prototype [1]-[6].

To meet these requirements several design methods have been developed. They can be classified into two main families.

The first one, more conventional, is based on the time domain or numerical simulation (direct method). It has the advantage to perform an accurate design but it can be very expensive in computation time especially when several design constraints have to be considered [7]-[10].

The second family suits more to multi-physic complex applications. It is based on a constrained optimization approach (indirect method). This method requires dedicated models to achieve compromise between accuracy and computation time [11]-[15].

From these two approach families an alternative design method of static converters based on a coupling between an optimization under multi-physic constraints procedure and numerical simulation have been emerged [16]-[19].

This paper is part of that way. It proposes a coupling design approach between constrained optimization and finite element simulation to optimize power components placement on a heat sink by respecting volume and thermal constraints. It allows to consider *3D* placement of semiconductors early in a design process to remove risks on their integration. This approach is set by a pre-sizing thermal step using analytical models to estimate semiconductors losses and their junction temperatures in order to preselect a convenient heat sink.

The developed approach is applied to a DC-DC boost converter including two semiconductors (a switch and a diode) to be placed on a heat sink with air cooling. To demonstrate the feasibility of the proposed approach on a complex application

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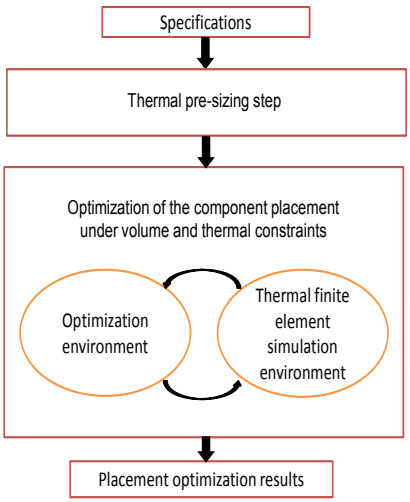

Fig. 1. Principle of the proposed power components placement approach.

including several semiconductors with water cooling heat sink, a three-phase inverter application is studied.

Firstly, the principle of the proposed optimization approach is presented. Then, analytical models related to the pre-sizing step as well as the placement optimization model under thermal and volume constraints are developed. Finally this approach is applied to a DC-DC boost converter and a three-phase inverter. For each converter, the impact of the geometric optimization parameters on the considered constraints and the optimized placement results are presented and discussed.

II. Principle of the Proposed Placement Optimization Approach

The principle of the proposed power components placement approach using an optimization procedure is given in Figure 1.

From specifications, a thermal pre-sizing is carried out. It consists in estimating the semiconductors losses and determining a convenient heat sink allowing to keep the semiconductors junction temperature under its maximal value specified by manufacturer. This step uses analytical models which are well suitable in a pre-sizing procedure allowing compromise between the accuracy and the computing time.

Considering the thermal pre-sizing results, the power components space placement is carried out using an optimization approach under volume and thermal constraints. The aim is to define the *3D* positions of the converter semiconductors on a heat sink while respecting the semiconductors maximal junction temperature and minimizing the heat sink volume.

This approach is based on a coupling between an optimization environment (Matlab/Simulink™) and a finite element simulation environment (Comsol™ multi-physics) to run an accurate finite element thermal model.

At the end of this approach, the optimized placement of the converter components is determined and the heat sink volume and the semiconductors junction temperatures are optimized and known with high accuracy.

III. Modeling

To achieve the proposed approach, analytical models are adopted in the pre-sizing step and finite element thermal model coupled to an optimization environment is developed to optimize the power components placement under volume and thermal constraints.

A. Modeling related to the thermal pre-sizing step

The pre-sizing step uses analytical models in order to estimate the semiconductors losses and their junction temperatures at a given heat sink.

1) Semiconductors losses analytical model: In our case, a fundamental switching cell including a MOSFET switch and a Schottky diode is considered. Conduction and switching losses in these semiconductors are calculated as follows:

- MOSFET :

$$P_{conduction(\tau_j)} = R_{s\_on}(\mathrm{T}_j)\cdot I_{s\_rms}^2 \quad (1)$$

$$P_{switching} = \frac{1}{2}\cdot V_{s\_\max}\cdot(\mathrm{T}_{on}+\mathrm{T}_{off})\cdot F_s \quad (2)$$

R_{s_on} is the switch dynamic resistance in the conduction state. This resistance depends on the semiconductor junction temperature.

I_{s_rms}, I_{s_max} and V_{s_max} are, respectively, the RMS current, the maximal current and the maximal voltage applied to the switch.

T_{on} and T_{off} are the switching times.

F_s is the switching frequency.

- Diode:

$$P_{conduction(\tau_j)} = R_{d\_on}\cdot I_{d\_rms}{}^2 + V_d(\mathrm{T}_j)\cdot I_{d\_m} \quad (3)$$

R_{d_on} is the diode dynamic resistance.

V_d is the diode voltage drop which depends on the diode junction temperature.

I_{d_rms} and I_{d_m} are the RMS and the mean diode currents.

Note that the switching losses in a Schottky diode are obviously neglected.

2) Thermal model: The switch and diode junction temperatures (T_{j_S} and T_{j_D}) can be estimated according to the modeling

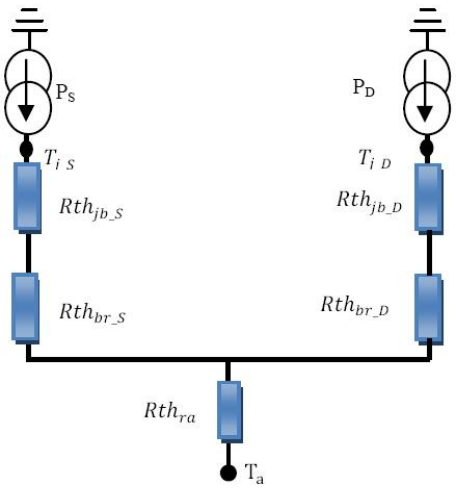

Fig. 2. Electrical equivalent circuit for electro-thermal modeling of switch, diode and heat sink.

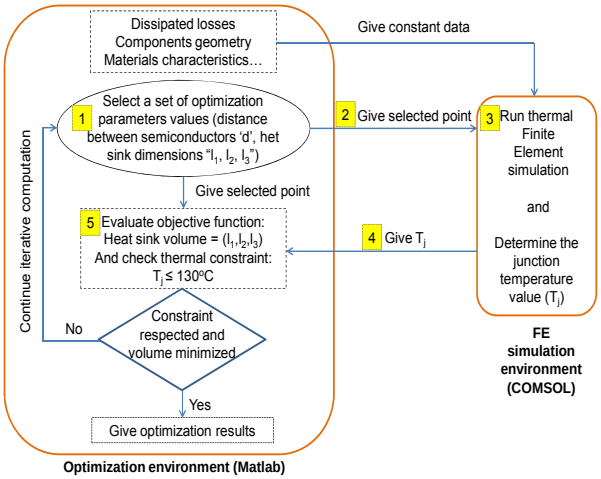

Fig. 3. Principle of the association between an optimization environment and a finite element simulation environment.

presented in figure 2 considering a shared heat sink. In this modeling, the total switch and diode losses (P_S and P_D) are considered as heating sources and the thermal exchanges between the semiconductor junction and its base, between the base and the heat sink and between the heat sink and the environment are modeled by thermal resistances (junction-base: Rth_{jb_S} and Rth_{jb_D}, base-heat sink: Rth_{br_S} and Rth_{br_D}, heat sink–air: Rth_{ra}).

Knowing the overall temperature T_a, the switch and diode junction temperatures are calculated from (4) and (5) respectively.

$$T_{j\_s} = T_a + (Rth_{jb\_s} + Rth_{br\_s}) \cdot P_{s(\tau_{js})} + Rth_{ra} \cdot [P_{s(\tau_{js})} + P_{D(\tau_{js})}] \quad (4)$$

$$T_{j\_o} = T_a + (Rth_{jb\_D} + Rth_{br\_D}) \cdot P_{D(\tau_{js})} + Rth_{ra} \cdot [P_{s(\tau_{js})} + P_{D(\tau_{js})}] \quad (5)$$

During the pre-sizing step, the junction-base and the base-heat sink thermal resistances are fixed (characterize semiconductors technologies). However, the heat sink–air resistance (Rth_{ra}) is calculated to ensure a junction temperature less than its maximal value specified by manufacturer (130°C in our case).

B. Modeling related to the 3D placement of semiconductors

Using results of the thermal pre-sizing step (semiconductors losses and pre-selected heat sink), the designer can optimize the *3D* placement of the active components on the heat sink by respecting a thermal constraint and by minimizing the heat sink size. To perform this optimization, an association between Matlab™ for the optimization method (genetic algorithm in our case) and Comsol™ for thermal finite element simulation is carried out.

Figure 3 shows the principle of this association.

As explained in figure 3, some constant data to supply finite element model (dissipated losses in semiconductors, active components dimensions, materials characteristics) are defined in the optimization environment.

The optimization principle associating the optimization environment and the finite element simulation tool can be summarized as follows:

First, a set of optimization parameters values is selected (step 1 in figure 3). The considered optimization parameters are the distance between semiconductors and the heat sink dimensions (length, width, height). In this paper only one heat sink dimension is taken into account (length or width).

Then selected set point is used in Comsol environment to run a finite element simulation (steps 2 and 3). This simulation allows determining the junction temperature of each semiconductor (step 4). The junction temperature is considered as the maximal obtained temperature on the semiconductor.

Knowing the optimization parameters values and the semiconductors junction temperatures, an evaluation of the objective function and a check of the thermal constraint are than done (step 5).

Steps (1 to 5) are repeated till minimizing the heat sink size and respecting the thermal constraint. At the end of the optimization process, the distance between semiconductors and the heat sink size, allowing respecting the thermal constraint and minimizing the heat sink volume, are determined.

Figure 4 shows the principle of a *3D* semiconductors placement on a heat sink modeled in Comsol environment.

In this case, each semiconductor is modeled by three layers (Silicon, substrate and sole). The Silicon one represents the

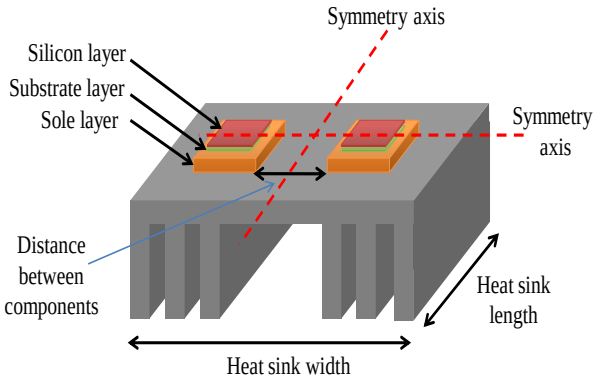

Fig. 4. Example of a 3D semiconductors placement on a heat sink.

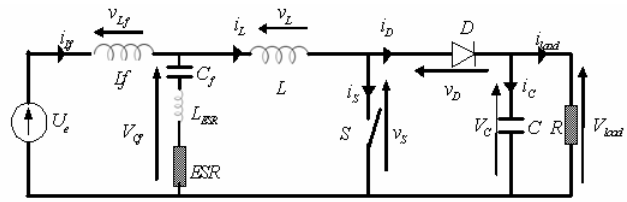

Fig. 5. DC-DC boost converter.

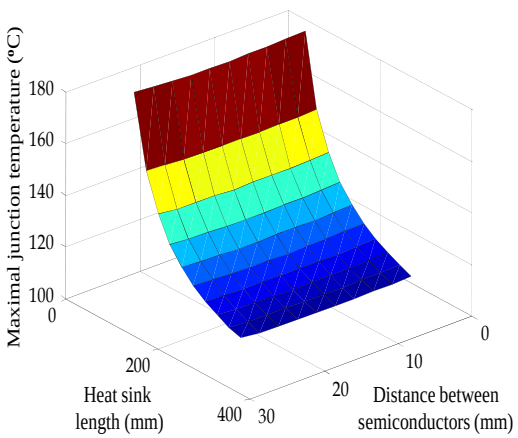

Fig. 6. Variations of the maximal junction temperature as a function of the optimization parameters.

heating source due to semiconductor losses. The substrate layer allows electrical insulation between the semiconductor and the heat sink. The sole layer represents the component packaging allowing to protect and to fix the semiconductor on the heat sink.

The optimized parameters are the distance between active components and the length of the heat sink. The objective function to be minimized is the heat exchange surface in order to minimize the heat sink volume. The constraint to be respected is the maximal semiconductors junction temperatures.

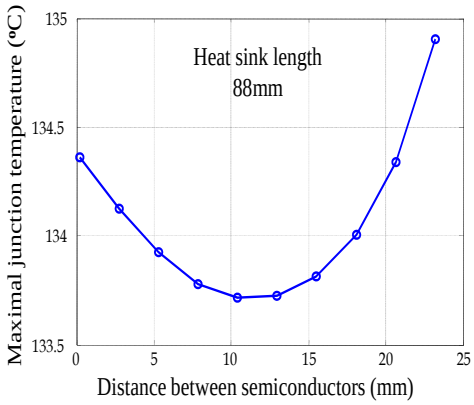

Fig. 7. Variations of the maximal junction temperature as a function of the distance between semiconductors (heat sink length 88 mm).

IV. Application of the Proposed Approach

The proposed optimization approach is applied to a DC-DC boost converter and to a three-phase inverter for electric vehicle application.

A. Application to a DC-DC boost converter

Figure 5 shows the considered boost converter as an example of a two semiconductors application with natural air cooling heat sink.

The converter power is 1kW. The dissipated losses are 26.4W in a MOSFET switch and 35.3W in a Schottky diode. The thermal resistances (sum of junction-base and base-heat sink resistances) are 1.5 °C/W for the switch and 1 °C/W for the diode. The considered ambient temperature is 30 °C.

The objective function to be minimized is the heat sink volume. In this case, the heat sink width and height are fixed. So the objective function is reduced to the heat sink length.

Therefore, the optimization parameters are the heat sink length and the distance between the semiconductors sole layers.

The optimization constraint is defined as follows:

$$T_j \leq 130°C$$

Where T_j is the maximal junction temperature of semiconductors (temperature of the Silicon layer).

Figures 6 and 7 show the variations of the maximal junction temperature as a function of the optimization parameters (the heat sink length and the distance between semiconductors).

As predicted, the maximal junction temperature decreases when the heat sink length increases. Moreover, at a given heat sink length, the maximal junction temperature increases when the two semiconductors are much close to each other as well as

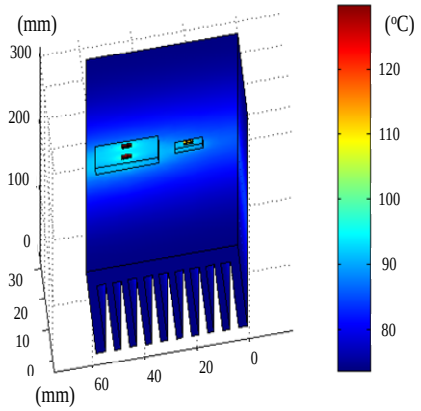

Fig. 8. Optimization of the semiconductors placement on the heat sink.

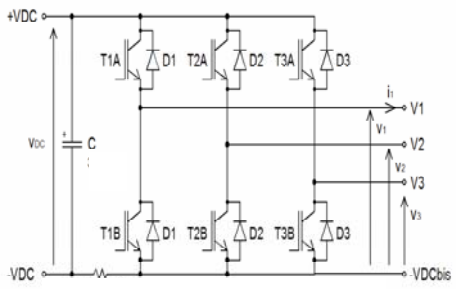

Fig. 9. Three-phase inverter architecture.

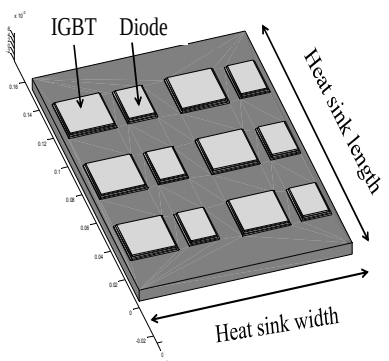

Fig. 10. Semiconductors placement on the thermal exchange layer of a heat sink.

when they reach the heat sink edge.

As a result, an optimum can be obtained on the heat sink length and the distance between power components while respecting the temperature constraint.

Note that in this case and according to figures 6 and 7, the heat sink length has a significant impact on the junction temperature compared to the effect of the distance between semiconductors.

Figure 8 shows the optimized placement of semiconductors on the heat sink obtained thanks to coupling Matlab™, as an optimization environment, to Comsol™ as a *3D* finite element simulation environment.

Remember that components are positioned on the heat sink according to two symmetry axis. This symmetry concerns the edges of semiconductors sole layers.

It's shown that semiconductors temperature constraint is respected (maximal junction temperature 129.8°C). The obtained minimal distance between the switch and the diode is 6.2 mm. The heat sink length is 320 mm and the optimized volume is 0.49 liter.

Note that the considered heat sink is selected from manufacturer database. In this case, the heat sink height and width are fixed. However these dimensions can be taken into account as optimization parameters too using the same principle of the proposed approach.

TABLE I

HEAT TRANSFER COEFFICIENT VALUES AS A FUNCTION OF THE WATER VELOCITY (Water cooling characteristics at 30°C : ρ =995.59 kg/m^3, μ = 8e-04 Pa.s, λ = 0.6133 W/m.°K, C_p = 4178 J/kg.°C, Pr = 5.453, L_c = 150 mm)

Flow velocity [m/s]	Reynolds number : Re	Nusselt number : Nu	Convective exchange coefficient
1	94581,05	498,83	4025,34
2	189162,1	868,51	7008,53
3	283743,15	1201,29	9693,93
4	378324,2	1512,16	12202,55
5	472905,25	1807,70	14587,43
6	567486,3	2091,56	16878,11
7	662067,35	2366,08	19093,31
8	756648,4	2632,83	21245,88
9	851229,45	2892,97	23345,15
10	945810,5	3147,39	25398,19

B. Application to an inverter

In this part, the proposed optimization approach is applied to a three-phase inverter used in an electric power train. The aim is to demonstrate the feasibility of the proposed method on a complex application including 12 semiconductors with water cooling heat sink.

Figure 9 shows the simplified architecture of the considered three-phase inverter.

The inverter power is 40 kW. The estimated semiconductors losses in the pre-sizing step are 350 W in each switch and 233 W in each diode which yields a converter efficiency of 91%.

Figure 10 shows an example of the semiconductors (IGBTs and diodes) placement on the thermal exchange layer of the heat sink.

Remember that IGBTs switches and diodes are modeled by three layers (Silicon, substrate and sole). The second one (substrate layer) allows electrical insulation between semiconductors and the heat sink.

The thermal exchange surfaces of the cooling heat sink are represented by an aluminum layer characterized by an equivalent convective exchange coefficient.

1) Calculation of the equivalent convective exchange coefficient : In order to simplify the finite element simulation, the cooling is modeled with an equivalent convective exchange coefficient. In this way, an average equivalent coefficient is calculated using equation 6 [20]:

$$\bar{h} = \frac{\overline{Nu} \cdot \lambda}{L_c} \qquad (6)$$

Where:

- λ : thermal conductivity of the fluid [W/m.°K]
- L_c : the heat sink characteristic length [m]
- $\overline{Nu}$: Nusselt number
  - In laminar flow (Re < 2400) :

$$\overline{Nu} = \frac{2}{3} \cdot Re^{0.5} \cdot Pr^{0.33}$$

  - In turbulent flow (Re >> 2400) :

$$\overline{Nu} = 0,0298 \cdot Re^{0.8} \cdot Pr^{0.33}$$

- $Re = \frac{\rho \cdot V_m \cdot L_C}{\mu}$: Reynolds number
- $Pr = \frac{\mu \cdot C_p}{\lambda}$: Prandtl number
- V_m : Flow velocity of the fluid [m/s]
- ρ : Density of the fluid [kg/m3]
- μ : dynamic viscosity [Pa.s]
- C_p : Specific heat of the fluid [J/kg.°C]

At a heat sink width of 76 mm (minimal needed width: sum of the widths of 2 IGBTs and 2 diodes), the corresponding Reynolds numbers have been calculated for the range flow velocity [1, 10 m/s]. Thus, we have noticed that the flow stills turbulent (Re>> 2400).

Table I shows the heat transfer coefficient values as a function of the water velocity (calculated in the case of a turbulent flow):

Knowing the convective exchange coefficient values, thermal finite element simulation can be done at a given flow velocity.

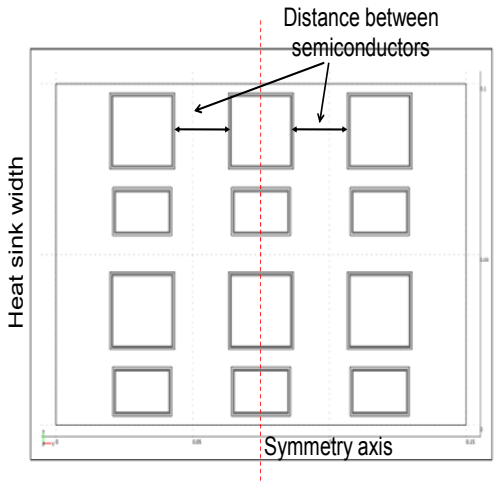

Fig.11. Placement of the inverter semiconductors on the heat sink.

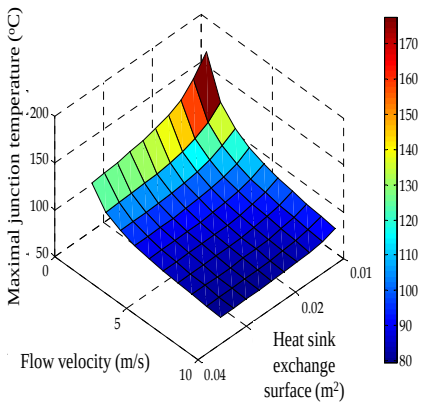

Fig. 12. Maximal junction temperature as a function of the flow velocity and the heat sink exchange surface (heat sink thickness: 4 mm, distance between semiconductors: 19 mm, ambient temperature: 30 ° C, heat sink length: 150 mm).

2) Influence of the flow velocity and the heat sink dimensions on the maximal junction temperature: Figure 11 shows the main considered geometric optimization parameters (distance between semiconductors and heat sink width).

During the optimization process, the semiconductors positioned on the symmetry axis are fixed and the other semiconductors are movable.

Figure 12 shows the influence of the flow velocity and the heat sink exchange surface on the maximal junction temperature.

As expected, the maximal junction temperature decreases when increasing the flow velocity and the heat exchange surface.

Figure 13 shows the maximal junction temperature versus the heat sink dimensions.

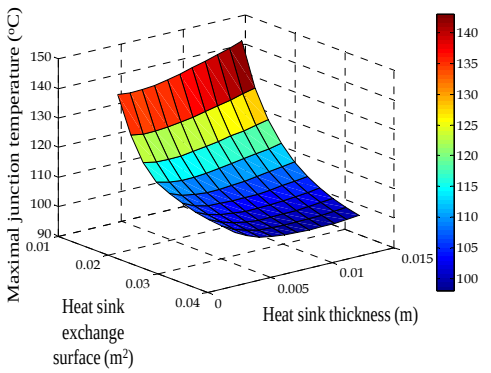

Fig. 13. Maximal junction temperature as a function of the heat sink thickness and exchange surface (flow velocity: 2 m/s, distance between semiconductors: 19 mm, ambient temperature: 30 ° C, heat sink length: 150 mm).

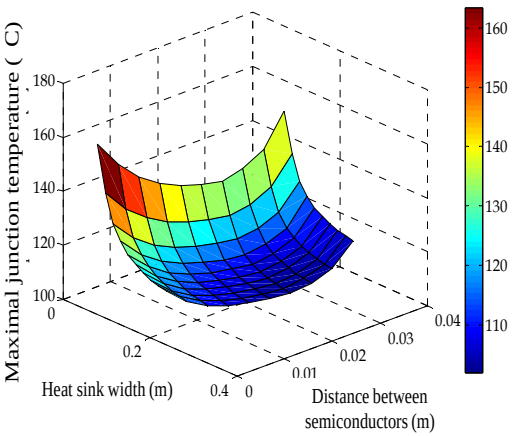

Fig. 14. Maximal junction temperature as a function of the distance between semiconductors and the heat sink width (flow velocity: 2 m/s, ambient temperature: 30 ° C, heat sink length: 150 mm, heat sink thickness: 4 mm).

For a given heat exchange surface, the maximal junction temperature increases when increasing the heat sink thickness. In fact, the convective heat exchange occurs through the lower surface of the cooling heat sink. However, the thermal resistance due to the vertical conduction exchange increases with increasing the heat sink thickness which increase the maximal junction temperature.

Figure 14 shows the evolution of the maximal temperature according to the distance between power components and the heat sink width.

The maximal junction temperature decreases when increasing the heat sink width and the distance between semiconductors. However this temperature increases when the components are much close to each other or when they reach the heat sink edge where the heat exchange is feeble.

3) Placement optimization results: The objective function to be minimized is the heat sink exchange surface. The considered constraint is the semiconductors junction temperatures (less or equal 130°C). During the optimization process, the flow velocity is fixed to 2 m/s. The heat sink length and thickness are fixed respectively to 150 mm and 4 mm. the optimization parameters are the distance between semiconductors and the heat sink width.

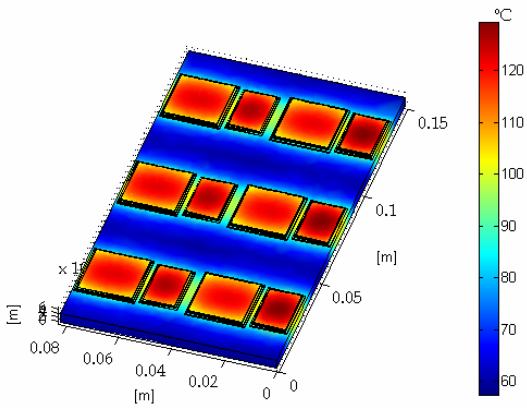

Fig. 15. Optimal placement of semiconductors on the heat sink.

To carry out this optimization, a genetic algorithm is used with 20 individuals and 20 generations [21], [22].

Figure 15 shows the components placement on the heat sink after optimization.

Note that the thermal constraint is respected (maximal junction temperature 129.5°C). Moreover, an optimal placement is determined while minimizing the heat exchange surface. The obtained heat sink width is 82 mm and the optimal distance between semiconductors is 26.2 mm.

Remember that the considered heat sink is selected from manufacturer database. In this inverter application, the heat sink thickness and length are fixed. These dimensions can be optimized in a generalized optimization approach. Moreover in our case, at a given length, the heat sink width has more significant impact on the components temperature than the impact of the distance between semiconductors through the width direction. However, in a generalized approach this distance can be considered as an optimization parameter too.

V. CONCLUSIONS

An automatic design approach to optimize the *3D* placement of semiconductors on a heat sink is presented in this paper. This approach is based on an optimization procedure under volume and thermal constraints. The aim is to remove risks on the *3D* converter components placement before carrying out the first physical prototype.

To perform this approach, a coupling between an optimization environment and a thermal finite element simulation tool is proposed.

The application of this approach to a three-phase inverter has shown the feasibility to optimize the placement of several components on a heat sink under semiconductors junction temperature and heat sink size.

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