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# Implementation of an Interleaved AC/DC Converter with a High Power Factor

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## Abstract

An interleaved bridgeless buck-boost AC/DC converter is presented in this paper to achieve the characteristics of low conduction loss, a high power factor and low harmonic and ripple currents. There are only two power semiconductors in the line current path instead of the three power semiconductors in a conventional boost AC/DC converter. A buck-boost converter operated in the boundary conduction mode (BCM) is adopted to control the active switches to achieve the following characteristics: no diode reverse recovery problem, zero current switching (ZCS) turn-off of the rectifier diodes, ZCS turn-on of the power switches, and a low DC bus voltage to reduce the voltage stress of the MOSFETs in the second DC/DC converter. Interleaved pulse-width modulation (PWM) is used to control the switches such that the input and output ripple currents are reduced such that the output capacitance can be reduced. The voltage doubler topology is adopted to double the output voltage in order to extend the useable energy of the capacitor when the line voltage is off. The circuit configuration, principle operation, system analysis, and a design example are discussed and presented in detail. Finally, experiments on a 500W prototype are provided to demonstrate the performance of the proposed converter.

**Key words:** AC-DC Converter, Harmonic, Power Factor Correction, , PWM, THD

## I. INTRODUCTION

To mitigate the climate change and environmental pollution resulting from the greenhouse gas emissions from fossil-fuel-based power generation, the Environmental Protection Agency (EPA) and the Climate Savers Computing Initiative (CCSI) have proposed efficiency requirements for modern power supply units. In order to meet the EN-61000-3-2 class D limit, power factor correction (PFC) is a solution to improve input the power factor and to reduce the amount of harmonic current when the power level of a switching mode power supply (SMPS) is more than 75W. The most popular type of PFC technology is based on a front-end diode bridge rectifier followed by a boost converter. References [1]-[9] propose different circuit technologies to improve circuit performance with a high power factor and a low harmonic current. However, the input current flows through at least three power semiconductors including two power diodes and at least one power switch such that the conduction losses on the power semiconductors become a serious problem when a high efficiency SMPS is demanded in modern power converters. A variety of the bridgeless PFC circuits have been proposed in [10]-[18] to allow the power to flow through only two power semiconductors in the line current path. Thus the conduction losses are reduced when compared to a conventional boost PFC converter.

An interleaved bridgeless buck-boost PFC converter with voltage doubler output is presented to increase the input power factor and to reduce the total current harmonic in order to meet the EN-61000-3-2 class D limits. There are two circuit modules in the proposed converter to achieve current sharing, partial ripple current reduction and to reduce the capacitances at the input and output sides due to the interleaved PWM operation. In each circuit module, the two buck-boost converters are connected to an AC source to achieve voltage doubler output. Each buck-boost converter conducts during one-half of the line voltage. One diode is connected in series with the buck-boost converter to conduct the line current with a unidirectional power flow. In each half cycle of the line voltage, there is only one diode conduction loss with the proposed circuit instead of the two diode conduction losses with a conventional boost PFC converter. Boundary conduction mode (BCM) operation is adopted to control the active switches such that the active switches are turned on under ZCS and the fast recovery diodes are turned off under ZCS. The AC line current can automatically follow

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the mains voltage with a high power factor. Experiments, conducted with a 500W laboratory prototype, are presented to demonstrate the circuit performance.

## II. CIRCUIT CONFIGURATION

Fig. 1 gives the circuit configuration of the proposed converter. There are two circuit modules in the adopted converter. These two circuit modules are operated with the interleaved PWM scheme to reduce the ripple currents at the input and output sides. For each circuit module, two buck-boost converters are connected back-to-back to achieve voltage doubler output. Each buck-boost converter operates during one-half of the line voltage cycle. In the positive half cycle of the line voltage ($v_s$>0). $D_{p1}$, $S_{p1}$, $L_{p1}$, $C_p$ and $D_{p2}$ in circuit module 1 and $D_{p3}$, $S_{p2}$, $L_{p2}$, $C_p$ and $D_{p4}$ in circuit module 2 are operated as buck-boost converters and the voltage $V_p$ across the capacitor $C_p$ is regulated by pulse-width modulation (PWM) of the active switches $S_{p1}$ and $S_{p2}$. $D_{n1}$, $S_{n1}$, $L_{n1}$, $C_n$ and $D_{n2}$ in circuit module 1 and $D_{n3}$, $S_{n2}$, $L_{n2}$, $C_n$ and $D_{n4}$ in circuit module 2 are operated in the negative half cycle of the line voltage ($v_s$<0). The voltage $V_n$ across the capacitor $C_n$ is controlled by the PWM of the active switches $S_{n1}$ and $S_{n2}$. In a conventional boost PFC converter, there are two conduction losses in the diode bridge rectifier. However, there is only one diode conduction loss in the proposed converter during the conduction of an active switch. Since the active switches $S_{p1}$, $S_{p2}$, $S_{n1}$ and $S_{n2}$ are connected between the input and output sides, the input inrush current during start-up can be controlled by the four active switches. Thus the inrush current control capability in the adopted circuit is better than that achieved with a conventional boost PFC converter. BCM operation is adopted to control the active switches such that the line current is a sinusoidal waveform with a high power factor and low current harmonics. All of the power switches are turned on under ZCS and the rectifier diodes are turned off under ZCS. Based on the above discussion, the proposed converter has less conduction and switching losses on the power semiconductors.

## III. OPERATION PRINCIPLE

Before the system analysis, it is assumed that $C_p$=$C_n$, $L_{p1}$=$L_{p2}$=$L_{n1}$=$L_{n2}$=$L$ and $V_p$=$V_n$=$V_o$/2. All of the power semiconductors in the proposed converter are ideal. Figs. 2 and 3 show the proposed circuit operated during the positive and negative half cycles of the line voltage. Inductors $L_{p1}$, $L_{p2}$, $L_{n1}$ and $L_{n2}$ are operated in the BCM mode.

### *A. Positive Half Cycle of the Line Voltage ($v_s$>0)*

$D_{p1}$ and $S_{p1}$ in circuit 1 and $D_{p3}$ and $S_{p2}$ in circuit 2 are connected in series to achieve a unidirectional power flow. $L_{p1}$ and $L_{p2}$ are the filter inductors, $D_{p2}$ and $D_{p4}$ are the

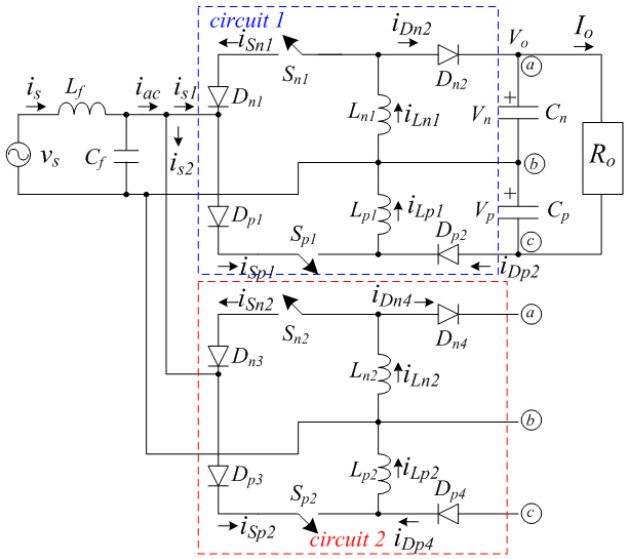


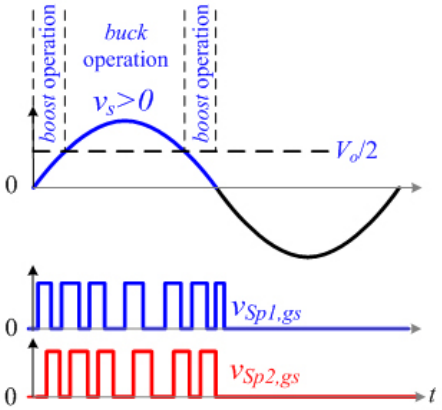

Fig. 1. Circuit configuration of the proposed converter.

freewheeling diodes, and $C_p$ is an output capacitor. During the positive line voltage, the switches $S_{p1}$ and $S_{p2}$ are controlled with PWM operation and the switches $S_{n1}$ and $S_{n2}$ are in the off state. The key waveforms of the proposed converter in the positive half cycle of the line voltage are illustrated in Figs. 2(a)~2(c). The capacitor voltage $V_p$ is regulated by the PWM of the switches $S_{p1}$ and $S_{p2}$. When the line voltage $v_s$ is less than the capacitor voltage $V_p$ (or $V_o$/2), the converter is operated in the boost operation. Thus the duty cycle of the switches $S_{p1}$ and $S_{p2}$ is greater than 0.5. Fig. 2(b) gives the key waveforms of the proposed converter for the positive line voltage and $v_s$<$V_o$/2 case. Since the PWM signals of the switches $S_{p1}$ and $S_{p2}$ are phase-shifted one-half of a switching period, there are four operation modes, mode 4 → mode 1 → mode 4 → mode 3, in the positive line voltage and $v_s$<$V_o$/2 during one switching period. On the other hand, the converter is operated in the buck operation when $v_s$>$V_o$/2. The duty cycle of the switches $S_{p1}$ and $S_{p2}$ is less than 0.5. Fig. 2(c) gives the key waveforms of the proposed converter for the positive line voltage and $v_s$>$V_o$/2 case. Similarly four operation modes, mode 1 → mode 2 → mode 3 → mode 2, can be found at $v_s$>0 and $v_s$>$V_o$/2 during one switching period. The four operation modes are discussed in the following.

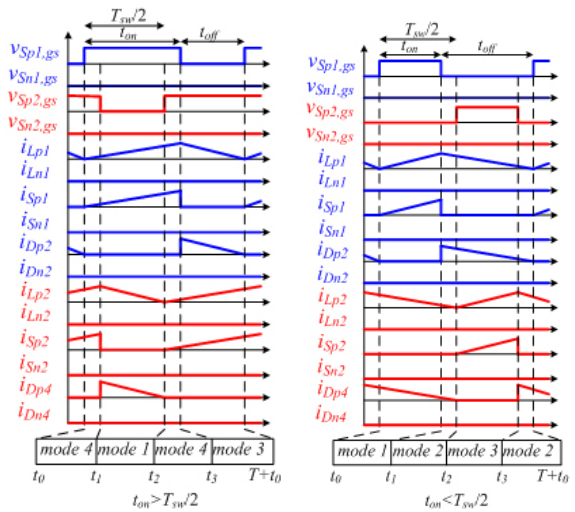
***Mode 1*** [*$S_{p1}$, $D_{p1}$, $D_{p4}$: ON; Fig. 2(d)*]: In this mode, only the switch $S_{p1}$ is in the on state. Since $v_s$>0, the inductor voltages $v_{Lp1}$=$v_s$ and $v_{Lp2}$=-$V_p$. Thus the inductor current $i_{Lp1}$ increases with the slope of $v_s$/$L_{p1}$ and $i_{Lp2}$ decreases with the slope of -$V_p$/$L_{p2}$ in this mode. There are two possible ways to end this mode. First, the switch $S_{p1}$ is turned off to end this mode. Then the operation of the converter goes to mode 2 as shown in Fig. 2(c). Second, this mode can be ended when the inductor current $i_{Lp2}$ decreases to zero such that the switch $S_{p2}$ can be turned on under ZCS and the diode $D_{p4}$ can be turned off under ZCS. Therefore there is no reverse recovery problem on the diode $D_{p4}$. Then the operation of the converter

goes to mode 4 as shown in Fig. 2(b).

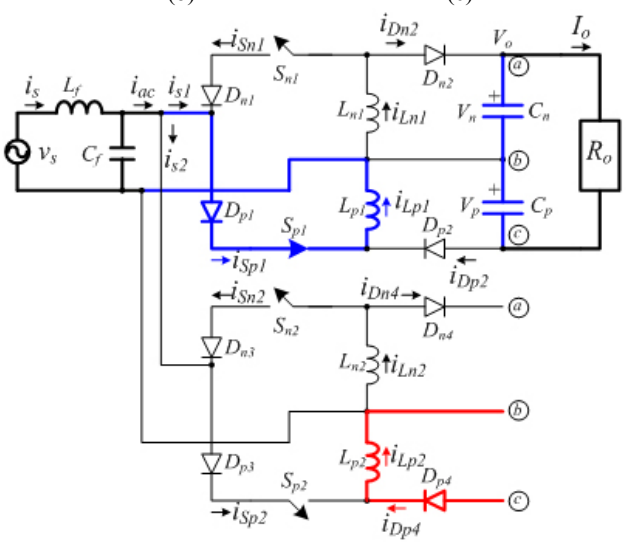
***Mode 2*** [$D_{p2}$, $D_{p4}$*: ON; Fig. 2(e)*]: In this mode, all of the active switches are in the off state. Since $i_{Lp1}$ and $i_{Lp2}$ are all positive, the freewheeling diodes $D_{p2}$ and $D_{p4}$ are conducting. The energy stored in the inductors $L_{p1}$ and $L_{p2}$ is released to the output capacitor $C_p$. The inductor voltages $v_{Lp1}$=$v_{Lp2}$=-$V_p$




(a)




(b) (c)



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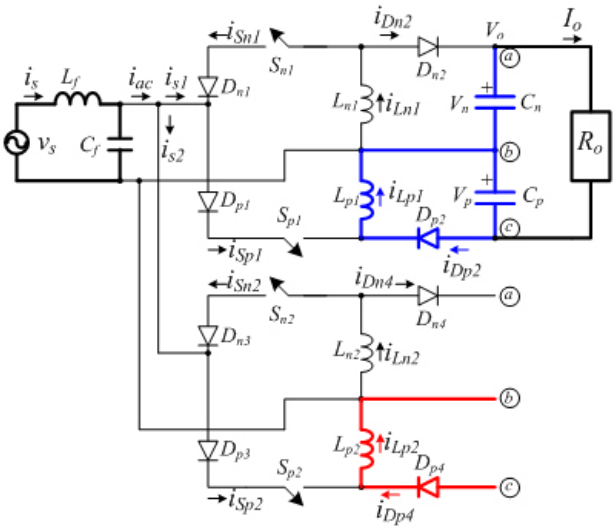

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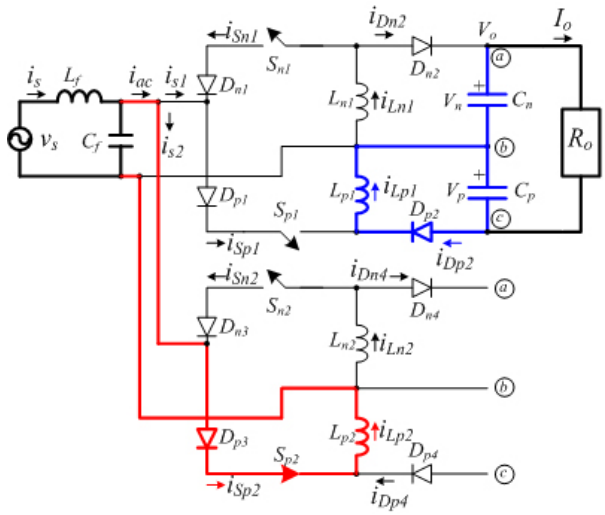

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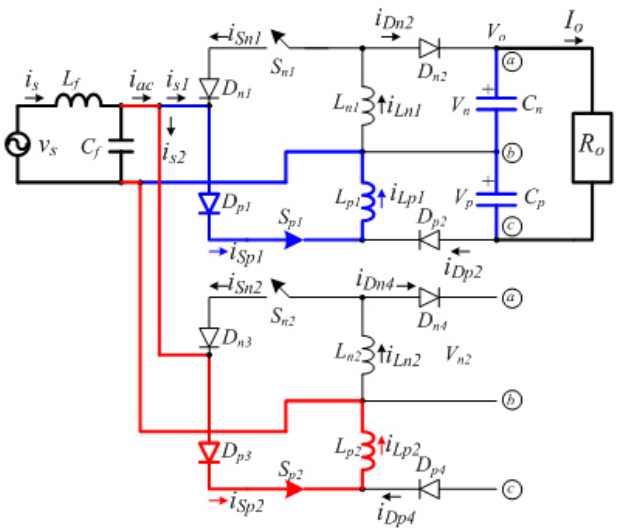


(g)

Fig. 2. Operation of the proposed converter during the positive half cycle of line voltage (a) line voltage and switch PWM signals (b) key waveforms of boost operation ($t_{on}$>$T_{sw}$/2) (c) key waveforms of buck operation ($t_{on}$<$T_{sw}$/2) (d) mode 1 (e) mode 2 (f) mode 3 (g) mode 4.

and the inductor currents $i_{Lp1}$ and $i_{Lp2}$ decrease with the rate of $-V_p/L_{p1}$. The inductor current $i_{Lp2}$ is decreased to zero at the end of this mode. Then the operation of the adopted circuit goes to mode 3 as shown in Fig. 2(c). Thus the diode $D_{p4}$ is turned off under ZCS and the switch $S_{p2}$ is turned on under ZCS.

***Mode 3*** [$S_{p2}$, $D_{p2}$, $D_{p3}$: *ON; Fig. 2(f)*]: In this mode, only the switch $S_{p2}$ is on. Since $v_s>0$, the inductor voltages $v_{Lp2}=v_s$ and $v_{Lp1}=-V_p$ such that the inductor current $i_{Lp2}$ increases with the slope of $v_s/L_{p2}$ and $i_{Lp1}$ decreases with the slope of $-V_p/L_{p1}$. There are two possible ways to end this mode. If the adopted converter is operated under boost operation ($v_s<V_o/2$), then this mode ends at $i_{Lp1}=0$. Then the operation of the proposed converter goes to mode 4 as shown in Fig. 2(b). Then the switch $S_{p1}$ is turned on under ZCS and the diode $D_{p2}$ is turned off under ZCS. If the adopted converter is operated under buck operation ($v_s>V_o/2$), then this mode ends when the switch $S_{p2}$ is turned off. Then the operation of the proposed converter goes to mode 2 as shown in Fig. 2(c).

***Mode 4*** [$S_{p1}$, $S_{p2}$, $D_{p1}$, $D_{p3}$: *ON; Fig. 2(g)*]: In this mode, the active switches $S_{p1}$ and $S_{p2}$ are on. This mode is only operated when $v_s>0$ and $v_s<V_o/2$. The inductor voltages $v_{Lp1}=v_{Lp2}=v_s>0$ such that the inductor currents $i_{Lp1}$ and $i_{Lp2}$ both increase with the slope of $v_s/L_{p1}$. The input energy is stored in the inductors $L_{p1}$ and $L_{p2}$ in this mode. There are two ways to end this mode. First this mode can be ended when the switch $S_{p1}$ is turned off. Then the operation of the proposed converter goes to mode 3 as shown in Fig. 2(b). Second, this mode can be ended when the switch $S_{p2}$ is turned off. Then the operation of the proposed converter goes to mode 1 as shown in Fig. 2(b).

*B. Negative Half Cycle of Line Voltage* ($v_s<0$)

During the negative half cycle of the line voltage, the switches $S_{n1}$ and $S_{n2}$ are controlled with PWM operation and the switches $S_{p1}$ and $S_{p2}$ are off. The key waveforms of the proposed converter during the negative line voltage are shown in Figs. 3(a)~3(c). The voltage $V_n$ is regulated by the PWM of the switches $S_{n1}$ and $S_{n2}$. When $v_s>-V_n$ (or $-V_o/2$), the converter is operated in the boost operation. Thus the duty cycles of the switches $S_{n1}$ and $S_{n2}$ are greater than 0.5. The key waveforms of the proposed converter at $v_s<0$ and $v_s>-V_o/2$ are shown in Fig. 3(b). In the boost operation, there are four operation modes, mode 4 → mode 1 → mode 4 → mode 3, during one switching period. If the proposed converter is operated in the buck operation, Fig. 3(c) gives the key waveforms of the proposed converter at $v_s<0$ and $v_s<-V_o/2$. Similarly there are another four operation modes, mode 1 → mode 2 → mode 3 → mode 2, in the buck operation during one switching period. These four operation modes are discussed in the following.

***Mode 1*** [$S_{n1}$, $D_{n1}$, $D_{n4}$: *ON; Fig. 3(d)*]: In this mode, only the switch $S_{n1}$ is on. Since $v_s<0$, the inductor voltages $v_{Ln1}=-v_s$ and $v_{Ln2}=-V_n$ such that the inductor current $i_{Ln1}$ increases with the slope of $-v_s/L_{n1}$ and $i_{Ln2}$ decreases with the slope of $-V_n/L_{p2}$. There are two ways to end this mode. If the buck-boost converter is operated under boost operation ($v_s>-V_o/2$), then this mode ends when $i_{Ln2}$ is decreased to zero. Then the operation of the proposed converter goes to mode 4 as shown in Fig. 3(b). Then the switch $S_{n2}$ is turned on under ZCS at this moment and the diode $D_{n4}$ is turned off under ZCS. Therefore there is no reverse recovery problem on the diode $D_{n4}$. If the adopted converter is operated under buck operation ($v_s<-V_o/2$), then this mode ends when the switch $S_{n1}$ is turned off. Then the operation of the proposed converter goes to mode 2 as shown in Fig. 3(c).

***Mode 2*** [$D_{n2}$, $D_{n4}$: *ON; Fig. 3(e)*]: In this mode, all of the power switches are off. This mode is only operated in the buck operation ($v_s<-V_o/2$). Since $i_{Ln1}$ and $i_{Ln2}$ are positive, the freewheeling diodes $D_{n2}$ and $D_{n4}$ are conducting. The energy stored in $L_{n1}$ and $L_{n2}$ is released to charge the capacitor $C_n$. Since $v_{Ln1}=v_{Ln2}=-V_n$, the inductor currents $i_{Ln1}$ and $i_{Ln2}$ decrease at a rate of $-V_n/L_{n1}$. This mode ends when $i_{Ln2}$ is decreased to zero. Then the operation of the adopted circuit goes to mode 3 as shown in Fig. 3(c). Thus the diode $D_{n4}$ is turned off under ZCS and the switch $S_{n2}$ is turned on under ZCS.

***Mode 3*** [$S_{n2}$, $D_{n2}$, $D_{n3}$: *ON; Fig. 3(f)*]: In this mode, only the switch $S_{n2}$ is in the on state. Since $v_{Ln1}=-V_n$ and $v_{Ln2}=-v_s$ the inductor current $i_{Ln1}$ decreases with the slope of $-V_n/L_{n1}$ and $i_{Ln2}$ increases with the slope of $-v_s/L_{n2}$. If the adopted converter is operated under boost operation ($v_s>-V_o/2$), then this mode ends at $i_{Ln1}=0$. Then the operation of the proposed converter goes to mode 4 as shown in Fig. 3(b). Then the switch $S_{n1}$ is turned on under ZCS and the diode $D_{n2}$ is turned off under ZCS. If the adopted converter is operated under buck operation ($v_s<-V_o/2$), then this mode ends when switch $S_{n2}$ is turned off. Then the operation of the proposed converter goes to mode 2 as shown in Fig. 3(c).

***Mode 4*** [$S_{n1}$, $S_{n2}$, $D_{n1}$, $D_{n3}$: *ON; Fig. 3(g)*]: In this mode, the active switches $S_{n1}$ and $S_{n2}$ are both turned on. This mode is only operated when $0>v_s>-V_o/2$. The inductor voltages $v_{Ln1}=v_{Ln2}=-v_s>0$ such that $i_{Ln1}$ and $i_{Ln2}$ both increase with the slope of $-v_s/L_{p1}$. The input energy is stored in $L_{n1}$ and $L_{n2}$ in this mode. There are two possible ways to end this mode. If the switch $S_{n1}$ is turned off, then the operation of the proposed converter goes to mode 3 as shown in Fig. 3(b). If the switch $S_{n2}$ is turned off, then the operation of the proposed converter goes to mode 1 as shown in Fig. 3(b).

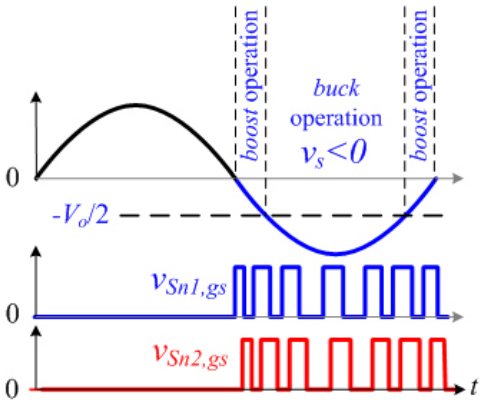
## IV. SYSTEM CHARACTERISTICS

The theoretical waveforms of the gating signal, the switch current and the diode current during the positive and negative line voltages are shown in Figs. 2 and 3. Interleaved BCM operation with a constant turn-on time, such as that made possible by UCC28061, FAN9612 and NCP1631, is used to control the active switches. The turn-on time of the active switches is constant and the turn-off time is variable. Thus all of the active switches are turned on under ZCS and the diodes $D_{p2}$, $D_{p4}$, $D_{n2}$ and $D_{n4}$ are turned off under ZCS. There are only two power semiconductors (one diode and one power switch) in the line current path instead of the three power semiconductors in a conventional boost PFC converter. Thus the adopted converter has less conduction losses and low switching losses. The interleaved PWM scheme is used to reduce the ripple currents at the input and output sides. From

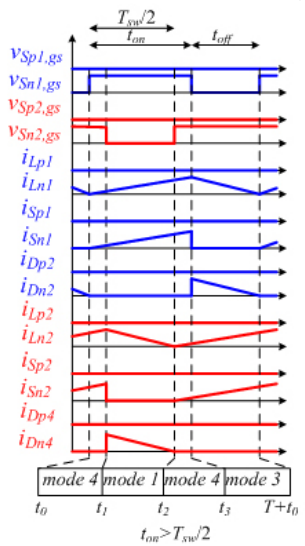
the power balance between the input and output sides, the maximum root mean square line current $I_{s,max}$ is expressed as:

$$I_{s,\max} = P_o / \eta V_{s,\min} \quad (1)$$

where $\eta$ is the circuit efficiency and $V_{s,min}$ is the minimum root mean square line voltage. If the operating switching frequency $f_{sw}$ is much higher than the line frequency $f_{line}$, the




(a)

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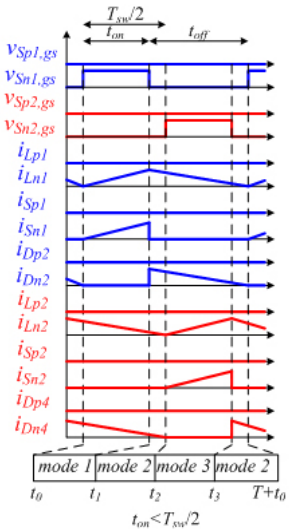


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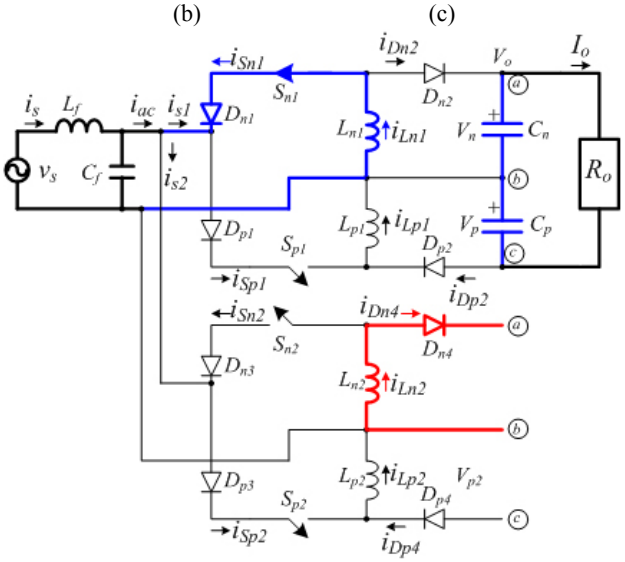


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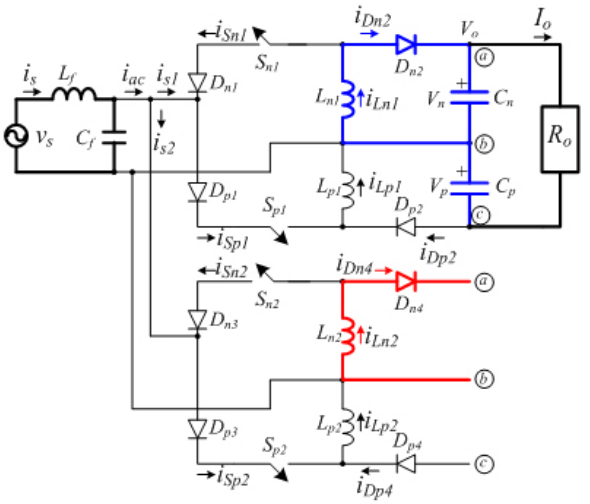


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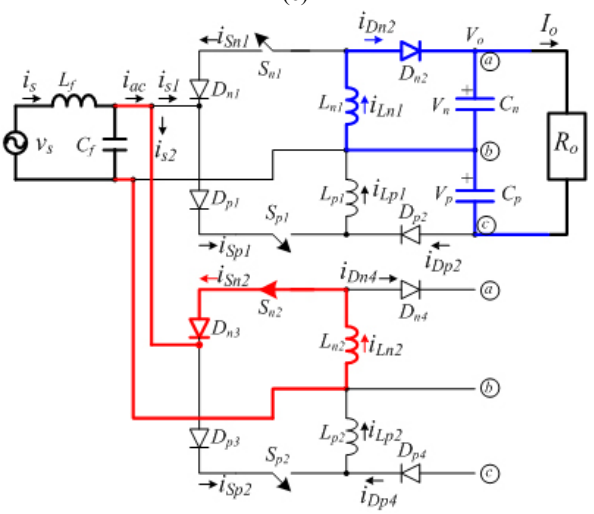


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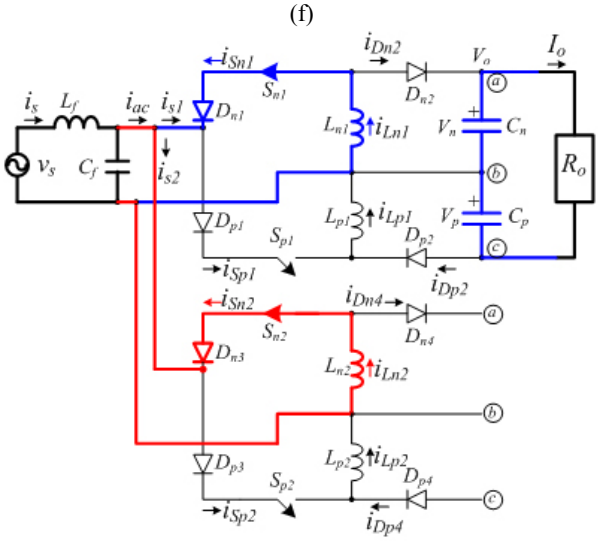


(g)

Fig. 3. Operation of the proposed converter during the negative half cycle of line voltage (a) line voltage and switch PWM signals (b) key waveforms of boost operation ($t_{on}$>$T_{sw}$/2) (c) key waveforms of buck operation ($t_{on}$<$T_{sw}$/2) (d) mode 1 (e) mode 2 (f) mode 3 (g) mode 4.

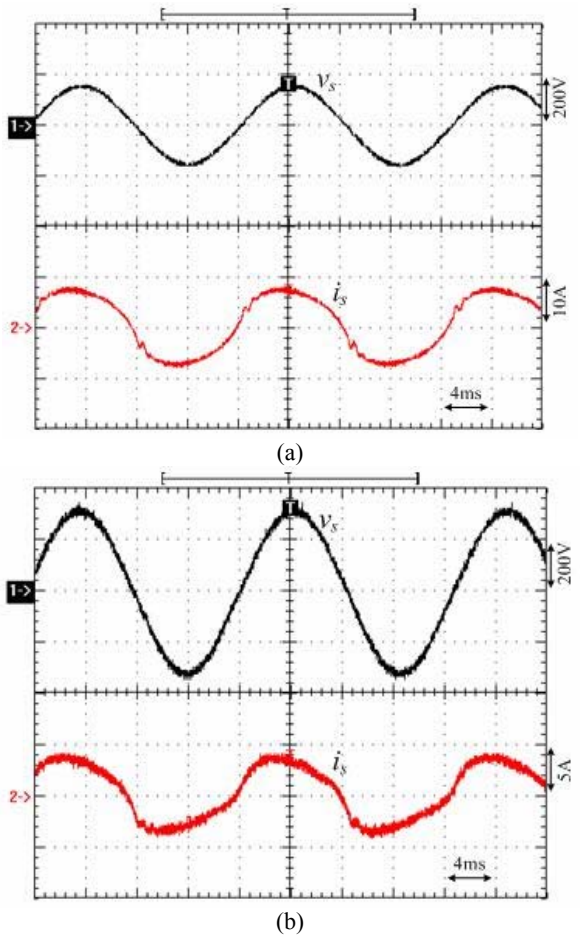


Fig. 4. Measured AC source voltage $v_s$ and line current $i_s$ at full load and (a) low line voltage ($v_s$=110 $V_{rms}$) (b) high line voltage ($v_s$=220 $V_{rms}$).

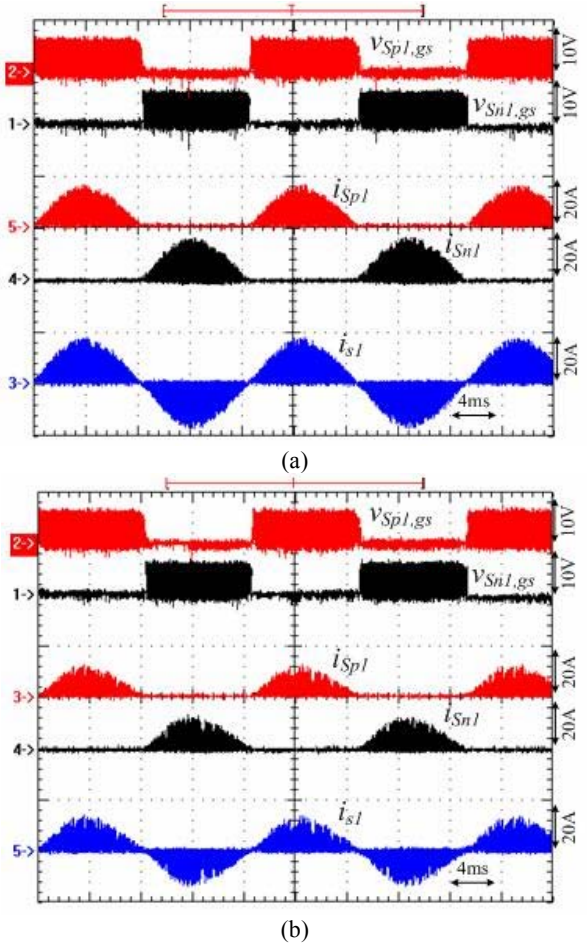


Fig. 5. Measured switch signals, $v_{Sp1,gs}$ and $v_{Sn1,gs}$, switch currents, $i_{Sp1}$ and $i_{Sn1}$, and input current $i_{s1}$ of circuit module 1 at full load and (a) low line voltage ($v_s$=110 $V_{rms}$) (b) high line voltage ($v_s$=220 $V_{rms}$).

line current can be considered as a constant value during one switching period. Since the turn-on time of the active switches is related to the peak inductor current, the switching frequency is variable. The minimum switching frequency $f_{sw,min}$ occurs at the peak value of the minimum line voltage. It is assumed that two circuit modules supply one-half of the rated power to the output load. From Fig. 3, the peak of the inductor currents $i_{Lp1,max,pk}$ and $i_{Lp2,max,pk}$ are given as:

$$i_{Lp1,\max,pk} = i_{Lp2,\max,pk} = \sqrt{2}I_{s,\max}/\delta' = \sqrt{2}V_{s,\min}t_{on}/L \quad (2)$$

where $L_{p1}$=$L_{p2}$=$L$, $\delta$' is the duty ratio of $S_{p1}$ and $S_{p2}$ at the peak value of the line voltage, and $t_{on}$ is the turn-on time of the switches $S_{p1}$ and $S_{p2}$. Thus the turn-on time $t_{on}$ can be expressed as:

$$t_{on} = Li_{Lp1,\max,pk}/\sqrt{2}V_{s,\min} = LI_{s,\max}/(\delta' V_{s,\min}) \quad (3)$$

The turn-off time of the active switches can be obtained by the output capacitor voltage and the peak inductor current.

$$t_{off} = \frac{2\sqrt{2}LI_{s,\max}\sin\omega t}{\delta' V_o} \quad (4)$$

The switching period $T_{sw}$ is obtained from (1), (3) and (4).

$$\begin{aligned} T_{sw} = t_{on}+t_{off} &= \frac{LI_{s,\max}}{\delta' V_{s,\min}} + \frac{2\sqrt{2}LI_{s,\max}\sin\omega t}{\delta' V_o} \\ &= \frac{LV_oI_o}{\delta'\eta V_{s,\min}^2}\left(1+\frac{2\sqrt{2}V_{s,\min}\sin\omega t}{V_o}\right) \end{aligned} \quad (5)$$

From (5), the maximum switching period $T_{sw,max}$ at the peak value of low the line voltage is derived as:

$$T_{sw,\max} = \frac{LV_oI_o}{\delta'\eta V_{s,\min}^2}\left(1+\frac{2\sqrt{2}V_{s,\min}}{V_o}\right) \quad (6)$$

If the minimum switching frequency is selected, the inductances of $L_{p1}$~$L_{n2}$ can obtained from (7).

$$L = L_{p1} = L_{p2} = L_{n1} = L_{n2} = \frac{\delta'\eta V_{s,\min}^2}{f_{sw,\min}I_o(V_o+2\sqrt{2}V_{s,\min})} \quad (7)$$

The voltage stress of the active switches is expressed as:

$$\begin{aligned} &v_{Sp1,stress} = v_{Sp2,stress} = v_{Sn1,stress} = v_{Sn2,stress} \\ &= \sqrt{2}V_{s,\max} + (V_o/2) \end{aligned} \quad (8)$$

The maximum reverse voltages of the diodes $D_{p1}$~$D_{n4}$ are given as:

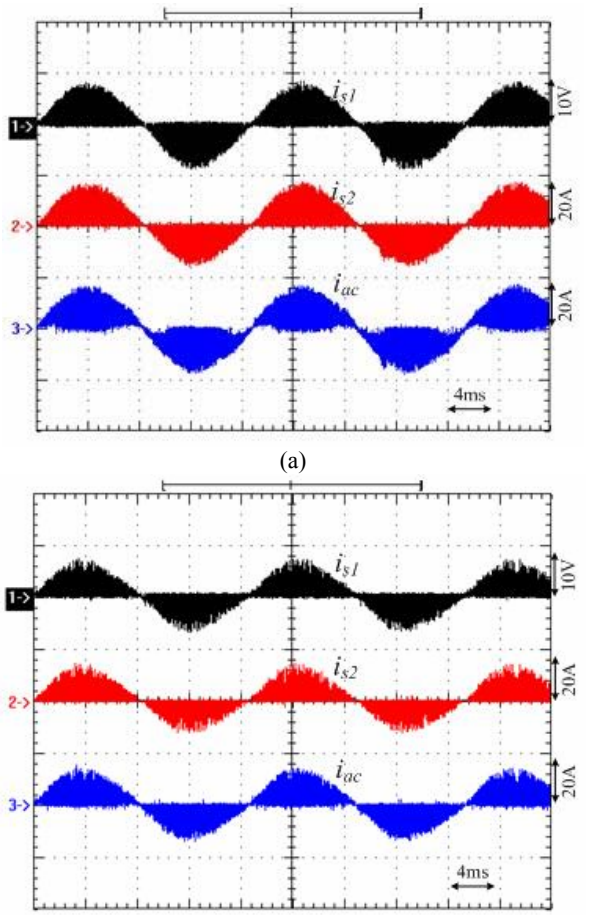


Fig. 6. Measured AC side currents of two circuit modules at full load condition and (a) low line voltage $v_s$=110 $V_{rms}$ (b) high line voltage $v_s$=220 $V_{rms}$.

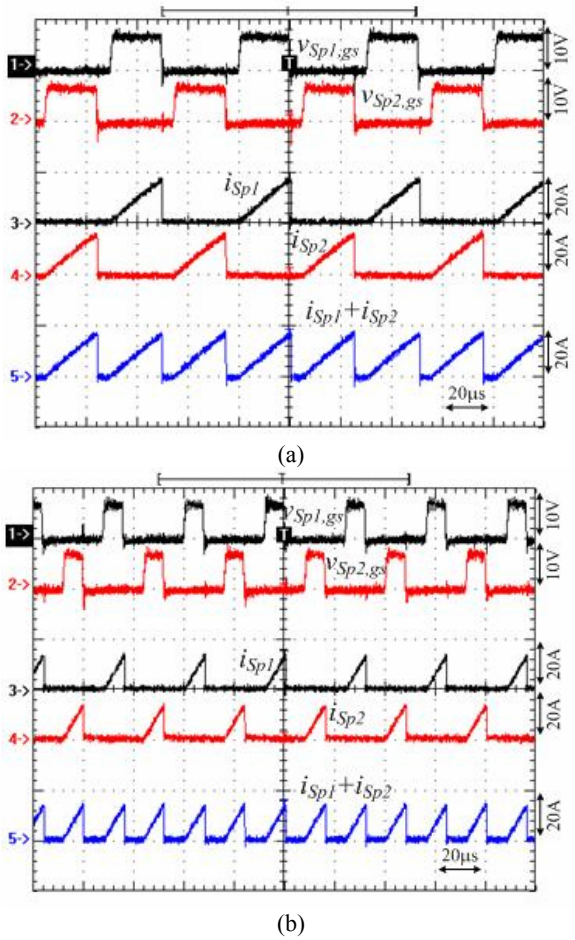


Fig. 7. Measured switch signals, $v_{Sp1,gs}$ and $v_{Sp2,gs}$, switch currents, $i_{Sp1}$ and $i_{Sp2}$, and the net input current $i_{ac}$=$i_{Sp1}$+$i_{Sp2}$ during the positive line voltage with full load and (a) low line voltage ($v_s$=110 $V_{rms}$) (b) high line voltage ($v_s$=220 $V_{rms}$).

$$v_{Dp1,stress} = v_{Dp3,stress} = v_{Dn1,stress} = v_{Dn3,stress} = \sqrt{2}V_{s,\max} \quad (9)$$

$$v_{Dp2,stress} = v_{Dp4,stress} = v_{Dn2,stress} = v_{Dn4,stress} = \sqrt{2}V_{s,\max} + (V_o/2) \quad (10)$$

Based on the voltage-second balance of the inductors $L_{p1}$, $L_{p2}$, $L_{n1}$ and $L_{n2}$, the DC voltage conversion ratio of the proposed converter is derived as:

$$M_{dc} = V_o / |v_s| = 2\delta/(1-\delta) \quad (11)$$

where $\delta$=$t_{on}$/$T_{sw}$.

## V. Design Procedure and Experimental Results

In this section, the design procedures for a laboratory prototype are presented and experiments are provided to verify the performance of the proposed converter. The specifications of the proposed converter are $v_s$=90$V_{rms}$~265$V_{rms}$; $V_o$=200$V$; $P_o$=500$W$; $\eta$=90% and $f_{sw,min}$=20kHz. From (3) and (5), the duty ratio at the peak voltage of the low line voltage can be obtained.

$$\delta' = \frac{t_{on}}{T_{sw}} = \frac{\eta V_o}{V_o + 2\sqrt{2}V_{s,\min}} = \frac{0.9\times 200}{200 + 2\sqrt{2}\times 90} \approx 0.4 \quad (12)$$

From (1) and (2), the peak inductor currents are given as:

$$i_{Lp1,\max,pk} = i_{Lp2,\max,pk} = i_{Ln1,\max,pk} = i_{Ln2,\max,pk} = \sqrt{2}P_o/(\eta V_{s,\min}\delta') = \sqrt{2}\times 500/(0.9\times 90\times 0.4) \approx 21.82A \quad (13)$$

From (7), the inductances of $L_{p1}$~$L_{n2}$ are obtained as:

$$L = \frac{\delta'\eta V_{s,\min}^2}{f_{sw,\min} I_o (V_o + 2\sqrt{2}V_{s,\min})} = \frac{0.4\times 0.9\times 90^2}{20000\times 2.5\times (200 + 2\sqrt{2}\times 90)} \approx 128\mu H \quad (14)$$

From (8)-(10), the voltage stresses of the active switches and the rectifier diodes are given as:

$$v_{Sp1,stress} = v_{Sp2,stress} = v_{Sn1,stress} = v_{Sn2,stress} = \sqrt{2}V_{s,\max} + (V_o/2) = \sqrt{2}\times 265 + (200/2) = 475V \quad (15)$$

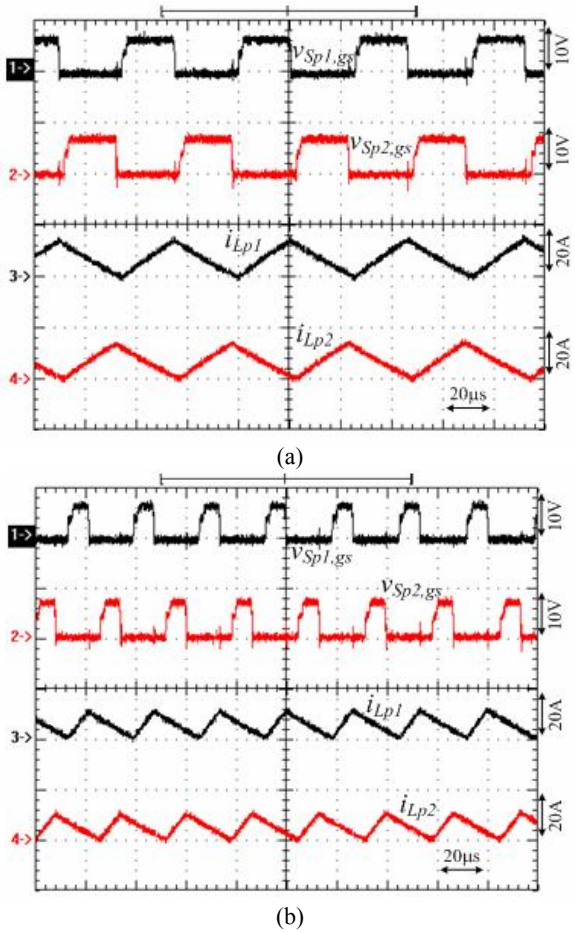


Fig. 8. Measured switch signals, $v_{Sp1,gs}$ and $v_{Sp2,gs}$, and inductor current, $i_{Lp1}$ and $i_{Lp2}$, at full load and (a) low line voltage ($v_s$=110 $V_{rms}$) (b) high line voltage ($v_s$=220 $V_{rms}$).

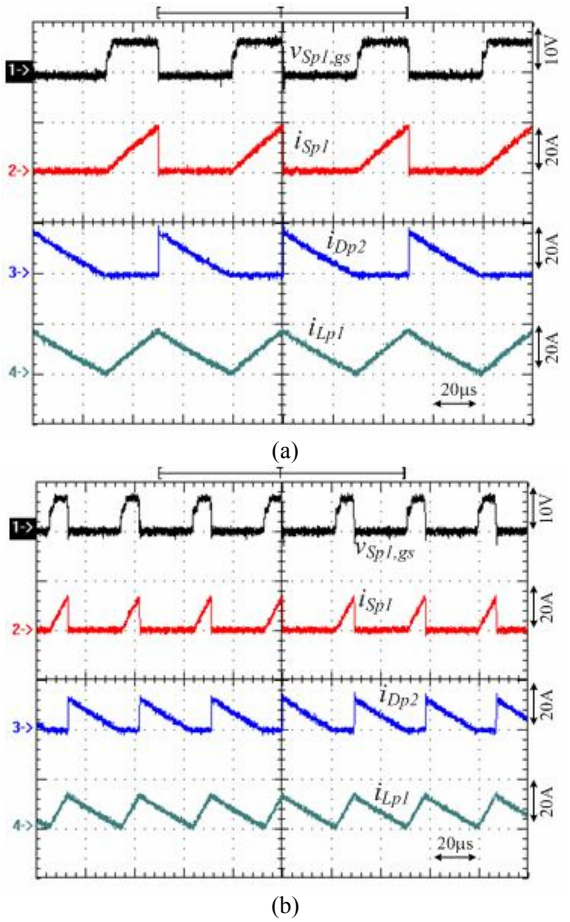


Fig. 9. Measured gate voltage $v_{Sp1,gs}$, switch current $i_{Sp1}$, diode current $i_{Dp2}$ and inductor current $i_{Lp1}$ of circuit module 1 at full load and (a) low line voltage $v_s$=110 $V_{rms}$ (b) high line voltage $v_s$=220 $V_{rms}$.

$$v_{Dp1,stress} = v_{Dp3,stress} = v_{Dn1,stress} = v_{Dn3,stress} = \sqrt{2}V_{s,\max} = \sqrt{2} \times 265 = 375V \quad (16)$$

$$v_{Dp2,stress} = v_{Dp4,stress} = v_{Dn2,stress} = v_{Dn4,stress} = \sqrt{2}V_{s,\max} + (V_o / 2) = \sqrt{2} \times 265 + (200/2) = 475V \quad (17)$$

Fast recovery diodes MUR1560 are used for the rectifier diodes $D_{p1}$~$D_{n4}$. MOSFETs IRFP460 are used for the active switches $S_{p1}$~$S_{n2}$. The output capacitances of $C_p$ and $C_n$ are 680 F. A boundary conduction mode control PWM IC UCC28061 is used to generate the control signals for the active switches $S_{p1}$~$S_{n2}$ and to regulate the output voltage $V_o$. A type-II voltage controller based on the *k*-factor approach is adopted to select the zero-pole frequencies with a 70 degree phase margin and a -20dB gain margin.

The measured AC source voltage $v_s$ and the line current $i_s$ at low and high line voltages with the rated power are shown in Fig. 4. The line current is a sinusoidal waveform in phase with the mains voltage. The measured power factor is 0.99, the total harmonic distortion of the line current is 7.9%, and the measured circuit efficiency is 92.7% at a low line voltage. Similarly the measured power factor is 0.93, the total harmonic distortion of the line current is 10.3%, and the measured circuit efficiency is 90.5% at a high line voltage. If a low conduction resistance on the MOSFETs and a low voltage drop on the rectifier diodes are adopted in the proposed circuit, the circuit efficiency can be increased by about 2-3% under full load. Fig. 5 gives the measured switch signals, $v_{Sp1,gs}$ and $v_{Sn1,gs}$, the switch currents, $i_{Sp1}$ and $i_{Sn1}$, and the input current $i_{s1}$ of circuit module 1 under full load. It is clear that the switch $S_{p1}$ is controlled at the positive line voltage and that the switch $S_{n1}$ is controlled at the negative line voltage. Thus the input current $i_{s1}$ of circuit module 1 is a sinusoidal waveform due to the BCM operation. Fig. 6 gives the measured AC side currents of the two circuit modules $i_{s1}$, $i_{s2}$ and $i_{ac}$ under full load. It is clear that the two AC source currents are balanced. Fig. 7 shows the measured switch signals, $v_{Sp1,gs}$ and $v_{Sp2,gs}$, the switch currents, $i_{Sp1}$ and $i_{Sp2}$, and the net input current $i_{ac}$=$i_{Sp1}$+$i_{Sp2}$ during the positive line voltage under full load. Fig. 8 illustrates the measured switch signals, $v_{Sp1,gs}$ and $v_{Sp2,gs}$, and the inductor current, $i_{Lp1}$ and $i_{Lp2}$,

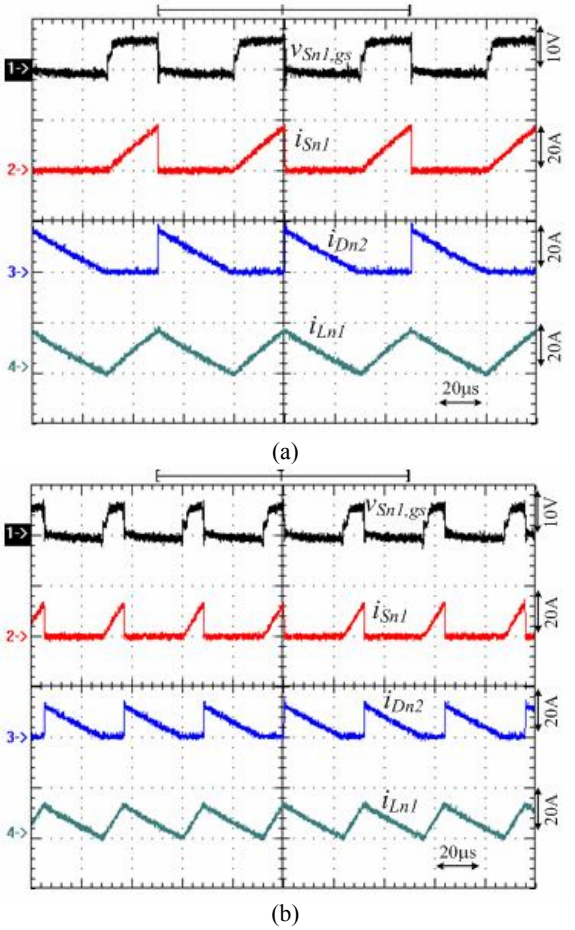


Fig. 10. Measured gate voltage $v_{Sn1,gs}$, switch current $i_{Sn1}$, diode current $i_{Dn2}$ and inductor current $i_{Ln1}$ of circuit module 1 at full load and (a) low line voltage $v_s$=110 $V_{rms}$ (b) high line voltage $v_s$=220 $V_{rms}$.

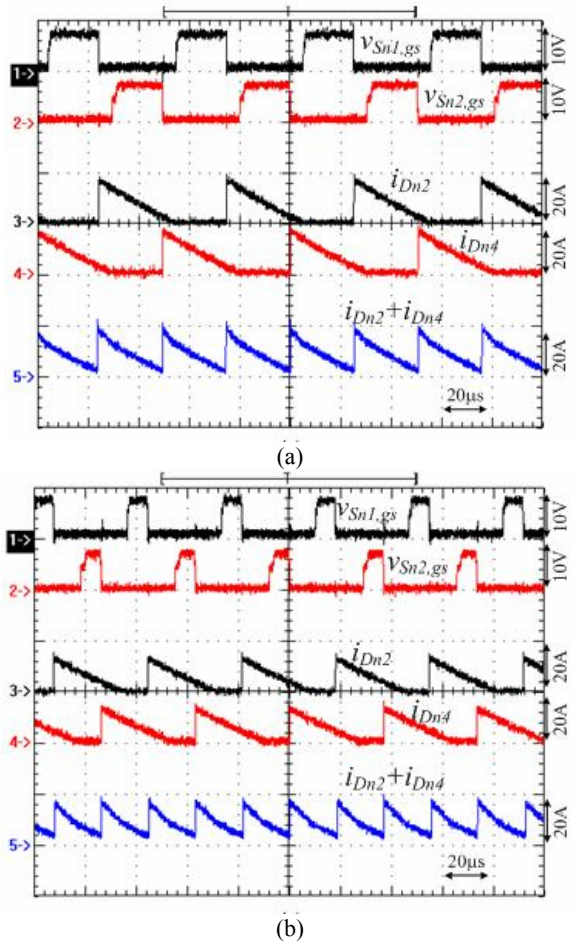


Fig. 11. Measured gate voltages, $v_{Sn1,gs}$ and $v_{Sn2,gs}$, diode currents, $i_{Dn2}$ and $i_{Dn4}$, and the resultant current $i_{Dn2}+i_{Dn4}$ at full load and (a) low line voltage $v_s$=110 $V_{rms}$ (b) high line voltage $v_s$=220 $V_{rms}$.

under full load. Since the interleaved PWM operation is adopted in the proposed converter, the ripple current of $i_{Lp1}$ and $i_{Lp2}$ can partially cancelled each other out. Fig. 9 gives the measured gate voltage $v_{Sp1,gs}$, the switch current $i_{Sp1}$, the diode current $i_{Dp2}$ and the inductor current $i_{Lp1}$ of circuit module 1 under a positive line voltage and a full load. Similarly the measured gate voltage $v_{Sn1,gs}$, the switch current $i_{Sn1}$, the diode current $i_{Dn2}$ and the inductor current $i_{Ln1}$ of circuit module 1 under a negative line voltage and a full load are shown in Fig. 10. It is clear that the switches $S_{p1}$ and $S_{n1}$ are turned on under ZCS and that the diodes $D_{p2}$ and $D_{n2}$ are turned off under ZCS. Thus the switching losses of the active switches and the reverse recovery losses of the fast reverse diodes are reduced. Fig. 11 gives the measured results of the two PWM signals, $v_{Sn1,gs}$ and $v_{Sn2,gs}$, the diode currents, $i_{Dn2}$ and $i_{Dn4}$, and the resultant current $i_{Dn2}$+$i_{Dn4}$ under a full load.

## VI. Conclusion

This paper presents an interleaved bridgeless buck-boost PFC converter with voltage doubler output to achieve power factor correction, conduction loss reduction, a low harmonic current, a low ripple current and a sinusoidal AC source current. The BCM operation in the proposed converter can achieve ZCS turn-on for the power switches and ZCS turn-off for the fast recovery diodes. Thus the switching losses of the active switches and the reverse recovery losses of the rectifier diodes are reduced. The buck-boost conversion can reduce the voltage stress of the active switches in the post stage such as the isolated DC/DC converter. The voltage doubler output can double its output voltage to extend the useable energy of the capacitor when the line voltage is off. Finally, experiments, conducted on a 500W laboratory prototype, are presented to demonstrate the circuit performance.

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