JPE 12-3-3

Analysis of Parameter Effects on the Small-Signal Dynamics of Buck Converters with Average Current Mode Control

Ruqi Li[†], Tony O'Brien^{*}, John Lee^{*}, John Beecroft^{*}, and Kenny Hwang^{*}

^{†*}Cisco, Inc., San Jose, California, United States

Abstract

In DC-DC Buck converters with average current mode control, the current loop compensator provides additional design freedom to enhance the converter current loop performance. On the other hand, the current loop circuit elements append substantial amount of complexity to not only the inner current loop but also the outer voltage loop, which makes it demanding to quantify circuit and operating parameter effects on the small-signal dynamics of such converters. Despite the difficulty, it is shown in this paper that parameter effects can be analyzed satisfactorily by using an existing small-signal model in conjunction with a newly proposed simplified alternative. As a result of the study, new insight into average current mode control is uncovered and discussed quantitatively. Measurable experimental results on a prototype averaged-current-mode-controlled Buck converter are provided to facilitate the analytical study with good correlation.

Key words: Average current mode control, Buck converters, Parameters effects, Small signal average models,

I. INTRODUCTION

Average Current Mode Control (ACMC) has been widely used in Boost converter Power Factor Correction (PFC) rectifier applications since its introduction in the late 1980s. In designing feedback control loops of such converters, the current loop and the voltage loop are essentially decoupled, and they can thus be treated separately. Unfortunately, in low voltage DC-DC Buck converters with ACMC, this is no longer the case. The added current loop compensator affects not only the inner current loop but also the outer voltage loop. Consequently, the small-signal dynamics of the Buck converters with ACMC possess unique characteristics, which are related directly with the converter circuit and operating parameters. It is highly desirable to perform a designoriented analysis to uncover the parameter effects to fully understand the nature of ACMC to develop effective design strategies.

Several publications have discussed this topic in the past

Recommended for publication by Associate Editor Byung-Cho Choi. [†]Corresponding Author: ruli@cisco.com

Tel: +408-902-8282, Fax: +408-527-1712, Cisco, Inc.

^{*}Cisco, Inc., San Jose, California, United States

[1]-[5]. The effect of mid-frequency gain of the current loop compensator, which is closely related to the ratio of the two resistive elements in the circuit, has been the main topic [1]-[2]. Based on the operating principles of this control scheme, an upper gain limit has been proposed to prevent undesired switching instabilities.

In [3], the inductor current ripple effect on the PWM modulator gain is taken into account in the small-signal model derivation, leading to an additional term in the gain expression. The derivation assumes an ideal current amplifier and absence of the high-frequency, ripple-reduction capacitor in the current loop compensator. The model reported in [4] proposes a more complex PWM modulator gain expression based on the actual waveform at the output of the current amplifier. The paper is devoted mainly to extending sampling effect of the PCMC into ACMC. As expected, the resultant model predicts that sub-harmonic oscillations at exactly half the switching frequency can occur for ACMC.

The effect of the high-frequency capacitor in the current loop compensator is also discussed in the literature. References [2], [4] propose guidelines to optimally place the capacitor-associated high-frequency pole in the current loop to enhance its performance.

Reference [5] discusses conceptually the effect of input

Manuscript received Aug. 29, 2011; revised Mar. 5, 2012



Fig. 1. Single phase ACMC Buck converter small-signal average model.

voltage variation on the poles of the Buck converter control-to-output voltage transfer function. The input voltage is referred as an operating parameter in this paper.

Owing to the complexity of ACMC models, the true parameter effects on the converter small-signal dynamics cannot be readily visualized and analyzed. A recent study [6] utilizes a design-oriented approach. Unlike the usual treatment, efforts are made to simplify an existing model in [2] as much as possible. This approach leads to a new small-signal model which is used, in conjunction with the original model, to perform an analysis of parameter effects on the ACMC Buck converter control loop transfer functions in this paper. Because the simplified model is expressed explicitly with converter circuit and operating parameters, it has the intrinsic property to clearly identify their effects on the ACMC Buck converter frequency response in low, mid, and high frequencies to explain what is observed with experimental data. As a result, new ACMC characteristics are revealed with experimental verification using a Buck converter as an example. Parameter effects on the ACMC Boost and Buck-Boost topologies can be analyzed similarly by using their simplified models [7].

II. SMALL-SIGNAL AVERAGE MODEL FOR THE BUCK DC-DC CONVERTER WITH ACMC

Fig. 1 shows the single phase ACMC Buck converter small-signal average model, and Fig. 2 is the control loop block diagram based on the equivalent circuit model.

From Fig. 2, two main transfer functions, namely the current loop gain, $T_c(s)$, and the control-to-output voltage transfer function, $T_p(s)$, can be derived. With the adoption of commonly used notations, $T_c(s)$ is found to be



Fig. 2. Single phase ACMC Buck converter control loop block diagram.

$$T_c(s) = R_s K_m H_c(s) G_{dc}(s) \tag{1}$$

or

$$T_{c}(s) = \frac{R_{s}}{R_{L}} \frac{V_{g}K_{m}[1 + (R_{L} + r_{c})Cs](1 + \frac{s}{s_{z}})}{\frac{s}{s_{i}}[1 + (\frac{L}{R_{L}} + r_{c}C)s + LC(1 + \frac{r_{c}}{R_{L}})s^{2}](1 + \frac{s}{s_{p}})}$$
(2)

with
$$H_c(s) = \frac{(1+\frac{s}{s_2})}{\frac{s}{s_i}(1+\frac{s}{s_p})} = \frac{[R_1(C_1+C_2)](1+sC_2R_2)}{s[1+s(C_1//C_2)R_2]}$$
 (3)

defined as the current loop compensator transfer function, and $G_{dc}(s)$ the control-to-inductor current transfer function. The control-to-output voltage transfer function is given by [2] (6)

$$\frac{\hat{v}_{o}(s)}{\hat{v}_{c}(s)} = T_{p}(s) = \frac{T_{v}(s)}{1 + T_{c}(s)} = \frac{K_{m}(1 + r_{c}Cs)[1 + H_{c}(s)]G_{dv}(s)}{1 + R_{s}K_{m}H_{c}(s)G_{dc}(s)}$$
(4)

where $G_{dv}(s)$ is the duty-cycle-to-output capacitor voltage transfer function.

Expansion of (4) leads to

$$T_{p}(s) = \frac{R_{L}}{R_{S}} \frac{(1 + r_{c}Cs)[1 + (\frac{1}{s_{i}} + \frac{1}{s_{z}})s + \frac{s^{2}}{s_{i}s_{p}}]}{\Delta(s)}$$
(5)

where $\Delta(s) = 1 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4$

$$\begin{split} a_{1} &= (R_{L} + r_{c})C + R_{2}C_{2} + \frac{R_{L}}{R_{s}K_{m}V_{g}}R_{1}(C_{1} + C_{2}) \\ a_{2} &= (R_{L} + r_{c})CR_{2}C_{2} + \frac{R_{L}}{R_{s}K_{m}V_{g}}\left[(\frac{L}{R_{L}} + r_{c}C)R_{1}(C_{1} + C_{2}) + R_{1}C_{1}R_{2}C_{2}\right] \\ a_{3} &= \frac{R_{L}}{R_{s}K_{m}V_{g}}\left[LC(1 + \frac{r_{c}}{R_{L}})R_{1}(C_{1} + C_{2}) + (\frac{L}{R_{L}} + Cr_{c})R_{1}C_{1}R_{2}C_{2}\right] \\ a_{4} &= \frac{R_{L}}{R_{s}K_{m}V_{g}}LC(1 + \frac{r_{c}}{R_{L}})R_{1}C_{1}R_{2}C_{2} . \end{split}$$

The above equations demonstrate that with the addition of the current loop compensator, the order of the controlto-output voltage transfer function is increased by two as a result of the two added capacitive elements C_1 and C_2 . This implies that unlike Buck converters with Voltage Mode Control (VMC) or PCMC, the current loop compensator circuit elements in ACMC Buck converters also directly affect the dynamics of the power stage transfer function.

For small-signal dynamic analyses, the 4th order polynomial (6) is the primary focus of investigation. Due to its high order, poles of $\Delta(s)$ can be solely obtained numerically. For analytical and design-oriented studies, References [6]-[7] propose an approximate solution to (6). An outline of the simplified model is given below.

In the numerator of (5), besides the first zero, $s_{z1} = (1/r_cC)$, caused by the output capacitor Equivalent Series Resistance (esr), there exists a second order term. Since its two roots (zeros) are far separated from each other in frequency, they can be well approximated by

$$s_{z2} \approx (\frac{1}{S_i} + \frac{1}{S_z})^{-1} = \frac{1}{R_1(C_1 + C_2) + R_2C_2}$$
 (7)

$$s_{z_3} \approx (\frac{1}{s_i} + \frac{1}{s_z}) s_i s_p \approx \frac{1}{C_1(R_1 / / R_2)}$$
 (8)

The second zero, s_{z2} , normally lies in the mid-frequency range, and the third zero, s_{z3} , in the much higher-frequency range (well beyond half the switching frequency). Therefore, its effect can be ignored.

In the denominator of (5), denote the exact poles, resonant frequencies and quality factors as s_{j^2} , j = 1 to 4, ω_k and Q_k , k = 1, 2. Also denote the approximate poles, resonant

frequencies and quality factors as s_{pj} , j = 1 to 4, ω_{nk} and Q_{nk} , k = 1, 2. If coefficients a_1 to a_4 in (6) satisfy

$$a_1 \gg (a_2/a_1) > (a_3/a_2) \gg (a_4/a_3),$$
 (9)

 $\Delta(s)$ is approximately equal to

$$T_{p}(s) = \frac{R_{L}}{R_{S}} \frac{(1+r_{c}Cs)[1+(\frac{1}{s_{i}}+\frac{1}{s_{z}})s+\frac{s^{2}}{s_{i}s_{p}}]}{(1+\frac{s}{s_{1}})(1+\frac{s}{\omega_{1}\varrho_{1}}+\frac{s^{2}}{\omega_{1}^{2}})(1+\frac{s}{s_{4}})}$$
$$\approx \frac{R_{L}}{R_{S}} \frac{(1+r_{c}Cs)(1+\frac{s}{s_{z2}})(1+\frac{s}{s_{z3}})}{(1+\frac{s}{\omega_{n1}\varrho_{n1}}+\frac{s^{2}}{\omega_{n1}^{2}})(1+\frac{s}{s_{p4}})}$$
(10)

with

$$s_1 \approx s_{p1} \approx \frac{1}{(R_L + r_c)C + R_2C_2 + \frac{R_L}{R_s K_m V_g} R_1(C_1 + C_2)}$$
(11)

$$\omega_{l}^{2} \approx \omega_{nl}^{2} \approx \frac{R_{s}K_{m}V_{g}}{R_{l}} \frac{1}{L(C_{l}+C_{2})}$$
(12)

$$Q_1 \approx Q_{n1} \approx \frac{1}{R_2 C_2} \sqrt{\frac{R_1}{R_s K_m V_g}} \sqrt{L(C_1 + C_2)}$$
 (13)

$$s_4 \approx s_{p4} \approx \frac{1}{R_2(C_1//C_2)}$$
 (14)

If coefficients a_1 to a_4 in (6) satisfy

$$a_1 >> (a_2/a_1) >> (a_3/a_2) > (a_4/a_3),$$
 (15)
is approximately equal to

$$\Delta(s)$$
 is approximately equal to

$$T_{p}(s) = \frac{R_{L}}{R_{s}} \frac{(1+r_{c}Cs)[1+(\frac{1}{s_{i}}+\frac{1}{s_{z}})s+\frac{s^{2}}{s_{i}s_{p}}]}{(1+\frac{s}{s_{1}})(1+\frac{s}{s_{2}})(1+\frac{s}{\omega_{2}Q_{2}}+\frac{s^{2}}{\omega_{2}^{2}})}$$
$$\approx \frac{R_{L}}{R_{s}} \frac{(1+r_{c}Cs)(1+\frac{s}{s_{z2}})(1+\frac{s}{s_{z3}})}{(1+\frac{s}{s_{p1}})(1+\frac{s}{s_{p2}})(1+\frac{s}{\omega_{n2}Q_{n2}}+\frac{s^{2}}{\omega_{n2}^{2}})}$$
(16)

with
$$s_2 \approx s_{p2} \approx \frac{1}{R_2 C_2} + \frac{1}{(R_L + r_c)C}$$
 (17)

$$\omega_2^2 \approx \omega_{n2}^2 \approx \frac{R_s K_m V_g}{R_1} \frac{1}{LC_1}$$
(18)

$$Q_2 \approx Q_{n2} \approx \frac{R_2 C_2}{(C_1 + C_2)} \sqrt{\frac{R_s K_m V_g}{R_l}} \sqrt{\frac{C_1}{L}}$$
(19)

If coefficients a_1 to a_4 in (6) satisfy

$$a_1 \gg (a_2/a_1) > (a_3/a_2) > (a_4/a_3),$$
 (20)

Equation (6) usually contains four real poles. Under this condition, the coefficient ratios of the second and the third inequalities in (20) are normally less than six, and either (10)

 L^1 R^2 V_{g} L V_{o} C $r_{\rm c}(esr)$ (V) (A) (V) (µH) $(m\Omega)$ (µF) $(m\Omega)$ 5 – 24 V 1 – 15 A 12 V 7.5 A 3.3 0.7 0.75 2000 5 Nominal Nominal

TABLE I

MAIN DESIGN SPECIFICATION AND POWER STAGE PARAMETERS

Note: 1. The per phase inductance $L_{pp} = 1.4 \mu$ H, and the equivalent single phase inductance $L = 0.5L_{pp}$.

2. The per phase current sense resistor $R_{pp} = 1.5 \text{ m}\Omega$, and the equivalent single phase current sense resistor $R = 0.5R_{pp}$.

TABLE II PWM Control IC And Current Loop Main Parameters

| Parameter | Nominal Value | Value Change Range |
|-----------------------------|---------------|--------------------|
| f_{sw} (per phase) | 500 kHz | None |
| g_m | 550 μS | None |
| $A_{\rm s}$ | 36 | None |
| $R_{\rm s} = R * A_{\rm s}$ | 27 mΩ | None |
| $R_1 = g_m^{-1}$ | 1.82 kΩ | None |
| <i>C</i> ₁ | 100 pF | 10 pF – 220 pF |
| <i>C</i> ₂ | 3300 pF | 1800 pF – 0.047 μF |
| R ₂ | 4.99 kΩ | 0.499 kΩ – 18.2 kΩ |
| $R_2/R_1(Gain)$ | 2.74 | 0.274 - 10.0 |
| K _m | 0.50 | 0.2 - 2.0 |

or (16) can be used to calculate the approximate poles of (6). However, there could be an increase in errors in the approximate pole calculations when either (10) or (16) is used.

It is obvious from the above analysis that for an ACMC Buck converter, the control-to-output voltage transfer function (4) can be approximated by two different mathematical representations (10) and (16), depending on the polynomial coefficients a_1 to a_4 which, in turn, are determined by the converter circuit and operating parameters. The distinct difference between (4) and (10), (16) is that the approximate poles, zeros, resonant frequencies and quality factors given by (7)-(8), (11)-(14) and (17)-(19) are associated explicitly with the converter circuit and operating parameters. This makes it easy to visualize and analyze how parameter changes affect the locations of the poles and zeros of (4), thus the small-signal dynamics. The simplified model has been experimentally verified against test data and model (4) predictions. In the next section, the polynomial $\Delta(s)$ in (6) and its approximate expressions (10) and (16) are analyzed in-depth to reveal a number of interesting properties of ACMC Buck converters.

III. EFFECTS OF PARAMETERS ON ACMC BUCK CONVERTER SMALL-SIGNAL DYNAMICS

In this study, the same example in [6] is adopted. The converter is a dual phase DC-DC Buck converter, and its single phase equivalent small-signal model is shown in Fig. 1 along with component reference designators. TABLE I and TABLE II show the main converter specifications and component values.

To limit the discussion, the power stage components, which are determined by the power converter design requirements, are not varied. The converter circuit parameters that are varied are highlighted in TABLE II, and the operating parameters are highlighted in TABLE I. The range of variation for each parameter is also given in the tables. Each of these parameters is altered one at a time while others are held constant at their nominal or specified values. Two main transfer functions, $T_c(s)$ and $T_p(s)$ given in (2) and (5), are discussed in the following subsections.

A. Effects of circuit and operating parameters on the design of the current loop

The design of the current loop is well documented in the literature [1]-[2], [4]-[5]. One design consideration, which is less discussed quantitatively, is the parameter-dependent current loop gain crossover frequency. A generalized expression for this design parameter is given in [6]

$$f_{c} = \frac{\omega_{c}}{2\pi} \approx \frac{R_{2}C_{2}}{2\pi R_{1}(C_{1}+C_{2})} \frac{R_{s}K_{m}V_{g}}{L}$$
(21)

If $C_1 << C_2$, which is usually the case in practical designs, it follows that $C_2/(C_1+C_2)\approx 1$, and (21) can be further simplified. The above equation plainly identifies the dependency of the current loop gain crossover frequency on the converter circuit as well as its operating parameters. The dependency of f_c on the parameters R_s , L and K_m is fixed once the converter power stage design is complete. The only two factors that most influence f_c in the design and operation of the converter are the mid-frequency gain R_2/R_1 and the input voltage V_g .

The maximum allowable mid-frequency gain for the current loop is suggested in [1] and subsequently modified in [2] as

$$\frac{R_2}{R_1} \le Minimum \left(\frac{2Lf_{sw}}{(V_{g_max} - V_o)R_sK_m}, \frac{Lf_{sw}}{V_oR_sK_m} \right)$$
(22)

The first term in the parenthesis in (22), which is usually lower than the second term, is to avoid possible switching instabilities by ensuring that the average value is higher than twice the peak-to-peak voltage ripple at the output of the current amplifier. With the converter circuit parameters given in TABLE I and TABLE II, this gain is calculated to be $R_2/R_1 \le 2.5$. To take into account the fact that the MAX5066 PWM controller used in this design does have a certain amount of DC offset to guarantee a minimum duty cycle operation without the high-frequency capacitor C_1 , the

| Electric Parameters | Calculated Values |
|---|-------------------|
| R_2/R_1 (Gain) maximum allowed with $V_{g_{max}} = 24$ V | 2.50 |
| R_2 / R_1 (Gain) designed | 2.74 |
| Nominal f_c and phase margin | 98.28 kHz |
| at 12 V input voltage | 71.0 degs |
| Minimum $f_{\rm c}$ and phase margin | 42.29 kHz |
| at 5 V input voltage | 72.0 degs |
| Maximum $f_{\rm c}$ and phase margin | 196.4 kHz |
| at 24 V input voltage | 60.0 degs |

 TABLE III

 CALCULATED ELECTRICAL QUANTITIES OF THE CURRENT LOOP

nominal gain is chosen to be 2.74. Another reason to not choose a large gain is to limit an excessive current loop gain crossover frequency when the wide input voltage range is considered. TABLE III lists calculated electrical quantities of the designed current loop. It is noted that even with a moderate gain of only 2.74, there is nearly a five-to-one current loop gain crossover frequency variation when the input voltage varies from its minimum to maximum. The maximum current loop gain crossover frequency approaches half the switching frequency of 250 kHz with the maximum input voltage.

B. Effects of PWM modulator gain K_m on the controlto-output voltage transfer function

The PWM modulator gain is generally modeled as the same as that with VMC [2]. This has been experimentally verified to be valid under the assumption of negligible inductor ripple contents at the output of the current amplifier in the current loop [5]. Ways to improve modeling of the PWM modulator gain are reported in [3]-[4]. However, what has not been studied is how this parameter affects the ACMC Buck converter small-signal dynamics. With the expressions of the control-to-output voltage transfer function in either its concise form (4) or expanded form (5), it is difficult to identify and quantify its unique role which it plays in the transfer function.

To better understand its effect on the ACMC Buck converter small-signal dynamics, Equation (6) is solved numerically with the modulator gain varied from 0.25 to 2.0 while the converter input voltage and loading are set at 12 V and 15 A, respectively. Fig. 3 illustrates how the four poles of (6) migrate and regroup as K_m is varied. With an initial value of $K_m = 0.25$, all the four poles lie on the real axis at locations marked as "Start". As K_m increases, s_1 stays essentially at the same location. This implies that effect of K_m on this pole is minimal. While the frequencies of s_2 and s_4 decrease, the frequency of s_3 increases. As the value of K_m rises further, s_3



Fig. 3. Illustration of pole migration and regrouping as $K_{\rm m}$ increases from 0.25 to 2.0. Input voltage is 12 V and loading is 15 A.

and s_4 become two identical real poles, coinciding at Point X_2 . Additional increase of K_m results in less and less damping. Consequently, a pair of complex conjugate poles is formed. The higher the K_m value, the greater the resonant frequency ω_2 and quality factor Q_2 . The final locations of the four poles are marked as "End" when K_m reaches its maximum value. The two zeros, s_{z1} and s_{z2} , remain unchanged throughout the process since they are not dependent on K_m .

The above phenomenon can be adequately modeled by (16)-(19), which predict that K_m affects mainly the high-frequency portion of the control-to-output voltage transfer function represented by the second order term in (16). As K_m increases, values of both the resonant frequency and quality factor rise. Additional studies showed that the relationship between the resonant frequency ω_2 , the quality factor Q_2 of the second order term in (16) and K_m were modeled well with simple square root functions given by (18)-(19).

The analytical expressions (11) and (17) to (19) can be used to calculate approximate locations of the poles as they migrate and regroup in the left half of the complex plane when the value of K_m changes. In particular, the two identical poles s_3 and s_4 at Point X_2 can be approximately evaluated by using the second order term in (16). It follows that

$$s_3, s_4 \approx s_{p3}, s_{p4} = \frac{-\omega_{n2}}{2Q_{n2}} \pm \omega_{n2} \sqrt{\left(\frac{1}{2Q_{n2}}\right)^2 - 1}$$
 (23)

Under the condition of critical damping, the two identical real poles are

$$s_3 = s_4 \approx s_{p3} = s_{p4} = -\frac{\omega_{n2}}{2Q_{n2}} = -\frac{s_p}{2} = -\frac{1}{2} \frac{(C_1 + C_2)}{R_2(C_1 C_2)}$$
 (24)

Thus, the frequency of the two identical poles at Point X_2 is approximately equal to half the high-frequency pole, s_p , of the current loop compensator. This value remains unchanged even when s_3 and s_4 become a pair of complex conjugates



Fig. 4. Predicted effects of $K_{\rm m}$ on the control-to-output voltage transfer function. $K_{\rm m}$ varies from 0.25 to 2 with 0.5 increment. Input voltage is 12 V and loading is 15 A.



Fig. 5. Illustration of pole migration and regrouping as $K_{\rm m}$ rises from 0.25 to 2.0. Input voltage is 5 V and loading is 15 A.

because their real parts do not depend on the value of $K_{\rm m}$. Fig. 4 shows the calculated effects of $K_{\rm m}$ on the Bode plots of control-to-output voltage transfer function. As predicted by (18)-(19), the Bode plots clearly illustrate increases in resonant peaking and resonant frequencies between 150 kHz and 400 kHz as $K_{\rm m}$ rises.

A similar analysis can be performed with the converter running at a high duty cycle. Fig. 5 illustrates how the four poles in (6) migrate and regroup as the value of K_m changes from 0.25 to 2.0 with 5 V input voltage of and 15 A loading. Initially, the four poles contain two real ones and two complex conjugate ones as predicted by (10). As the value of K_m increases, the quality factor, $Q_2 \approx Q_{n2}$, decreases according to (13). Hence, s_2 and s_3 move rapidly toward the real axis and coincide at Point X_1 when the value of K_m becomes sufficiently large. Then, a similar pole movement pattern as in the low duty cycle operation case shown in Fig. 3 follows afterwards.



Fig. 6. Illustration of pole and zero migration and pole regrouping as the current loop gain R_2/R_1 increases.

It can be shown from the second order term of (10) that under the condition of critical damping, the two real poles s_2 and s_3 intersecting at Point X_1 can be estimated by

$$s_2 = s_3 \approx s_{p2} = s_{p3} = -\frac{\omega_c}{2}$$
 (25)

Therefore, the frequency of the two real poles at Point X_1 is approximately equal to half the current loop gain crossover frequency given by (21).

C. Effects of current loop gain R_2/R_1 on the controlto-output voltage transfer function

Published papers focus on the effects of the mid-frequency gain R_2/R_1 on the ACMC Buck converter current loop [1]-[2]. It is demonstrated in this paper that this gain also has dramatic effects on the control-to-output voltage transfer function. Fig. 6 shows how poles of (6) migrate and regroup as the gain increases from 0.274 to 10. Similar to the previous case in Fig. 5 when the gain is low, Equation (6) contains two real poles, s_1 and s_4 , and two complex conjugate poles, s_2 and s_3 . As the gain increases, the magnitudes of the real parts of s_2 and s_3 become larger while the imaginary parts decrease until the two become real poles, coinciding at Point X_1 . As s_2 and s_3 move toward Point X_1 , the frequency of s_4 decreases, and s_1 stays nearly at its "Start" point. This part of the pole movement can be readily explained by using (11) to (14). When R_2/R_1 increases from a very small to a larger value, it causes Q_1 to decrease as predicted by (13), leading to higher damping of the second order term in (10). Consequently, this causes s_2 and s_3 to become real poles if R_2/R_1 is large enough.

When the gain continues to rise, s_3 and s_4 coincide at Point X_2 , and they regroup to form a pair of complex conjugates while s_1 and s_2 stay as two real poles. It is noted that unlike the previous case shown in Fig. 3 in which the real parts of s_3 and s_4 in (24) remain unchanged as the value of the modulator



Fig. 7. Predicted (solid line) and measured (dotted line) Bode plots of the control-to-output voltage transfer function with $R_2 = 0.499 \text{ k}\Omega$, $R_2/R_1 = 0.274$, 12 V input voltage and 7.5 A load.

gain K_m gets larger, the real parts of s_3 and s_4 do become progressively smaller, suggesting less and less damping of this second order term. Equations (18) and (19) model this phenomenon well.

Fig. 7 and Fig 8 illustrate predicted and measured Bode plots for low gain and high gain to validate the above analysis. In Fig. 7, the value of the gain R_2/R_1 is 0.274 (with $R_2 = 0.499$ k Ω) while in Fig. 8, the values of the gain R_2/R_1 are 2.74 ($R_2 = 4.99$ k Ω), 6.81 ($R_2 = 12.4$ k Ω) and 10 ($R_2 = 18.2$ k Ω), respectively. In both cases, the input voltage is 12 V, and loading is 7.5 A.

The Bode plots in Fig. 7 and Fig. 8 resemble the PCMC Bode plot rather closely at low frequencies with a dominant pole located approximately at 175 Hz for both cases. On the other hand, they also look remarkably similar to VMC with a second order resonance at around 30 kHz and 180 kHz, respectively. This type of PCMC-and-VMC-combined Bode plot characteristic is reported in [3]. However, the paper does not provide an explanation to identify the true cause of this unique characteristic for the ACMC Buck converter.

With the mid-frequency current loop gain R_2/R_1 much less than unity, a noticeable second order resonance that occurs in the mid-frequency shown in Fig. 7 corresponds to s_2 and s_3 locations on the complex plane marked as "Start" in Fig. 6. Using (12) and (13), we estimate the resonant frequency and the quality factor to be

$$f_1 = \frac{\omega_1}{2\pi} \approx f_{n1} = \frac{\omega_{n1}}{2\pi} \approx \frac{1}{2\pi} \sqrt{\frac{R_s K_m V_g}{R_1}} \sqrt{\frac{1}{L(C_1 + C_2)}} = 30.82 kHz$$

 $Q_1 \approx Q_{n1} \approx \frac{1}{R_2 C_2} \sqrt{\frac{\kappa_1}{R_s K_m V_g}} \sqrt{L(C_1 + C_2)} = 3.14.$

The measured resonant frequency is approximately equal to



Fig. 8. Predicted (solid lines) and measured (dotted lines) Bode plots showing effects of current loop gain R_2/R_1 on the control-to-output voltage transfer function with $R_2/R_1 = 2.74$, 6.81 and 10, respectively. Input voltage is 12 V, and loading is 7.5 A.

28.18 kHz. It is conceivable that the observed resonance results from the interaction between the converter power stage inductor L and the two capacitors C_1 and C_2 in the current loop compensator with capacitor C_2 being the main contributor because its value is generally much larger than that of capacitor C_1 .

When the gain is equal to or larger than 2.74, the resonant frequency shifts to high frequencies as shown in Fig. 8. There is a noticeable increase in resonant peaking near 180 kHz as the gain R_2/R_1 rises. Using (18) and (19), we estimate the resonant frequency and the quality factor to be

$$f_{2} = \frac{\omega_{2}}{2\pi} \approx f_{n2} = \frac{\omega_{n2}}{2\pi} \approx \frac{1}{2\pi} \sqrt{\frac{R_{s}K_{m}V_{g}}{R_{1}}} \sqrt{\frac{1}{LC_{1}}} = 179.7 \text{ kHz}$$
$$Q_{2} \approx Q_{n2} \approx \frac{R_{2}C_{2}}{(C_{1} + C_{2})} \sqrt{\frac{R_{s}K_{m}V_{g}}{R_{1}}} \sqrt{\frac{C_{1}}{L}} = 1.97.$$

The measured resonant frequency is approximately equal to 170.0 kHz. This observed behavior can be regarded as the interaction between the converter power stage inductor *L* and the capacitor C_1 in the current loop compensator. As can be seen from (18)-(19), when the value of R_2 increases, the quality factor, $Q_2 \approx Q_{n2}$, rises linearly with it, but the resonant frequency, $\omega_2 \approx \omega_{n2}$, remains unchanged.

The above analysis also demonstrates that when the current loop gain R_2/R_1 is either small or large, the resultant second order resonance has a frequency-shifting property. In neither case, the resonant frequency is fixed at half the switching frequency of 250 kHz.

D. Effects of current loop compensator capacitive elements C_1 and C_2 on the control-to-output voltage transfer function

The two capacitive elements C_1 and C_2 in the current loop



Fig. 9. Illustration of pole and zero migration and pole regrouping as capacitor C_1 changes from 10 pF to 220 pF with 12 V input voltage and 7.5 A load.

compensator influence not only the inner current loop but also the outer voltage loop. Fig. 9 illustrates a typical pole and zero movement pattern as capacitor C_1 is varied from 10 pF to 220 pF with 12 V input voltage and 7.5 A load. Initially, with capacitor $C_1=10$ pF, Equation (6) contains four real poles lying on the real axis. As the capacitor value increases, poles s_3 and s_4 move toward each other on the real axis while other poles and zeros stay essentially where they are from their starting points. When the value of the capacitor C_1 is large enough, a pair of complex conjugates is formed at intersecting Point X_2 . While the quality factor of the second order term in (16) rises with the increase in value of capacitor C_1 , the resonant frequency decreases. This property can be well predicted by (18)-(19).

It can be shown that with an input voltage of 5 V, all the four poles remain on the real axis throughout the capacitor C_1 varying range. This behavior simply implies that under this combined circuit parameter and low input voltage operating condition, the system possesses ample internal damping to not have a high-frequency second order resonance as shown in the previous case in Fig. 9.

Fig. 10 illustrates analysis results of pole and zero movement pattern when capacitor C_2 is varied from 1800 pF to 0.047 µF with 12 V input voltage. With the initial capacitor value C_2 being equal to 1800 pF, the system transfer function (6) contains two real poles s_1 and s_2 as well as a complex conjugate pole pair s_3 and s_4 , all marked as "Start" on the plot. As the value of capacitor C_2 increases, both the mid-frequency zero s_{z2} and pole s_2 are affected, and they move toward lower frequencies as predicted by (7) and (17). The pole and the zero are rather close in frequency, and they tend to cancel each other throughout the process. The second order term in (16) or the high-frequency portion of the transfer function is much less sensitive to this capacitor value



Fig. 10. Illustration of pole and zero migration as capacitor C_2 changes from 1800 pF to 0.047 μ F with 12 V input voltage and 7.5 A load.



Fig. 11. Illustration of pole and zero migration and pole regrouping as capacitor C_2 changes from 1800 pF to 0.047 μ F with 5 V input voltage and 7.5 A load.

variation except when the values of the two capacitors C_1 and C_2 are comparably close. This causes a slight increase in the imaginary parts of the pole pair s_3 and s_4 .

The operating case with 5 V input and 7.5 A load is illustrated in Fig. 11. Under this condition, the model that best describes the system small-signal dynamic behavior is given by (10) with the initial value $C_2 = 1800$ pF. The mid-frequency poles s_2 and s_3 marked as "Start" points are a pair of complex conjugates. As the value of capacitor C_2 rises, the quality factor $Q_1 \approx Q_{n1}$ reduces, resulting in more damping of the second order term in (10). When the value of capacitor C_2 is sufficiently large, poles s_2 and s_3 become two real poles, moving in the opposite direction on the real axis as capacitor C_2 continues to increase.



Fig. 12. Predicted (solid lines) and measured (dotted lines) Bode plots showing effects of capacitor C_1 on the control-to-output voltage transfer function with C_1 =47 pF and 220 pF, respectively. Input voltage is 24 V, and loading is 7.5 A.

Comparing the effects of the two capacitive elements C_1 and C_2 on the pole and zero movement patterns in Fig. 9 to Fig. 11, we can conclude that capacitor C_1 influences mainly the high frequency portion of the control-to-output voltage transfer function while C_2 the mid-frequency portion of the control-to-output voltage transfer function.

Fig. 12 and Fig. 13 reveal predicted and measured Bode plots of the control-to-output voltage transfer function when capacitors C_1 and C_2 values are varied to validate the above analysis. To demonstrate more clearly the high-frequency effect of capacitor C_1 on the control-to-output voltage transfer function, the input voltage is set at 24 V under which any resonant peaking is more visible. Fig. 12 exhibits that as the value of capacitor C_1 increases from 47 pF to 220 pF, the initial resonance at the frequency near 370 kHz reduces to around 170 kHz. Meanwhile, the quality factor of this high-frequency second order term increases. As a result, more resonant peaking at the lower frequency point is evident. Using (18)-(19), we predict that the resonant frequency corresponding to $C_1 = 220$ pF is $f_{n2} = \omega_{n2}/2\pi = 171.3$ kHz and quality factor $Q_{n2} = 1.108$. This compares with the predicted resonant frequency $f_{n2} = \omega_{n2}/2\pi = 370.4$ kHz and quality factor $Q_{n2} = 0.538$ for $C_1 = 47$ pF.

It is also noticed that with a much larger value of C_1 , both predicted gain and phase of the Bode plot match those of the measured data with good accuracy up to nearly 250 kHz, or half the switching frequency. This results from lower ripple contents at the output of the current loop amplifier, which makes the model more accurate.

The effect of capacitor C_2 on the Bode plot of the control-to-output voltage transfer function is shown in Fig. 13. As predicted by (17)-(19), when the capacitor value is varied in such a wide range, it affects solely the transfer function in the mid-frequency range. Its high-frequency effect on the transfer function is barely noticeable.



Fig. 13. Predicted (solid lines) and measured (dotted lines) Bode plots showing effects of capacitor C_2 on the control-to-output voltage transfer function with $C_2 = 1800$ pF and 0.047 uF, respectively. Input voltage is 12 V, and loading is 7.5 A.

E. Effects of operating parameters on the control-tooutput voltage transfer function

Operating parameters include converter loading and input voltage. When loading varies, both (10) and (16) predict that it predominantly affects the low-frequency pole, s_1 . Fig. 14 shows the Bode plots of the predicted and measured control-to-output voltage transfer function with 12 V input voltage under the loading conditions of 5 A, 10 A and 15 A, respectively. It is seen from (11) that the simplified expression for estimating this low-frequency pole, $s_1 \approx s_{p1}$, has three terms in the denominator. In practical designs, the first term, $[(R_L+r_c)C]$, usually dominates, which is nearly the same as the low-frequency dominant pole for the PCMC Buck converters. Because of this, the low-frequency response characteristics of the ACMC Buck converter are nearly the same as those of PCMC [8]-[10].

Pole migration and regrouping of the control-to-output voltage transfer function also take place when the input voltage changes. With the input voltage varied from 5 V to 24 V, which corresponds to a duty cycle variation from 0.68 to 0.14, it can be readily shown that a typical pattern is very similar to that of the modulator gain $K_{\rm m}$ illustrated in Fig. 3. This is because both the modulator gain and the input voltage are related with the resonant frequency and the quality factor the same way as modeled by the expressions (12)-(13) and (18)-(19). Pole movement under the condition of duty cycle changes is discussed briefly in [5], and the results reported in this paper provide an analytical explanation and confirm further the author's observations. Fig. 15 illustrates Bode plots of predicted and measured control-to-output voltage transfer function as the input voltage varies. As shown in the Bode plots, when the input voltage is low, the system inherently has a high level of damping which is predicted by (13). Rising input voltage causes poles to migrate and regroup, ultimately resulting in increases in both the resonant



Fig. 14. Predicted (solid lines) and measured (dotted lines) Bode plots showing effects of loading on the control-to-output voltage transfer function with various loads of 5 A, 10 A and 15 A, respectively.



Fig. 15. Predicted (solid lines) and measured (dotted lines) Bode plots showing effects of input voltage variation from 5 V to 24 V on the control-to-output voltage transfer function.

frequency and quality factor of the second order term in (16). The mid-frequency range pole and zero tend to cancel each other due to proximity of their locations. Because of this, for practical designs, Equation (16) can be further simplified to

$$T_{p}(s) \approx \frac{R_{L}}{R_{S}} \frac{(1+r_{c}Cs)}{(1+\frac{s}{s_{p1}})(1+\frac{s}{\omega_{n2}Q_{n2}}+\frac{s^{2}}{\omega_{n2}^{2}})} \quad .$$
(26)

This is the minimum order control-to-output voltage transfer function for the ACMC Buck converter operating under a low duty cycle. Equation (26) distinctly illustrates similarities and differences between ACMC and PCMC with or without considering sampling effect [8]-[10].

IV. CONCLUSIONS

A detailed and in-depth study of effects of converter circuit and operating parameters on the small-signal dynamics of ACMC Buck converters has been presented. Despite some similarities between ACMC and PCMC, the study reveals a number of interesting properties and insight into ACMC that are not present for PCMC.

For the inner current loop, the paper shows the importance of proper selection of mid-frequency current loop gain R_2/R_1 from the point of view not only maintaining switching stability but also the current loop crossover frequency if the converter is to be designed to operate in a wide input range.

For the outer voltage loop, it is shown that the poles and zeros of the ACMC Buck converter control-to-output transfer function are very sensitive to variations of both converter circuit and operating parameters. In particular, the paper provides specific details to reveal how and in what frequency the poles and zeros are affected by these parameter changes. The study also demonstrates that while current feedback makes the ACMC Buck converters possess characteristics of the PCMC Buck converters, there exist strong interactions between the power stage inductive element and the current loop compensator capacitive elements. This makes the ACMC Buck converters also possess characteristics of VMC Buck converters in both mid and high frequencies, depending on the circuit and operating parameters. Understanding these sole characteristics of ACMC enables us to develop more effective design strategies on an analytical basis.

REFERENCES

- L. H. Dixon, "Average current-mode control of switching power supplies," Unitrode (Texas Instruments) Power Supply Design Seminar Manual, 1990.
- [2] J. Sun, R. Bass, "Modeling and practical design issues for average current control," *in Proc. APEC*, Vol. 2, pp. 980-986, 1999.
- [3] T. Suntio, J. Lempinen, I. Gadoura, K. Zenger, "Dynamic effects of inductor current ripple in average current mode control," *in Proc. PESC*, pp. 1259-1264, 2001.
- [4] W. Tang, F. Lee and R. B. Ridley, "Small-signal modeling of average current-mode control," *IEEE Tran. Power Electron.*, Vol. 8, No. 2, pp. 112-119, Apr. 1993.
- [5] P. Cooke, "Modeling average current mode control," in Proc. APEC, Vol. 1, pp. 256-262, 2000.
- [6] R. Li, "Modeling average-current-mode-controlled multiphase Buck converters," *in Proc. PESC*, pp. 3299-3305, 2008.
- [7] R. Li, T. O'Brien, J. Lee, J. Beecroft, "A Unified smallsignal analysis of DC-DC converters with average current mode control," *in Proc. ECCE*, pp. 647-654, 2009.
- [8] R. W. Erickson, D. Maksimovic, *Fundamentals of Power Electronics*, 2nd Edition, Kluwer Academic Publishers, 2001.
- [9] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Trans. Power Electron.*, Vol. 2, No. 2, pp. 109-124, Apr. 1987.
- [10] R. Ridley, "A new, continuous-time model for currentmode control," *IEEE Trans. Power Electron.*, Vol. 6, No. 2, pp. 271-280, Apr. 1991.



Ruqi Li received his B.S.E.E degree from Wuhan Univ., Wuhan, China in 1982 and an M.S.E.E as well as Ph.D. degrees from Oregon State Univ., Corvallis, Oregon, USA in 1988 and 1991, respectively. He worked at the Univ. of California, Berkeley, Exponent Inc. and Emerson Network Power as a

Researcher, Consulting Engineer and Senior Design Engineer from 1991 to 2000. Currently, he is a member of the technical staff in the Services Routing Technology Group at Cisco Inc., designing and developing power systems for Cisco's networking products. His professional interest includes Power Systems, Adjustable Speed Motor Drives and Static Power Conversion.



Tony O'Brien received a B.S.E.E. from Rensselaer in 1973. His career includes R&D for power supplies, DC-DC converters and Engineering Management at Artesyn (now Emerson Network Power), Martek Power, and Micrel Semiconductor. Patents include a High Efficiency L.F. Transmitter and a High

Frequency Switching Regulator. He has been managing the Power Systems Engineering for Services Routing Technology Group at Cisco, Inc. since 2006. He is a member of IEEE.



John Lee received his B.S.C.E. in 1976 from National Chungshing Univ., Taichung, Taiwan and M.S.E.E. from Virginia Tech., Blacksburg, VA in 1988. His working experience includes Power Generation Div., Taiwan Power Company, Rockdyne Div. (International Space Station power system),

Rockwell International, Lockheed Martin Missile & Space, Lucent Technology and Delta Electronic, Inc. He has been with Cisco Inc. as a Power Electronics Engineer since 2004. He is a member of IEEE.



John Beecroft received a B.Sc in electrical and electronic eng., and an M.Sc in Systems eng. from Surrey Univ., Guildford, UK, in 1980 and 1984, and is a professional engineer registered with the Engineering Council UK. He has spent his career working on the design of switched mode

power supplies from 5 W up to 5 kW at several companies in the UK and USA. He has spent the last 5 years at Cisco Systems in San Jose, California where he is responsible for the integration of custom power supplies into new networking systems. He is a member of the IET (UK) and a senior member of the IEEE.



Kenny Hwang received the B.S. degree in Electrical Engineering from Chung-Ang University, Seoul, Korea in 1989. He worked for Hewlett Packard Co. for 9 years and then Samsung Electronics for 3 years. He has been with Cisco Inc. in San Jose, California, USA since 2006. He is engaged

in DC/DC converter, PoE, and VR12 designs.